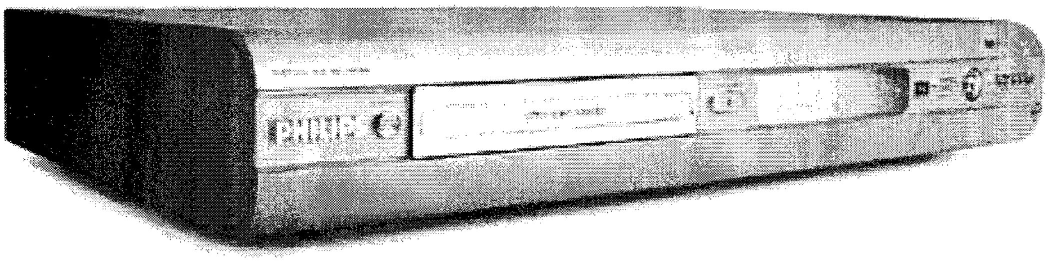
VIDE-V31805

DVD-Video Recorder DVDR610, DVDR615 & DVDR616

DVDR610/00/02/05/19/33, DVDR615/00/02/05/19/33
DVDR616/00/02/05

Service
Service
Service



Service Manual

CLASS 1
LASER PRODUCT

DVD+ReWritable

COMPACT DISC DIGITAL VIDEO

COMPACT DISC DIGITAL AUDIO

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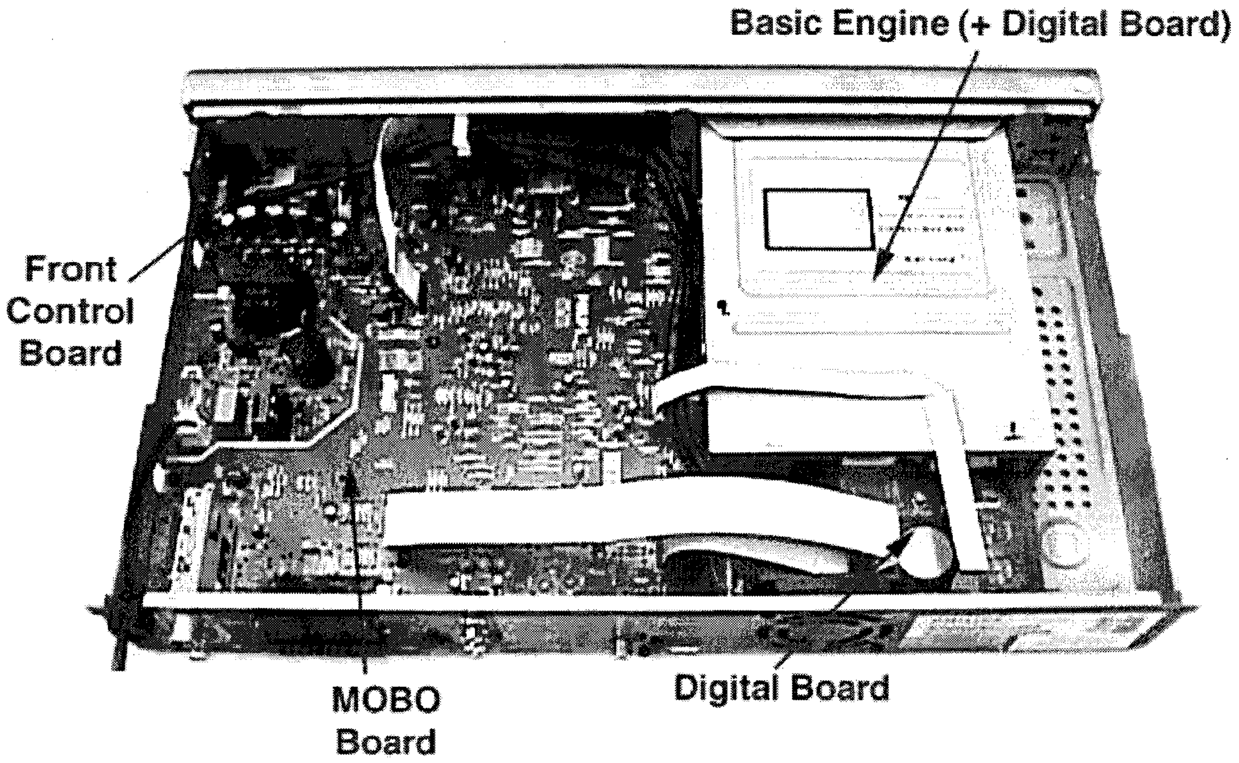
Version 1.1

PHILIPS

1. Technical Specifications and Connection Facilities

1.1 PCB Locations



1.2 Diversity Matrix and Read and Write speed

Module / Pcb Application	VFM RANGE		
	DVDR610/0x/19/33	DVDR615/0x/19/33	DVDR616/0x/19/33
MOBO 04 E1 12NC: 3139 248 82891	x	x	x
VAU8041/11 DS version: E2_AV3_4 12NC: 9305 025 84111 FEBE pcb: 3104 128 09271 Drive: AV3.5	x		
VAU8041/21 DS version: E1_AV3_4 12NC: 9305 025 84121 pcb: 3104 128 09281 Drive: AV3.5		x	x
LECOLITE U4.01L DS version: OL22FEBE 12NC: 3139 247 10942 pcb: 3139 248 83791 Drive: D4.0	x		

Type of Disc (Function)	Disc Rotation Speed
Read Speed CD	CAV 7x
Read Speed DVD	CAV 4x
Write Speed DVD+RW	ZCAV 2.4x
Write Speed DVD+R	ZCAV2.4x

1.3 General:

Mains voltage	: 198V-276V
Mains frequency	: 43 Hz - 63Hz
Power consumption (record)	: 27 W
Power consumption (AV loop through)	: < 15W
Power consumption low power stand-by	: < 3 W

1.4 RF Tuner

Test equipment:Fluke 54200 TV Signal generator
Test streams:PAL BG Philips Standard test pattern

1.4.1 System:

PAL B/G, PAL D/K, SECAM L/L', PAL I

1.4.2 RF - Loop Through:

Frequency range	: 45 MHz - 860 MHz
Gain: (ANT IN - ANT OUT)	: -6 dB to 0dB

1.4.3 Radio Interference:

input voltage /3 tone method (+40 dB min)	: no limit

1.4.4 Receiver:

PLL tuning with AFC for optimum reception

Frequency range: : 45.25 MHz - 857 MHz
Sensitivity at 40 dB S/N : ≥ 60dBμV at 75Ω (video unweighted)

1.4.5 Video Performance:

Channel 25 / 503,25 MHz,
Test pattern: PAL BG PHILIPS standard test pattern,
RF Level 74 dBV
Measured on SCART 1
Frequency response: : 0.1- 4.00 MHz ± 3dB
Group delay (0.1 MHz - 4.4 MHz) : 0 nsec ± 150nsec

1.4.6 Audio Performance:

Audio Performance Analogue - HiFi:
Frequency response at SCART 1 (L+R) output: : 100 Hz - 12 kHz / 0± 3dB
S/N according to DIN 45405, 7, 1967 and PHILIPS standard test pattern video signal: : ≥ 50dB, unweighted
Harmonic distortion (1 kHz, ± 25 kHz deviation): : ≤ 1.5%

Audio Performance NICAM:
Frequency response at SCART 1(L+R) output: : 40 Hz - 15 kHz 0 ± 3dB
S/N according to DIN 45405, 7, 1967 and PHILIPS standard test pattern video signal: : ≥ 60 dB unweighted
Harmonic distortion (1 kHz): : ≤ 0.5 %

1.4.7 Tuning

Automatic Search Tuning
scanning time without antenna : typ. 3 min.
stop level (vision carrier) : ≥ 37dBμV
Maximum tuning error of a recalled program : ± 62.5 kHz
Maximum tuning error during operation : ± 100 kHz

Tuning Principle
automatic B,G, I, DK and L/L'detection
manual selection in "STORE" mode

1.5 Analogue Inputs / Outputs

1.5.1 SCART 1 (Connected to TV)

Pin Signals:

1	- Audio R	1.8V RMS	⊖→
2	- Audio R		→⊖
3	- Audio L	1.8V RMS	⊖→
4	- Audio GND		⏚
5	- Blue/Chroma GND		⏚
6	- Audio L		→⊖
7	- Blue out/ Chroma in	0.7Vpp ± 0.1V into 75 Ohm (*)	⊟→
8	- Function switch	<2V = TV >4.5V / <7V = asp. ratio 16:9 DVD >9.5V / <12V = asp. ratio 4:3 DVD	⊖→
9	- Green GND		⏚
10	- P50 control		⊟→
11	- Green	0.7Vpp ± 0.1V into 75 Ohm (*)	⊟→
12	- Nc		
13	- Red/Chroma GND		⏚
14	- fast switch GND		⏚
15	- Red out/ Chroma out	0.7Vpp ± 0.1V into 75 Ohm (*) ± 3dB 0.3Vpp Chroma (burst)	⊟→
16	- fast switch	RGB/ CVBS or Y <0.4V into 75 Ohm = CVBS >1V / <3V into 75 Ohm = RGB	⊖→
17	- Y/CVBS GND OUT		⏚
18	- Y/CVBS GND IN		⏚
19	- CVBS/Y	1Vpp ± 0.1V into 75 Ohm (*)	⊟→
20	- CVBS/Y		→⊟
21	- Shield		⏚

1.5.2 SCART 2 (Connected to AUX)

Pin Signals:

1	-Audio R	1.8V RMS	⊖→
2	-Audio R		→⊖
3	-Audio L	1.8V RMS	⊖→
4	-Audio GND		⏚
5	-Blue/Chroma GND		⏚
6	-Audio L		→⊖
7	-Blue in/ Chroma out	± 3dB 0.3Vpp Chroma (burst)	⊟→
8	-Function switch		→⊖
9	-Green GND		⏚
10	-P50 control		⊟→
11	-Green in		→⊟
12	-Nc		
13	-Red/Chroma GND		⏚
14	-fast switch GND		⏚
15	-Red in/Chroma in		→⊟
16	-fast switch RGB/ CVBS or Y		→⊖
17	-CVBS GND OUT		⏚
18	-CVBS GND IN		⏚
19	-CVBS/Y/RGB sync	1Vpp ± 0.1V into 75 Ohm (*)	⊟→
20	-CVBS/Y		→⊟
21	-Shield		⏚

(*) for 100% white

1.5.3 Audio/Video Front Input Connectors

Audio - Cinch
Input voltage : 2.2 Vrms
Input impedance : >10kΩ

Video - Cinch
Input voltage : 1 Vpp ± 3dB
Input impedance : 75 Ω

Video - YC (Hosiden)
According to IEC 933-5
Superimposed DC-level on pin 4 (load > 100kΩ)
< 2.4V is detected as 4:3 aspect ratio
> 3.5V is detected as 16:9 aspect ratio
Input voltage Y : 1Vpp ± 3dB
Input impedance Y : 75 Ω
Input voltage C : burst 300 mVpp ± 3 dB
Input impedance C : 75 Ω

1.5.4 Audio/Video Output rear Connectors

Audio- Cinch
Output voltage : 2Vrms max.
Output impedance : >10kΩ

Video- Cinch
Output voltage : 1 Vpp ± 3dB

Output impedance : 75 Ω

Video - YC (Hosiden)
According to IEC 933-5
Superimposed DC-level on pin 4 (load > 100kohm)
< 2.4V is detected as 4:3 aspect ratio
> 3.5V is detected as 16:9 aspect ratio
Output voltage Y : 1Vpp +10/-15%
Output voltage C : 300mVpp +1/-4dB

1.6 Video Performance

All outputs loaded with 75 Ohm
SNR measurements over full bandwidth without weighting.

1.6.1 SCART (RGB)

SNR : > -65 dB on all output
Bandwidth : 4.8 MHz ± 2dB

1.7 Audio Performance CD

1.7.1 Cinch Output Rear

Output voltage 2 channel mode : 2Vrms ± 2dB
Channel unbalance (1kHz) : <1dB
Crosstalk 1kHz : >95dB
Crosstalk 16Hz-20kHz : >87dB
Frequency response 20Hz- 20kHz : ±0.2dB max
Signal to noise ratio : >85 dB
Dynamic range 1kHz : >83dB
Distortion and noise 1kHz : >83dB
Distortion and noise 16Hz-20kHz : >75dB
Intermodulation distortion : >70dB
Mute : >95dB
Outband attenuation: : >40dB above 30kHz

1.7.2 Scart Audio

Output voltage 2 channel mode : 1.6Vrms ± 2dB
Channel unbalance (1kHz) : <1dB
Crosstalk 1kHz : >85dB
Crosstalk 16Hz-20kHz : >70dB
Frequency response 20Hz- 20kHz : ± 0.2dB max
Signal to noise ratio : >80 dB
Dynamic range 1kHz : >75dB
Distortion and noise 1kHz : >75dB
Distortion and noise 16Hz-20kHz : >50dB
Intermodulation distortion : >70dB
Mute (spin-up, pause, access) : >80dB
Outband attenuation: : >40dB above 25kHz

1.8 Digital Output

1.8.1 Coaxial

CDDA/LPCM (incl MPEG1) : according IEC958
MPEG2, AC3 audio : according IEC1937
DTS : according IEC1937, amendment 1

1.9 Digital Video Input (IEEE 1394)

1.9.1 Applicable Standards

Implementation according:
IEEE Std 1394-1995
IEC 61883 - Part 1
IEC 61883 - Part 2 SD-DVCR (02-01-1997)
Specification of consumer use digital VCR's using 6.3 mm magnetic tape - dec.1994
Mechanical connection according:
Annex A of 61883-1

1.10 P50 System Control

Via SCART pin nr 10

1.11 Dimensions and Weight

Height of feet : 5.5mm
Apparatus tray closed : WxDxH :435 x 285x 65mm
Apparatus tray open : WxDxH :435 x 422x 65mm
Weight without packaging : app. 4 kg ± 0.5 kg
Weight in packaging : app. 6.5 kg

1.12 Laser Output Power & Wavelength

1.12.1 DVD

Output power during reading : 0.8mW
Output power during writing : 20mW
Wavelength : 660nm

1.12.2 CD

Output power : 0.3mW
Wavelength : 780nm

2. Safety Information, General Notes

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:

- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol ⚠, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:

- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
  1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
  2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
  3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
  4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
  5. Verify this, before you return the unit to the customer/ user (ref. UL-standard no. 1492).
  6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	:	Semiconductor laser GaAlAs
Wavelength	:	650 nm (DVD)
	:	780 nm (VCD/CD)
Output Power	:	20 mW (DVD+RW writing)
	:	0.8 mW (DVD reading)
	:	0.3 mW (VCD/CD reading)
Beam divergence	:	60 degree

CLASS 1
LASER PRODUCT

Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ⚠). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential.
  Available ESD protection equipment:
  - Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
  - Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply (pos. 1005), including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off'!). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGA UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

Figure 2-2

2.2.3 Notes

Dolby

Manufactered under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works.
©1992-1997 Dolby Laboratories, Inc. All rights reserved.

DOLBY SURROUND
PRO • LOGIC

Figure 2-3

Trusurround

TRUSURROUND, **SRS** and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence frm SRS labs, Inc.

Figure 2-4

Video Plus

"Video Plus+" and "PlusCode" are registered trademarks of the Gemstar Development Corporation. The "Video Plus+" system is manufactored under licence from the Gemstar Development Corporation.

Figure 2-5

Macrovision

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners.

Use of this copyright protection technology must be autorized by Macrovision Corporation, and is intended for home and other limited viewing uses only unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

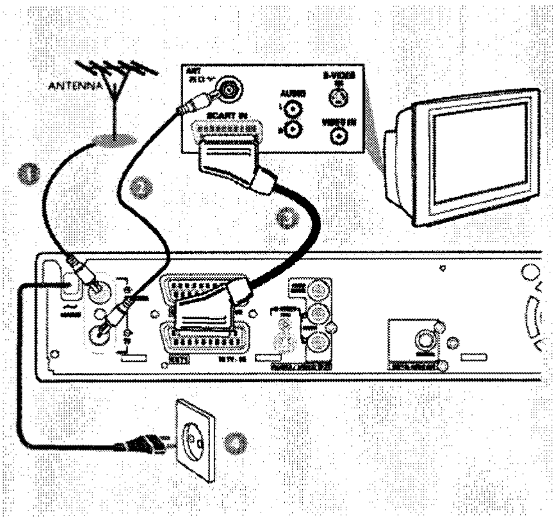
3. Directions For Use

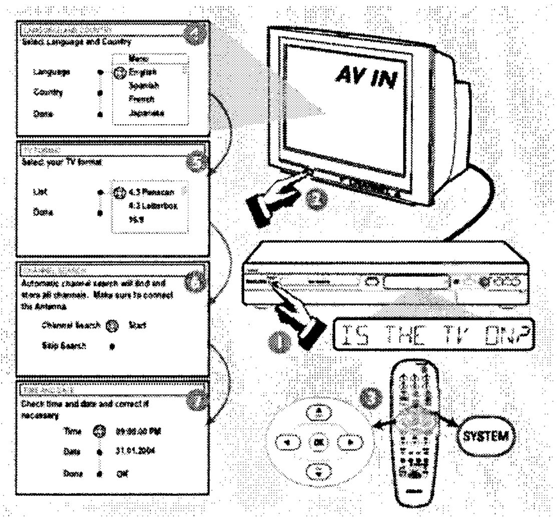
The following excerpt of the Quick Use Guide serves as an introduction to the set.
The complete Direction for Use can be downloaded in different languages from the internet site of Philips Customer Care Center:
www.p4c.philips.com

QUICK USE GUIDE

DVDR610
DVDR615
DVDR616

12nc: 3139 246 14051





1 First connect

1. Remove the antenna cable plug from your TV (or Satellite Receiver/Cable Box). Connect it to the **ANTENNA IN** socket at the back of the DVD recorder.
2. Use the supplied antenna cable to connect the DVD recorder's **TV OUT** socket to the antenna input socket at the back of your TV set
3. Use the supplied scart cable to connect the DVD recorder's **EXT 1 TO TV-I/O** socket to the SCART socket at the back of your TV set.
4. Connect the power cable from the DVD recorder's ~ **MAINS** to the power supply.

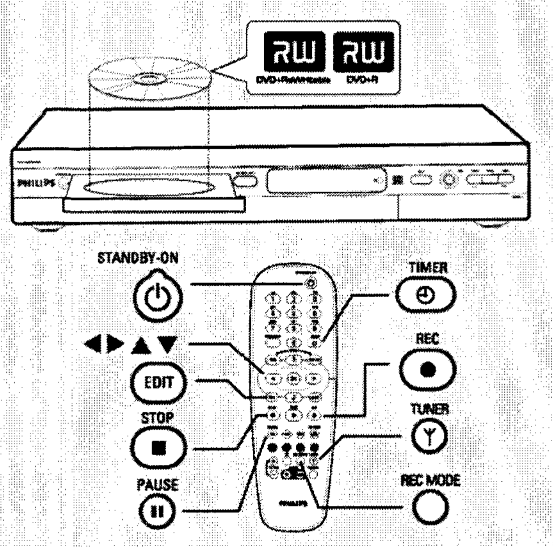
Helpful Hints:
If your TV does not have the above-mentioned connectors, please refer to the user manual for more information on others possible connection to your TV set.

2 Start first installation

1. Press **STANDBY-ON** ⏻ on the DVD recorder to switch it on.
2. Switch on the TV set.
   If the first installation menu does not appear, press the CHANNEL ▲ ▼ button on the TV to select the correct video in channel, for example, 'EXT', '0', or 'AV'.
3. Press ▲ ▼ to select an item in the menu.
   Press ▶ to access the selected item's options.
   Press ◀ to confirm your selection.
   Once completed, select { **Done** } in the menu and press **OK** to continue.
4. { **Language and Country** } menu appears.
   { **Language** } – select on-screen display language.
   { **Country** } – select country of your residence.
5. { **TV Format** } menu appears.
   { **List** } – select TV screen display.
6. { **Channel Search** } menu appears.
   Press **OK** to start automatic TV channel search.
   → Once completed, the total number of channels found appears on the TV.
7. { **Time and Date** } menu appears.
   If the time and date shown on the TV are not correct, press ▶ to enter the respective time/date field. Press ▲ ▼ to change the first digit and press ▶ to go to the next digit field. Once completed, press **OK**.
8. Press ▼ to select { **Done** } and press **OK** to save the changes.
   → The initial installation is now completed.

The DVD recorder is ready for use!

ooo cont.



Preparation before recording :

① Insert a recordable DVD+R(W).
→ If the DVD+RW already contained recordings, you have to select an empty title in the Index Picture screen to start a new recording.
→ For DVD+R, the recording will make at the end of the disc automatically.

② Press **REC MODE** to select a recording mode ({M1}, {M2}, {M2x}, {M3}, {M4}, {M6} or {M8}). It defines the picture quality and the maximum recording time for a disc. Refer to the "Recording settings" in the user manual for more information.

3 Start a manual recording

① Press **TUNER** on the remote control to see the TV programmes, then press ▲ ▼ to select the programme number (or external input channel, for example EXT1, CAM1) you wish to record.
→ The input channel must correspond to the socket to which you have connected the additional device.

② Press **REC ●** to start recording.

- If required, you can press **REC ●** twice to start a 30-minute recording. Each time you press **REC ●** button, you will add 30 minutes to the recording time.

③ During recording, you may press **PAUSE II** to pause the recording and press **REC ●** to continue.

④ To stop the recording, press **STOP ■**.
→ Wait until the 'MENU UPDATE' message disappears from the display panel before you remove the disc.

To play the DVD+R on other DVD players, you must finalise it first

① Press **EDIT** on the remote control.

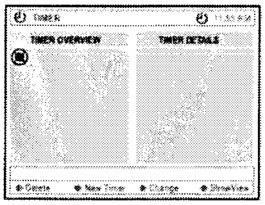
② Press ▲ ▼ to select { **Finalise** } in the menu and press **OK** to start finalising the DVD+R.

Once finalised, no further recordings and editings can be made to the DVD+R. Unfinalise a DVD+R is not possible.

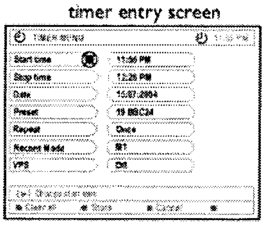
4 Prepare timer recording

① Press **TIMER**.
→ The timer overview appears.

timer overview



timer entry screen



Start time 11:56 PM
Stop time 12:26 PM
Date 15/07/2004
Preset 19 BBC24
Repeat Once
Record Mode M1
VPS Off

② Press the matching colour coded button on the remote control to select { **New Timer** }.
→ The timer entry screen appears.

③ Use ▲ ▼ ◀ ▶ to select the appropriate entry field.

④ Use ▲ ▼ ◀ ▶ to enter the programme information (or use the **alphanumeric keypad 0-9**), then press **OK** to confirm.

⑤ Once completed, press the matching colour coded button on the remote control to select { **Store** }.
→ The timer overview screen will appear showing the stored programme information.

⑥ To exit, press **TIMER**.

⑦ Press **STANDBY-ON** to switch off the DVD recorder.
→ The DVD recorder must be off in order for the timer recording to occur, at least five minutes before the timer recording is set to begin.

Detailed playback features and additional functions are described in the accompanying user manual.

4. Mechanical Instructions

4.1 Dismantling and Assembly of the Set

For item numbers please see the exploded views in chapter 10.

4.1.1 Front Panel Assembly

- After removing the top cover, remove tray front 134+138, see picture 4-1
- Remove the three screws 188
- Release the two snap hooks on the sides and remove the front assembly
- Remove the 4 screws 186 to remove the front plate 184, see picture 4-2

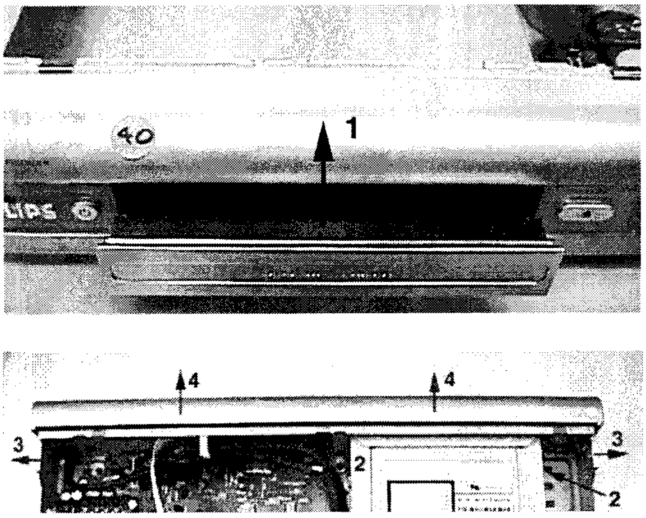


Figure 4-1

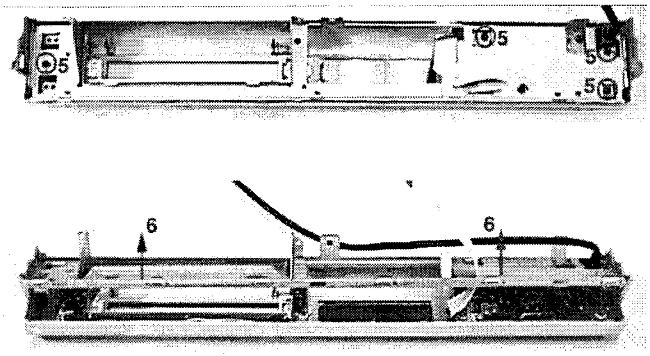


Figure 4-2

4.1.2 Basic Engine

- Remove the Front Panel Assembly as given in 4.1.1
- Remove the 6 screws 260, 269 to free the Basic Engine
- Remove the dust cover assembly 147 and 148
- Loosen 2 screws to remove bracket 256
- Loosen 4 screws to remove the Basic Engine metal casing
- Place the Basic Engine in the service position

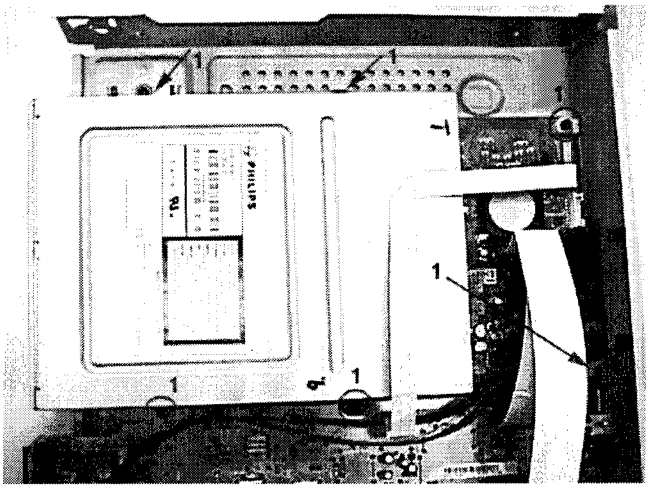


Figure 4-3

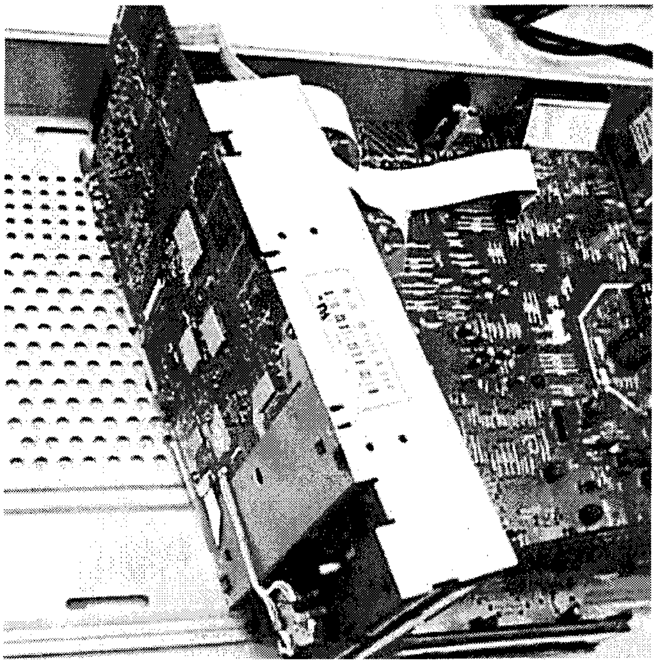


Figure 4-4

4.1.3 MOBO Board

- Remove the Front Panel assembly as given in 4.1.1
- Remove 6 screws 246 and 254
- Remove 4 screws 270
- Service position is achieved by flipping the MOBO board above the Basic Engine

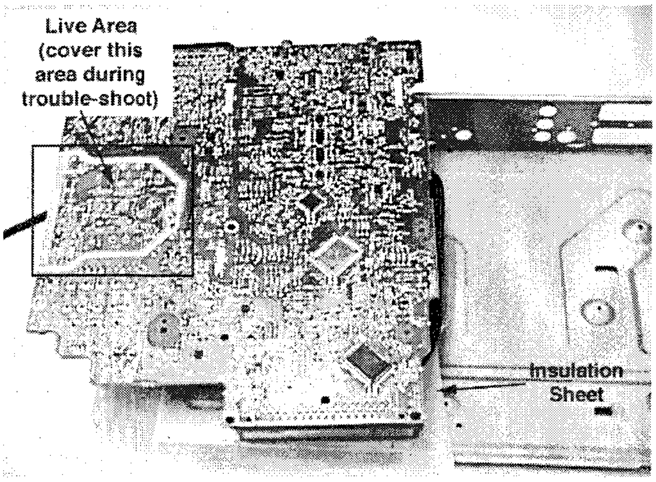


Figure 4-5

4.2 Dismantling and assembly of the Basic Engine

4.2.1 General

Follow the dismantling instructions in described order.
Do not place the unit with its PCB on a hard surface (e.g. table), as it could damage the components on it.
Always place something soft (a towel or foam cushion) under it.
Never touch the lens of the OPU.
Take sufficient ESD measures during handling.

4.2.2 Dismantling the FEBE Board / Lecolite (LECO) Board

- Remove 4 screws to remove the metal case 150+180
- Remove 2 screws to separate the P.C. board 179 or 180 from the main Loader/Drive assembly

Note: After exchange of the PCB (or the Drive mechanism) the complete Basic Engine has to be adjusted! Refer to chapter 8 for adjustment instructions!

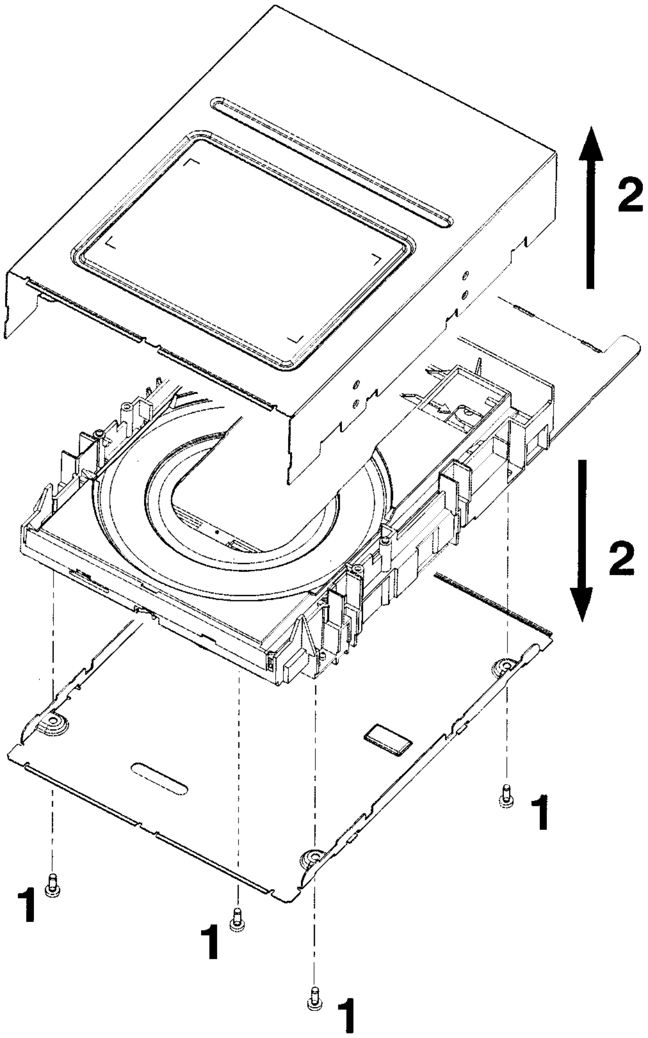


Figure 4-6 Basic Engine Module dismantling

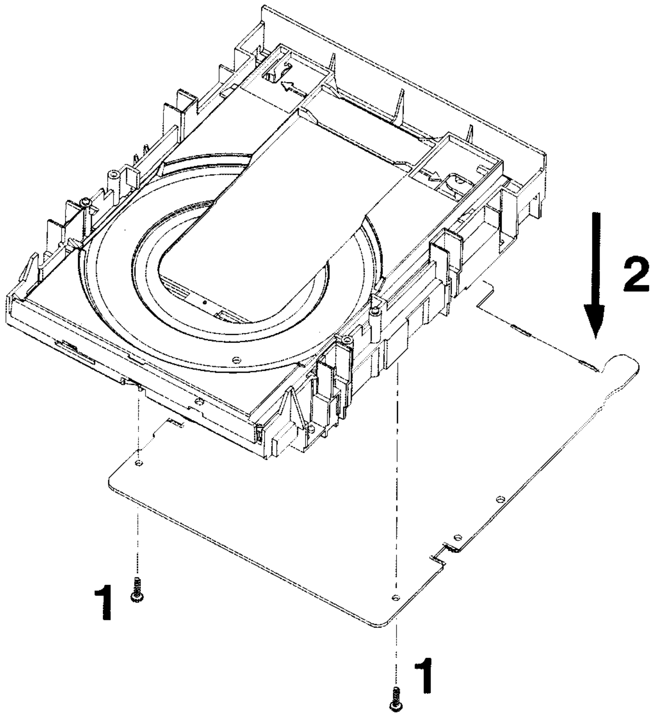


Figure 4-7 Remove P.C. board

4.2.3 Dismantling the Tray

- Remove the encasing as described in 4.2.2
- Disengage the two holders that fix the tray [1] and pull out the tray [2]

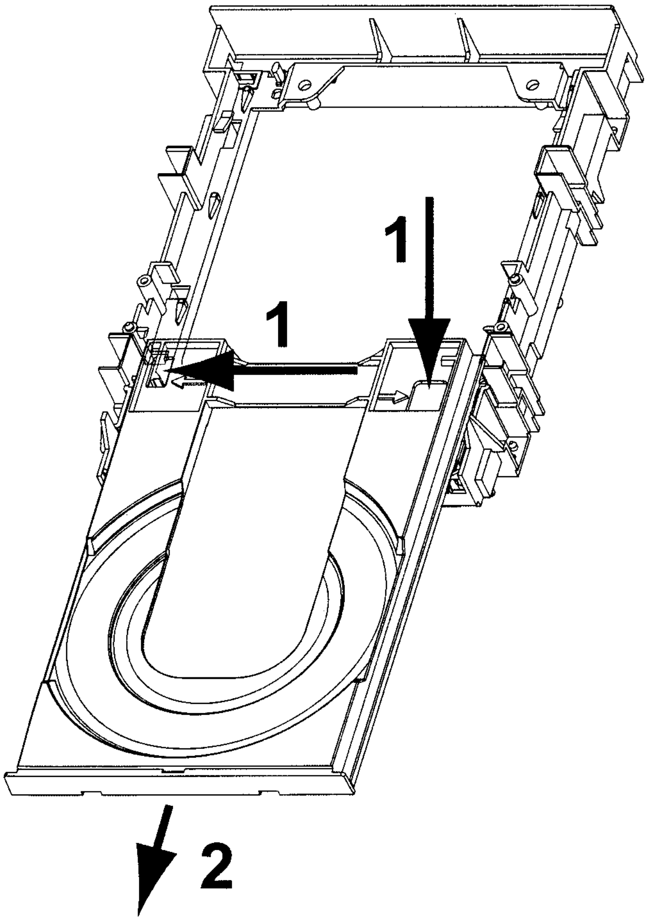


Figure 4-8 Remove Tray

4.2.4 DVD-M (Drive Mechanism)

Caution: Never try to align or repair the DVD-Module itself! Only the factory can do this properly. Service engineers are only allowed to exchange the sledge motor assy.
After Exchanging the DVD-M (or the PCB) the complete drive has to be adjusted! Refer to chapter 8 for adjustment instructions!

- Remove encasing and P.C. board as described in 4.2.2
- Remove the Sealing strip 5 by uncatching it
- Loosen the 4 screws/washer [1] to remove the DVD-M [2]

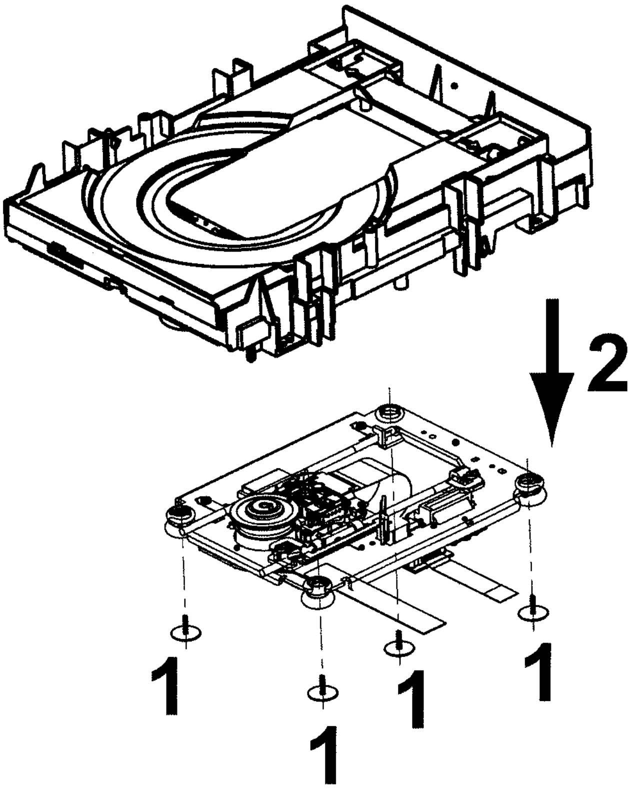


Figure 4-9 Remove DVD-M

4.2.5 Re - assembly

To re-assemble the module, do all processes in reverse order. Take care of the following:

- **Heat Paths:** Put the 5 heat paths (gray rubber pieces) back to their position on the ICs.
- **Complete module:** Place all wires/cables in their original positions
- **Emergency opening slot:** Be sure that the slot for the emergency tray opener is covered by adhesive tape!

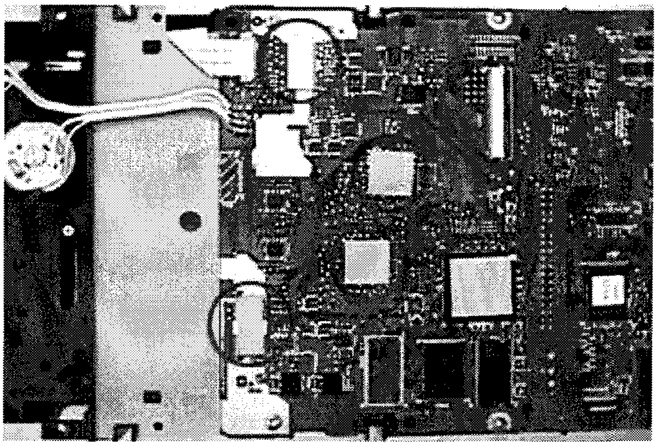
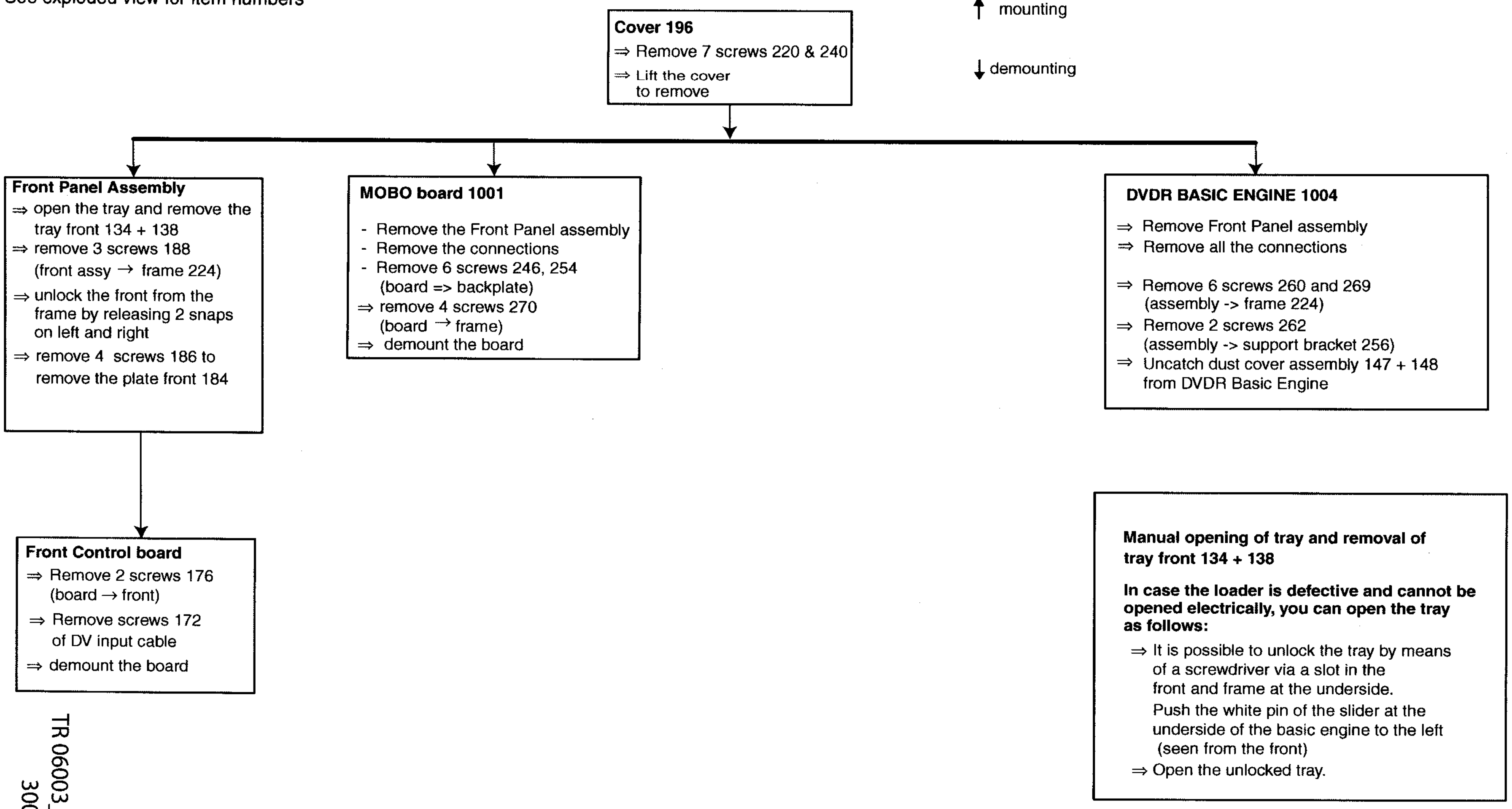


Figure 4-10 Heat Paths

4.3 Dismantling Instructions

DISMANTLING INSTRUCTIONS

See exploded view for item numbers



Cover 196

⇒ Remove 7 screws 220 & 240

⇒ Lift the cover to remove

Front Panel Assembly

⇒ open the tray and remove the tray front 134 + 138

⇒ remove 3 screws 188 (front assy → frame 224)

⇒ unlock the front from the frame by releasing 2 snaps on left and right

⇒ remove 4 screws 186 to remove the plate front 184

Front Control board

⇒ Remove 2 screws 176 (board → front)

⇒ Remove screws 172 of DV input cable

⇒ demount the board

MOBO board 1001

- Remove the Front Panel assembly
- Remove the connections
- Remove 6 screws 246, 254 (board => backplate)

⇒ remove 4 screws 270 (board → frame)

⇒ demount the board

DVDR BASIC ENGINE 1004

⇒ Remove Front Panel assembly

⇒ Remove all the connections

⇒ Remove 6 screws 260 and 269 (assembly -> frame 224)

⇒ Remove 2 screws 262 (assembly -> support bracket 256)

⇒ Uncatch dust cover assembly 147 + 148 from DVDR Basic Engine

Manual opening of tray and removal of tray front 134 + 138

In case the loader is defective and cannot be opened electrically, you can open the tray as follows:

⇒ It is possible to unlock the tray by means of a screwdriver via a slot in the front and frame at the underside.
Push the white pin of the slider at the underside of the basic engine to the left (seen from the front)

⇒ Open the unlocked tray.

TR 06003_003
300504

Figure 4-11

5. Diagnostic Software

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

1. End user/Dealer script interface
2. Command Interface

5.1 End User/Dealer Script Interface

5.1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

5.1.2 Structure

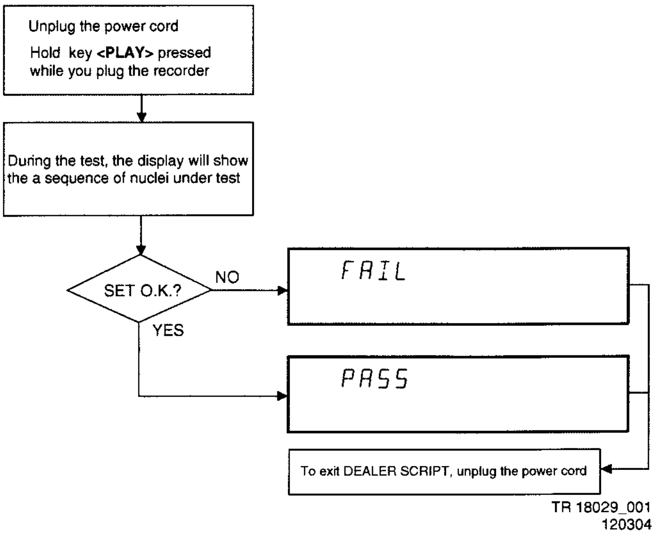

Unplug the power cord
Hold key **<PLAY>** pressed while you plug the recorder
During the test, the display will show the a sequence of nuclei under test
SET O.K.?
NO
YES
FAIL
PASS
To exit DEALER SCRIPT, unplug the power cord
TR 18029_001
120304

Figure 5-1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder.

5.1.3 Contents

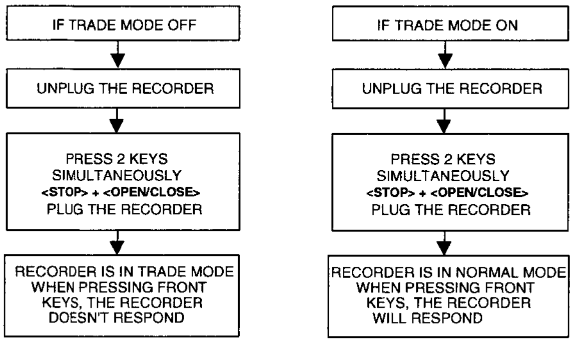
Included tests:	1.DS_ANAB_COMMUNICATIONECHO_NUC 2.DS_DCB_COMMUNICATIONECHO_NUC 3. DS_BROM_COMMUNICATION_NUC 4. DS_SYS_SETTINGSDISPLAY_NUC 5. DS_CHR_DEVTYPEGET_NUC 6. DS_CHR_INT_PIC_NUC 7. DS_CHR_DMA_NUC 8. DS_BROM_WRITEREAD_NUC 9. DS_NVRAM_COMMUNICATION_NUC 10. DS_NVRAM_WRITEREAD_NUC 11. DS_SDRAM_WRITEREADFAST_NUC 12. DS_FLASH_WRITEREAD_NUC 13.DS_FLASH_CHECKSUMPROGRAM_NUC 14.DS_SYS_HARDWAREVERSIONGET_NUC 15. DS_VIP_DEVTYPEGET_NUC 16. DS_VIP_COMMUNICATION_NUC 17. DS_DVIO_LINKDEVTYPEGET_NUC 18. DS_DVIO_PHYDEVTYPEGET_NUC 19. DS_DVIO_LINKCOMMUNICATION_NUC 20. DS_DVIO_PHYCOMMUNICATION_NUC 21.DS_PSCAN_COMMUNICATIONDENC_NUC 22.DS_PSCAN_COMMUNICATIONDEINTERLACER_NUC 23. DS_BE_COMMUNICATIONECHO_NUC 24.DS_ANAB_COMMUNICATIONIICNVRAM_NUC 25.DS_ANAB_COMMUNICATIONIICTUNER_NUC 26.DS_ANAB_COMMUNICATIONIICSOUNDPROCESSOR_NUC 27.DS_ANAB_COMMUNICATIONIICAVSELECTOR_NUC 28. DS_ANAB_CHECKSUMPROGRAM_NUC

5.2 Player Script Interface

5.2.1 Trade Mode

TRADE MODE

When the recorder is in Trade Mode, the recorder cannot be controlled by means of the front key buttons, but only by means of the remote control.


IF TRADE MODE OFF
UNPLUG THE RECORDER
PRESS 2 KEYS SIMULTANEOUSLY <STOP> + <OPEN/CLOSE> PLUG THE RECORDER
RECORDER IS IN TRADE MODE WHEN PRESSING FRONT KEYS, THE RECORDER DOESN'T RESPOND
IF TRADE MODE ON
UNPLUG THE RECORDER
PRESS 2 KEYS SIMULTANEOUSLY <STOP> + <OPEN/CLOSE> PLUG THE RECORDER
RECORDER IS IN NORMAL MODE WHEN PRESSING FRONT KEYS, THE RECORDER WILL RESPOND

CL 16532095_071.eps
150801

Figure 5-2

5.2.2 Virgin mode

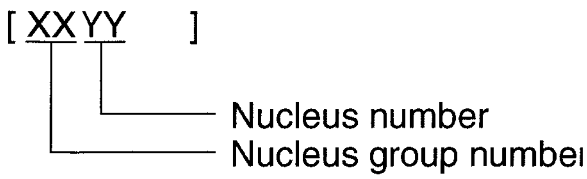
If you want that the recorder starts up in Virgin mode, follow this procedure:

- Unplug the recorder
- plug the recorder again while you keep the STAND BY/ON key pressed
- the set starts up in Virgin mode.

5.3 Menu and Command Mode Interface

5.3.1 Nuclei Numeration

Each nucleus has a unique number of four digits. This number is the input of the command mode.


[XXYY]
Nucleus number
Nucleus group numbe

CL 06532152_012.ep
05120

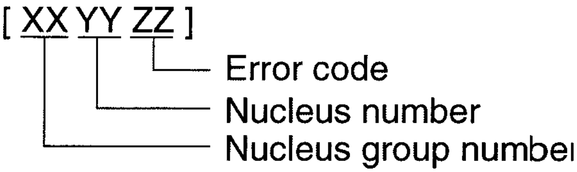
Figure 5-3

Group number	Group name
0	Scripts
1	Codec (e.g. Chrysalis, Leco)
2	Boot EEPROM
3	NVRAM
4	SDRAM
5	Flash
6	Video Input Processor
7	DVIO
8*	Progressive Scan
9	Basic Engine
10*	Display and Control Board
11*	Analogue Board
12	System
13*	Electronic Program Guide Board
14*	PCMCIA
15*	HDMI
16	Analogue Slave Processor
17	Analogue Board EEPROM
18	Video Matrix
19	Audio Matrix
20	Front End
21*	Hard Disk
22*	Digital Terrestrial Tuner Module

* Not applicable for DVDR610, DVDR615 & DVDR616 Range

5.3.2 Error Handling

Each nucleus returns an error code. This code contains six numerals, which means:


[XX YY ZZ]
Error code
Nucleus number
Nucleus group numbe

CL 06532152_013.ep
05120

Figure 5-4

The nucleus group numbers and nucleus numbers are the same as above.

5.3.3 Command Mode Interface

Set-Up Physical Interface Components

Hardware required:

- Service PC
- one free COM port on the Service PC
- special cable to connect DVD recorder to Service PC

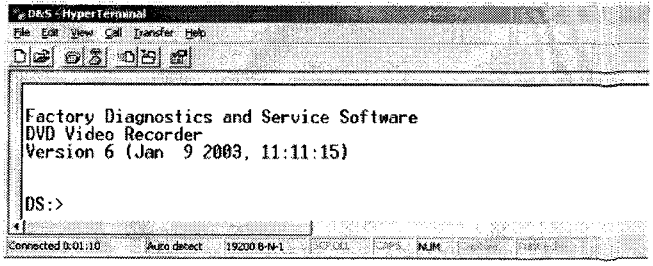
The service PC must have a terminal emulation program (e.g. Hyperterminal) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

Code number of PC interface cable: 3122 785 90017

Activation of Diagnostic Software

1. Pull the mains cord from the recorder and reconnect it again (reboot).
2. The next welcome message will appear on the PC:

Welcome screen D&S program


D&S - HyperTerminal
File Edit View Call Transfer Help
Connected 0:01:10
Auto detect
19200 8-N-1
NUM

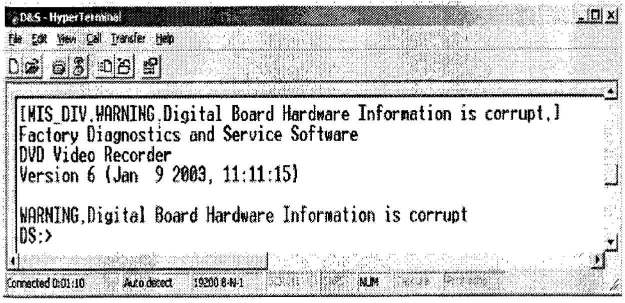
```
Factory Diagnostics and Service Software
DVD Video Recorder
Version 6 (Jan  9 2003, 11:11:15)

DS:>
```

Figure 5-5

Now, the prompt 'DS:>' will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei. If you see above shown screen, continue with paragraph 'Nuclei Codes'.

3. It is possible that the next messages will appear when starting the DVD+RW for the first time

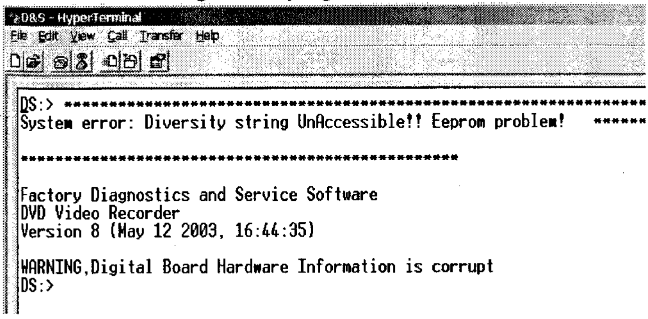
Error messages D&S program


D&S - HyperTerminal
File Edit View Call Transfer Help
Connected 0:01:10 Auto detect 19200 8-N-1 NUM

```
[MIS_DIV.WARNING.Digital Board Hardware Information is corrupt.]
Factory Diagnostics and Service Software
DVD Video Recorder
Version 6 (Jan  9 2003, 11:11:15)

WARNING,Digital Board Hardware Information is corrupt
DS:>
```

Figure 5-6a

Error messages D&S program

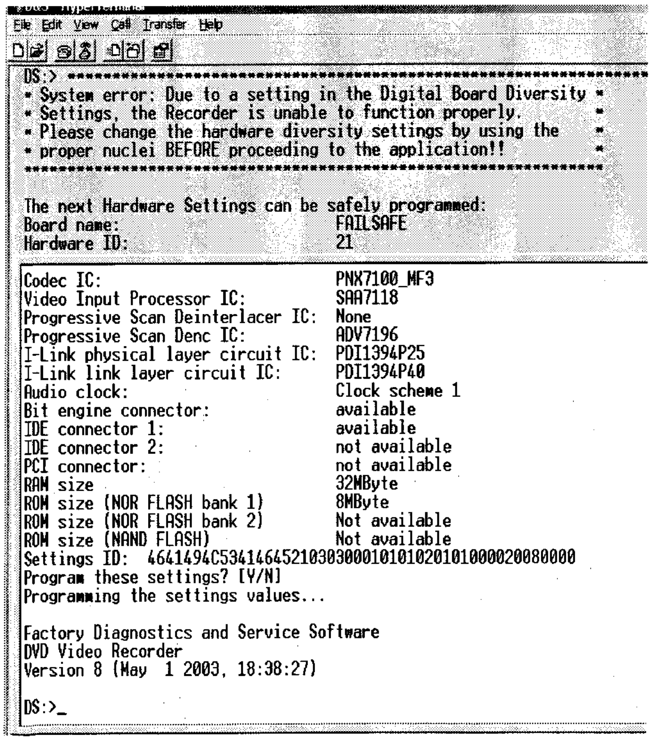

D&S - HyperTerminal
File Edit View Call Transfer Help

```
DS:> ************************************************************
System error: Diversity string UnAccessible!! Eeprom problem!   ******

*********************************************

Factory Diagnostics and Service Software
DVD Video Recorder
Version 8 (May 12 2003, 16:44:35)

WARNING,Digital Board Hardware Information is corrupt
DS:>
```

Figure 5-6b

In these cases, the boot EEPROM of the Digital Board does not contain the required string with the hardware information. To update the Digital Board with the correct string, nucleus 1226 must be executed.

See next section 'Diversity String Input'.
There can also be the next error message.


File Edit View Call Transfer Help

```
DS:> **************************************************************
* System error: Due to a setting in the Digital Board Diversity *
* Settings, the Recorder is unable to function properly.        *
* Please change the hardware diversity settings by using the    *
* proper nuclei BEFORE proceeding to the application!!          *
*****************************************************************

The next Hardware Settings can be safely programmed:
Board name:                          FAILSAFE
Hardware ID:                         21
Codec IC:                            PNX7100_MF3
Video Input Processor IC:            SAA7118
Progressive Scan Deinterlacer IC:    None
Progressive Scan Denc IC:            ADV7196
I-Link physical layer circuit IC:    PDI1394P25
I-Link link layer circuit IC:        PDI1394P40
Audio clock:                         Clock scheme 1
Bit engine connector:                available
IDE connector 1:                     available
IDE connector 2:                     not available
PCI connector:                       not available
RAM size                             32MByte
ROM size (NOR FLASH bank 1)          8MByte
ROM size (NOR FLASH bank 2)          Not available
ROM size (NAND FLASH)                Not available
Settings ID:  4641494C5341464521030300010101020101000020080000
Program these settings? [Y/N]
Programming the settings values...

Factory Diagnostics and Service Software
DVD Video Recorder
Version 8 (May  1 2003, 18:38:27)

DS:>_
```

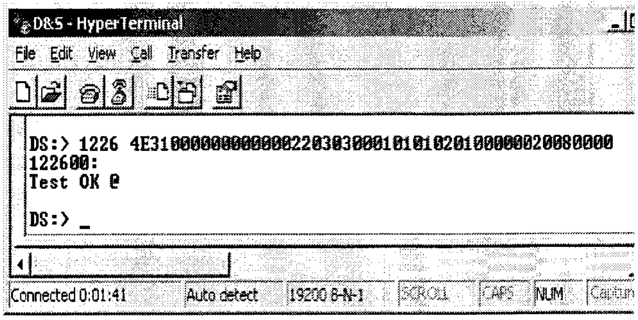
Figure 5-6c

Enter "Y" to program a safe string. With this automatically generated string the board will work in principle but it has to be checked if all board settings were detected correctly.

Diversity String Input

4. Execute nucleus 1226 to enter the string. Please see chapter 8.4 for details

Nucleus 1226 execution with string

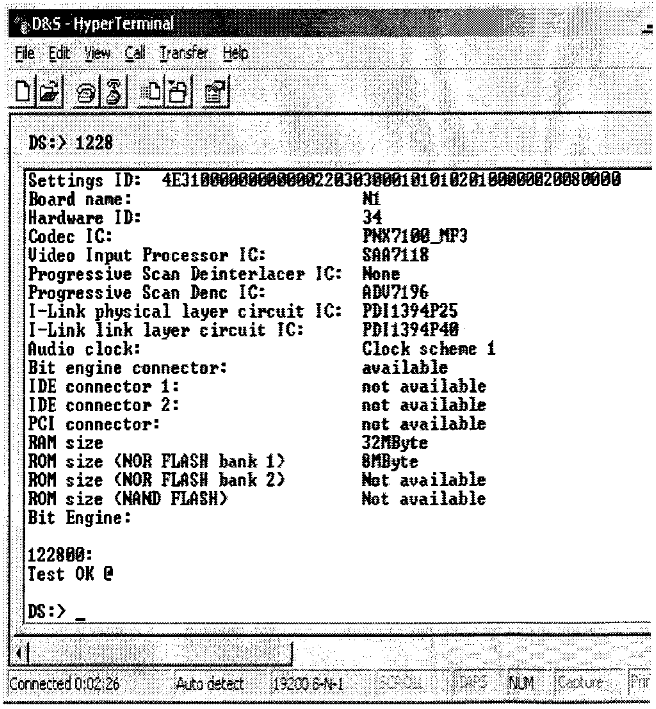

D&S - HyperTerminal
File Edit View Call Transfer Help
Connected 0:01:41 Auto detect 19200 8-N-1 SCROLL CAPS NUM Captur

```
DS:> 1226 4E3100000000000000220303000101010201000000200800000
122600:
Test OK @

DS:> _
```

Figure 5-7

5. To check if the hardware info is filled correctly, you can execute nucleus 1228.

Nucleus 1228 info example


D&S - HyperTerminal
File Edit View Call Transfer Help
Connected 0:02:26 Auto detect 19200 8-N-1 SCROLL CAPS NUM Capture Pri

```
DS:> 1228

Settings ID:  4E3100000000000000220303000101010201000000200800000
Board name:                          N1
Hardware ID:                         34
Codec IC:                            PNX7100_MF3
Video Input Processor IC:            SAA7118
Progressive Scan Deinterlacer IC:    None
Progressive Scan Denc IC:            ADV7196
I-Link physical layer circuit IC:    PDI1394P25
I-Link link layer circuit IC:        PDI1394P40
Audio clock:                         Clock scheme 1
Bit engine connector:                available
IDE connector 1:                     not available
IDE connector 2:                     not available
PCI connector:                       not available
RAM size                             32MByte
ROM size (NOR FLASH bank 1)          8MByte
ROM size (NOR FLASH bank 2)          Not available
ROM size (NAND FLASH)                Not available
Bit Engine:

122800:
Test OK @

DS:> _
```

Figure 5-8

6. Exit the 'Terminal' program.

7. Reboot the DVD recorder to allow the software to start.

Command overview Digital Board

Below you will find an overview of the nuclei, their numbers, and their error codes. This overview is preliminary and subject to modifications.

Note: AV3 in the overview includes also the AV3.5 drive.

CODEC HOST CONTROLLER (CHR)

Nucleus Name	**DS_CHR_DevTypeGet**	
Nucleus Number	100	
Description	Retrieves the device id, the module ids and revisions of the Codec and returns them to the stdout port.	
Technical	- Determine the codec id by means of comparing version ids of the modules.- Read the module-id register of every module and display it to the user.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10000	Getting the information succeeded
	10001	Wrong codec id detected

Example

```
DS:> 100
010000:
Device ID 7100
Codec ID  PNX7100_C
F-BCU  (0x0102) 1.0     INTC   (0x011d) 1.0        PCI-XIO(0x0113) 1.0
SIF    (0x013b) 1.0     EJTAG  (0x0104) 0.1        S-BCU  (0x0102) 1.0
  (0x010a) 1.0          CONFIG (0x013f) 1.1        RESET  (0x0123) 1.0
DEBUG  (0x0116) 0.0     UART0  (0x0107) 0.1        UART1  (0x0107) 0.1
UART2  (0x0107) 0.1     UART3  (0x0107) 0.1        I2C0   (0x0105) 0.1
I2C1   (0x0105) 0.1     GPIO   (0x013c) 1.0        SYNC   (0x013a) 1.0
DISP0  (0xa015) 1.12    DISP1  (0xa00f) 1.1        OSD    (0x0136) 0.1
SPU    (0xa00e) 0.0     MIXER  (0x0137) 1.0        DENC   (0x0138) 1.0
CCIR   (0x0139) 1.0     VDEC   (0x0133) 0.2        PARSER (0xa00d) 0.0
DV     (0xa00c) 0.0     BEI    (0xa00a) 0.1        IDE    (0xa009) 0.1
SGDX   (0xa008) 1.0     BYTE   (0xa00b) 0.1        OUTPUT (0xa003) 1.0
ACOMP  (0xa000) 1.0     VFE    (0xa001) 0.1        VCOMP  (0xa002) 1.0
SCR    (0x0000) 0.0     SIFF   (0xa011) 0.1        WMD    (0xa010) 0.0
AUDIO0 (0xa015) 1.12    AUDIO1 (0xa00f) 1.1        PSCAN  (0xa018) 0.1

Test OK @
```

Nucleus Name	**DS_CHR_TestImageOn**
Nucleus Number	101
Description	Generates a test-image of a selected video standard on selected video output on the digital board. When no input is given, the default values will be used (see user input description below). Make sure to use the proper nuclei to route the video signal on the analogue board to get the videosignal to the proper output.
Technical	-Validate the user input. -Initialise the SYNC module. -Initialise the DISPLAY module. -Initialise the MIXER module. -Initialise the DENC module. -Set the selected video standard. -Generate the selected test image in memory. -Start the DISPLAY module. -Start the MIXER module. -Start the DENC module according to the selected test image id.
Execution Time	6 seconds.

Nucleus Name	**DS_CHR_TestImageOn**	
User Input	The user has to decide which test image, video standard and video output must be used: Test image id: 0 VERTICAL_COLOURBAR (default) 1 HORIZONTAL_COLOURBAR 2 WHITE 3 YELLOW 4 CYAN 5 GREEN 6 MAGENTA 7 RED 8 BLUE 9 BLACK 10GRAY 11TEST_IMAGE_FOR_PROGRESSIVE_SCAN Video standard: PAL (default) NTSC Video output ALL CVBS and YC and RGB (default) CVBS YC RGB YUV PSCAN progressive scan	
Error	Number	Description
	10100	Generating the test image succeeded.
	10101	Invalid input was provided.
	10102	The Codec SYNC-module cannot be initialised.
	10103	The Codec MIXER-module cannot be initialised.
	10104	The Codec VPP-module cannot be initialised.
	10105	The Codec DENC-module cannot be initialised.
	10106	The digital board hardware information is corrupt
Example	DS:> 101 010100: Test OK @ DS:> 101 0 pal cvbs 010100: Test OK @ DS:> 101 4 ntsc yc 010100: Test OK @	

Nucleus Name	**DS_CHR_TestImageOff**	
Nucleus Number	102	
Description	Switches the test-image off.	
Technical	- Stop the DENC module.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10200	Stopping the test image generation succeeded
	10201	The Codec DENC-module failed.
Example	DS:> 102 010200: Test OK @	

Nucleus Name	**DS_CHR_SineOn**
Nucleus Number	103
Description	Generate an audio sine signal on the audio output of the digital board. Note: Left channel 6kHz, right channel 12 kHz sine. Make sure to route the signal first.

Technical	- De-mute the analogue board - Set fifo parameters for audio - Set the volume - Set the I2S outputs and configuration paths - Set the decoder mode - Configure the audio decoder - Put the AC3 audio in the fifo - Send ‘prepare’ command to the audio decoder - Send ‘play’ command to the audio decoder	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	10300	The sine signal was successfully generated
	10301	The analogue board could not be de-muted
	10302	The audio decoder did not initialise
	10303	The dsp2 of the audio decoder did not configure
	10304	The dsp1 of the audio decoder did not configure
	10305	There was a delay-error before starting
	10306	Wrong input was given to the decoder function
	10307	Wrong input was given to the decoder function @@@@@
	10308	The audio decoder did not get into the 'prepared' state
Example	DS:> 103 010300: Test OK @	

Nucleus Name	**DS_CHR_SineOff**	
Nucleus Number	104	
Description	Stop generating the audio sine signal	
Technical	- Reset the audio block of the Codec	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10400	Switching off the audio sine signal succeeded
	10401	Failed to reset the audio decoder
Example	DS:> 104 010400: Test OK @	

Nucleus Name	**DS_CHR_SineBurst**	
Nucleus Number	105	
Description	Generate an audio sine signal on the audio output of the digital board for 4 seconds. Note: Left channel 6kHz, right channel 12 kHz sine with some known hick-ups	
Technical	- Call the DS_CHR_SineOn nucleus - Delay for 4 seconds - Call the DS_CHR_SineOff nucleus	
Execution Time	4 seconds	
User Input	None	
Error	Number	Description
	10500	The sine signal burst was successfully generated
	10501	The delay did not succeed during the burst
	10502	The audio sine could not be generated
Example	DS:> 105 010500: Test OK @	

Nucleus Name	**DS_CHR_MuteOn**	
Nucleus Number	106	
Description	Mute the audio outputs of the digital board	
Technical	- Send the 'Mute' command to the audio decoder	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10600	Muting the audio succeeded

Example	DS:> 106 010600: Test OK @	

Nucleus Name	**DS_CHR_MuteOff**	
Nucleus Number	107	
Description	De-mute the audio outputs of the digital board	
Technical	- Send the 'DeMute' command to the audio decoder	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10700	De-muting the audio succeeded
Example	DS:> 107 010700: Test OK @	

Nucleus Name	**DS_CHR_DvLedOn**	
Nucleus Number	108	
Description	Check the connection to the DV-LED on the digital board by switching it on	
Technical	- Write to the PIO pin to light the DV LED	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10800	Switching the DV-LED on succeeded
	10801	Switching the DV-LED on failed
Example	DS:> 108 010800: Test OK @	

Nucleus Name	**DS_CHR_DvLedOff**	
Nucleus Number	109	
Description	Switch off the DV-LED on the digital board	
Technical	- Write to the PIO pin to switch off the DV LED	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	10900	Switching the DV-LED off succeeded
	10901	Switching the DV-LED off failed
Example	DS:> 109 010900: Test OK @	

Nucleus Name	**DS_CHR_MacroVisionOn**	
Nucleus Number	110	
Description	Turn on MacroVision.	
Technical	- Set some registers of the DENC module in the Codec.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	11000	Turning on MacroVision succeeded
	11001	Turning on MacroVision failed
Example	DS:> 110 011000: Test OK @	

Nucleus Name	**DS_CHR_MacroVisionOff**	
Nucleus Number	111	
Description	Turn off MacroVision.	
Technical	- Set some registers of the DENC module in the Codec.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	11100	Turning off MacroVision succeeded

	11101	Turning off MacroVision failed
Example	DS:> 111 011100: Test OK @	

Nucleus Name	**DS_CHR_Peek**	
Nucleus Number	112	
Description	Peek a value on a specified address	
Technical	- Check the user input - Read out the address specified - Check whether the address to be read is aligned on 4 bytes	
Execution Time	Less than 1 second.	
User Input	The address to peek on	
Error	Number	Description
	11200	Peeking on the specified address succeeded
	11201	Peeking on the specified address failed, wrong user input
	11202	Peeking on the specified address failed due to misalignment
Example	DS:> 112 0xa0700000 011200: Value read = 0x000001BD Test OK @	

Nucleus Name	**DS_CHR_Poke**	
Nucleus Number	113	
Description	Poke a value on a specified address	
Technical	- Check the user input - Change the value on the address specified - Check whether the address to be modified is aligned on 4 bytes	
Execution Time	Less than 1 second.	
User Input	The address to poke and the value: <address><value>	
Error	Number	Description
	11300	Poking the specified address succeeded
	11301	Poking the specified address failed, wrong user input
	11302	Poking the specified address failed due to misalignment
Example	DS:> 113 0xa0700000 0xaabbccdd 011300: Test OK @	

Nucleus Name	**DS_CHR_INT_PICInterrupts**	
Nucleus Number	114	
Description	Test all interrupts of the priority interrupt controller	
Technical	- Install interrupt handlers - Generate interrupts - Test whether all interrupts were received	
Execution Time	Less than 1 second.	
User Input	-	
Error	Number	Description
	11400	Testing all the PIC interrupts succeeded
	11401	Testing all the PIC interrupts failed
Example	DS:> 114 011400: Test OK @	

Nucleus Name	**DS_CHR_DMA_TestDMA**	
Nucleus Number	115	
Description	Test the memory to memory DMA transfer	
Technical	- Create a block with known data in memory - Copy this block to the consecutive area using 3 different DMAs - Check whether all DMAs transferred the data properly	
Execution Time	Less than 2 seconds.	
User Input	-	
Error	Number	Description
	11500	The testing of the DMAs succeeded
	11501	The initialisation of the DMAs failed for one or more DMA
	11502	One or more DMAs failed the test

Example	DS:> 115 011500: Test OK @	

Boot EEPROM (BROM)

Nucleus Name	**DS_BROM_Communication**	
Nucleus Number	200	
Description	Check the communication between the IIC controller of the Chrysalis and the boot EEPROM	
Technical	- Initialise IIC - Read something from the EEPROM	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	20000	The data is properly read so the communication is OK
	20001	The IIC bus was not accessible
	20002	There was a timeout reading the device
	20003	The IIC acknowledge was not received
	20004	An IIC-bus error occurred
	20005	The IIC bus initialisation failed
	20006	An unexpected IIC error occurred
Example	DS:> 200 020000: Test OK @	

Nucleus Name	**DS_BROM_WriteRead**	
Nucleus Number	201	
Description	Check whether the Boot EEPROM can be written to and read from	
Technical	- Initialise IIC - Write something to the EEPROM - Read from the same location and check whether it is the same as written	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	20100	The write-read test succeeded
	20101	The write-read test failed
	20102	An IIC-bus error occurred
	20103	There was a timeout reading the device
	20104	The IIC bus was not accessible
	20105	The IIC acknowledge was not received
	20106	Got unknown IIC bus error
	20107	The IIC bus initialisation failed
Example	DS:> 201 020100: Test OK @	

NVRAM

Nucleus Name	**DS_NVRAM_Communication**	
Nucleus Number	300	
Description	Check the communication between the IIC controller of the Codec and the EEPROM	
Technical	- Initialise IIC - Read from a location in NVRAM	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	30000	Something is properly read so the communication is OK
	30001	The IIC bus was not accessible
	30002	There was a timeout reading the device
	30003	The IIC acknowledge was not received
	30004	The communication with the device failed
	30005	The IIC bus initialisation failed
	30006	@@@@@@

Example	DS:> 300 030000: Test OK @	

Nucleus Name	**DS_NVRAM_WriteRead**	
Nucleus Number	301	
Description	Check whether the EEPROM can be written to and read from	
Technical	- Initialise IIC - Backup data from location to modify - Write to location and read it back again - Write back the backed up data to the location to leave the NVRAM as found	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	30100	The write-read test succeeded
	30101	The IIC bus could not be initialised
	30102	There was an NVRAM IO error
	30103	The value could not be read back from the NVRAM
Example	DS:> 301 030100: Test OK @	

Nucleus Name	**DS_NVRAM_Clear**	
Nucleus Number	302	
Description	Make the EEPROM empty, containing all zeroes.	
Technical	- Initialise IIC - Create a memory block filled with zeroes - Write this block to the NVRAM	
Execution Time	16 seconds	
User Input	None	
Error	Number	Description
	30200	The clearing of the NVRAM succeeded
	30201	There was an IIC error
	30202	Clearing the NVRAM failed
Example	DS:> 302 030200: Test OK @	

Nucleus Name	**DS_NVRAM_Modify**	
Nucleus Number	303	
Description	Modifies one or more locations in NVRAM and updates the checksum of the section modified	
Technical	- Initialise IIC - Decode user input - Modify the NVRAM as indicated - Validate the NVRAM by calculating the checksum and storing it	
Execution Time	Less than 1 second	
User Input	1. The location that must be modified i.e. "ALL" "BOOT" "DIAGNOSTICS" "DOWNLOAD" "CONFIG" "RECORDER" or no string if an offset from the base address of the NVRAM is required 2. The offset and data which to put on the selected location <offset> <length> <data>	
Error	Number	Description
	30300	Modifying the NVRAM contents succeeded
	30301	Unable to initialise NVM
	30302	Modifying the NVRAM contents failed
	30303	length out of range
	30304	unable to decode length
	30305	offset out of range
	30306	unable to decode offset
	30307	unknown location specified
	30308	no location is specified
	30309	number of values incorrect
	30310	There was an IIC error

Example	DS:> 303 DIAGNOSTICS 5 1 0x5a 030300: Section is modified successfully Test OK @

Nucleus Name	**DS_NVRAM_Read**	
Nucleus Number	304	
Description	Read out one or more locations in the NVRAM	
Technical	- Initialise IIC - Decode user input - Read from the NVRAM and return this info to the user	
Execution Time	Less than 1 second	
User Input	1. The location which must be read i.e. "ALL" "BOOT" "DIAGNOSTICS" "DOWN LOAD" "CONFIG" "RECORDER" or no string if an offset from the base address of the NVRAM is required 2. The offset and number of bytes to read <offset> <length>	
Error	Number	Description
	30400	Value read
	30401	Unable to initialise NVM
	30402	Reading the NVRAM contents failed
	30403	length out of range
	30404	unable to decode length
	30405	offset out of range
	30406	unable to decode offset
	30407	unknown location specified
	30408	no location is specified
Example	304 DIAGNOSTICS 0 6 030400: Value read = 0x00 0x00 0x00 0x00 0x00 0x5A Test OK @	

SDRAM

Nucleus Name	**DS_SDRAM_WriteRead**	
Nucleus Number	400	
Description	Check all data lines, address lines and memory locations of the SDRAM	
Technical	- Test the databus - Test the address bus - Test the integrity of the device itself (memory locations)	
Execution Time	11 seconds for 32 Mb 23 seconds for 64 Mb	
User Input	None	
Error	Number	Description
	40000	The write-read test succeeded
	40001	The data bus contains an error
	40002	The address bus contains an error
	40003	The SDRAM itself contains an error
Example	DS:> 400 040000: Test OK @	

Nucleus Name	**DS_SDRAM_WriteReadFast**	
Nucleus Number	401	
Description	Check all data lines and address lines of the SDRAM	
Technical	- Test the databus - Test the addressbus	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	40100	The write-read test succeeded
	40101	The data bus contains an error
	40102	The address bus contains an error
Example	DS:> 401 040100: Test OK @	

Nucleus Name	**DS_SDRAM_Write**	
Nucleus Number	402	
Description	Write to a specific memory address	
Technical	- Decode the user input and check its ranges and alignment on 4 bytes - Write the data to the SDRAM	
Execution Time	Less than 1 second	
User Input	1. The location that must be modified (SDRAM starts at address 0xA0000000) 2. The value to put on the selected location	
Error	Number	Description
	40200	Writing to the SDRAM succeeded
	40201	Writing to the SDRAM failed; Wrong user input
	40202	Address is not dividable by 4
Example	DS:> 402 0xa1000010 0xad112222 040200: Test OK @	

Nucleus Name	**DS_SDRAM_Read**	
Nucleus Number	403	
Description	Read from a specific memory address	
Technical	- Decode the user input and check the ranges - Read from the SDRAM and return this info to the user	
Execution Time	Less than 1 second	
User Input	The location from which the data must be read (SDRAM starts at address 0xA0000000)	
Error	Number	Description
	40300	Reading from the SDRAM succeeded
	40301	Reading from the SDRAM failed; Wrong user input
	40302	Address is not dividable by 4
Example	DS:> 403 0xa1000010 040300: Value read = 0xAD112222 Test OK @	

FLASH

Nucleus Name	**DS_FLASH_DevTypeGet**	
Nucleus Number	500	
Description	Get the device (revision) type information of the FLASH IC. (type, manufacturer, device ID and size)	
Technical	- Set the timing for the flash writing - Write a command sequence to determine device type information - Return the information to the user	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	50000	Getting the information from the FLASH succeeded
	50001	Getting the information from the FLASH failed
Example	DS:> 500 050000: Found FLASH memory: NOR AMD 29DL640G 8MB,NOR AMD 29DL640G 8MB Test OK @	

Nucleus Name	**DS_FLASH_WriteRead**	
Nucleus Number	501	
Description	Check whether the FLASH can be written to and read from	
Technical	- Find the test segment in flash - Read the data into SDRAM - Modify the data - Write this data from SDRAM to FLASH and verify it by reading back again	
Execution Time	Less than 1 seconds.	
User Input	None	
Error	Number	Description
	50100	The FLASH write-read test succeeded
	50101	The test segment could not be found
	50102	All bits is the TEST region are filled with 0 (region exhausted)

	50103	The WriteRead test failed
	50104	The Write Failed
Example	DS:> 501 050100: Test OK @	

Nucleus Name	**DS_FLASH_Read**	
Nucleus Number	502	
Description	Read from a specific memory address in FLASH	
Technical	- Decode the user input and check the ranges and whether the address is aligned on 4 bytes - Read the data and return this to the user	
Execution Time	Less than 1 seconds.	
User Input	The location from which data must be read (FLASH starts at address 0xB8000000)	
Error	Number	Description
	50200	Reading the FLASH succeeded
	50201	Reading the FLASH failed; Wrong user input
	50202	Address is not dividable by 4
Example	DS:> 502 0xb8000000 050200: Value read = 0x3C08A000 Test OK @	

Nucleus Name	**DS_FLASH_ChecksumProgram**	
Nucleus Number	503	
Description	Check the checksum of the application partitions by recalculating and comparing partition checksums	
Technical	- Determine the number of segments - Find the application in each segment and determine its checksum - Check whether the checksums stored match the newly calculated	
Execution Time	6 seconds	
User Input	None	
Error	Number	Description
	50300	The checksum is valid, the test succeeded
	50301	The checksum is invalid
Example	DS:> 503 050300: BootCode checksum is: 0xBABE5B6F, which is correct Diagnostics checksum is : 0xBABEBAFF, which is correct Download checksum is: 0xBABEEDBF, which is correct Application checksum is : 0xBABE8EEC, which is correct Test OK @	

Nucleus Name	**DS_FLASH_CalculateChecksum**	
Nucleus Number	504	
Description	Calculate the checksum over all memory addresses. Used to check entire FLASH contents	
Technical	- Run the checksum calculation algorithm all flash memory addresses	
Execution Time	6 seconds	
User Input	None	
Error	Number	Description
	50400	Calculating the checksum over all addresses succeeded
Example	DS:> 504 050400: The Checksum = 0xBABE30A4 Test OK @	

Nucleus Name	**DS_FLASH_CalculateChecksumFast**	
Nucleus Number	505	
Description	Calculate a checksum over a selected number of address locations	
Technical	- Run the checksum calculation algorithm on a selected number of flash memory addresses	
Execution Time	6 seconds	
User Input	None	
Error	Number	Description
	50500	Calculating the checksum over selected addresses succeeded

Example	DS:> 505 050500: The Checksum = 0xBABEB064 Test OK @

Video Input Processor (VIP)

Nucleus Name	**DS_VIP_DevTypeGet**	
Nucleus Number	600	
Description	Get the device (revision) type information of the VIP IC	
Technical	- Initialise IIC - Read out the device (revision) type information of the VIP IC	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	60000	Getting the information from the VIP succeeded
	60001	The IIC bus initialisation failed
	60002	The was an error getting the information from the VIP
	60003	Type not according to type stored in HW diversity string
Example	DS:> 600 060000: Found SAA7118 Test OK @	

Nucleus Name	**DS_VIP_Communication**	
Nucleus Number	601	
Description	Check the communication between the IIC controller of the Codec and the VIP IC	
Technical	- Initialise IIC - Read data from a location in the VIP	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	60100	Communicating with the VIP succeeded
	60101	The IIC bus was not accessible
	60102	There was a timeout reading the device
	60103	The IIC acknowledge was not received
	60104	The communication with the device failed
	60105	The IIC bus initialisation failed
Example	DS:> 601 060100: Test OK @	

Nucleus Name	**DS_VIP_ClockOutputOn**	
Nucleus Number	602	
Description	Switch the clock output on	
Technical	- Initialise IIC - Set the clock output through IIC	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	60200	Switching the clock output on succeeded
	60201	Switching the clock output on failed
Example	DS:> 602 060200: Test OK @	

Nucleus Name	**DS_VIP_ClockOutputOff**	
Nucleus Number	603	
Description	Switch the clock output off	
Technical	- Initialise IIC - Reset the clock output through IIC	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	60300	Switching the clock output off succeeded
	60301	Switching the clock output off failed

Example	DS:> 603 060300: Test OK @	

Nucleus Name	**DS_VIP_SelectInput**	
Nucleus Number	604	
Description	Select an input video path to be switched to the analogue output pin (AOUT) of the VIP	
Technical	- Check the user input - Initialise IIC - Read out the VIP id - Write the set of registers required for the input specified	
Execution Time	Less than 1 second	
User Input	The input to select, see table below.	
Error	Number	Description
	60400	Selecting the input of the VIP succeeded
	60401	The user provided wrong input
	60402	The VIP was not accessible
	60402	An unsupported VIP was found
Example	DS:> 604 1 060400: Test OK @	

Table 5-1 *Available channels for input of the 7118 and their description*

Channel number	Description
1	CVBS_Y_IN_A
2	CVBS_OUT_B
3	CVBS_Y_IN_B
4	CVBS_Y_IN_C
6	C_IN
8	G_IN
9	Y_IN
13	B_IN
14	U_IN
18	R_IN
19	V_IN

Table 5-2 *Available channels for input of the 7115 and their description*

Channel number	Description
1	CVBS_Y_IN_B
2	CVBS_OUT_B_VIP
4	C_IN_VIP
7	CVBS_Y_IN_B

Digital Video Input Output (DVIO)

Nucleus Name	**DS_DVIO_LinkDevTypeGet**	
Nucleus Number	700	
Description	Get the device (revision) type information of the 1394 Link layer IC	
Technical	- Initialise the PIO pins on the Codec - Read out the ID register	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	70000	Getting the information from the link layer IC succeeded
	70001	Getting the information from the link layer IC failed
	70002	Type not according to type stored in HW diversity string
Example	DS:> 700 070000: Device type of the link layer IC: ffc00301 Test OK @	

Nucleus Name	**DS_DVIO_PhyDevTypeGet**
Nucleus Number	701

Description	Get the device (revision) type information of the 1394 Physical layer IC
Technical	- Initialise the PIO pins of the Codec-Write the PHY - access register in the Link chip to indicate phy read access - Wait until the link chip has obtained the value from the phy-chip - Read this out and filter the data to be returned to the user
Execution Time	Less than 1 second
User Input	None
Example	DS:> 701 070100: Physical layer IC: VendorID: 0x006037, ProductID: 0x412801 Test OK @

Nucleus Name	**DS_DVIO_LinkCommunication**	
Nucleus Number	702	
Description	Check the accessibility of the 1394 Link layer IC by writing to and reading from a specific address	
Technical	- Initialise the PIO pins of the chrysalis - Write a pattern to the CYCTM register of the link chip - Read back and verify the pattern	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	70200	Communicating with the link layer IC succeeded
	70201	Communicating with the link layer IC failed
	70202	Result of nucleus not according to HW diversity string
Example	DS:> 702 070200: Test OK @	

Nucleus Name	**DS_DVIO_PhyCommunication**	
Nucleus Number	703	
Description	Check the accessibility of the 1394 Physical layer IC by writing to and reading from a specific address	
Technical	- Initialise the PIO pins of the Codec - Initialise IIC - Write the data to be written to the phy-chip to the link chip first - Wait until the link chip indicates that the data has been written to the PHY - Write the PHY-access register in the Link chip to indicate PHY read access - Wait until the link chip has obtained the value from the PHY-chip - Test whether the value read back equals the one previously written	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	70300	Communicating with the physical layer IC succeeded
	70301	The physical layer IC was not accessible
	70302	Communicating with the physical layer IC failed
	70303	Result of nucleus not according to HW diversity string
Example	DS:> 703 070300: Test OK @	

Nucleus Name	**DS_DVIO_Routing**
Nucleus Number	704
Description	Route a DV stream containing an audio and video signal through the physical and link layer ICs to the Codec. This test works for both NTSC and PAL.
Technical	- Initialise the DMA to transfer 5 frames PAL/NTSC - Initialise the DV demultiplexer - Initialise the 1394 interface and start reception of the DV stream - Check whether the stream was copied to memory properly by the byte input interface (port to memory type DMA)
Execution Time	6-10 seconds (6 when OK, 10 when no stream or error)
User Input	None

Error	Number	Description
	70400	Routing the signals succeeded
	70401	The 1394 link chip could not be initialised properly
	70402	There was a syntax error in the DV stream
	70403	DMA could not copy DV stream to memory. Stream connected?
	70404	DMA not working properly
Example	DS:> 704 070400: Test OK @	

Nucleus Name	**DS_DVIO_DetectNode**	
Nucleus Number	705	
Description	Check whether a DV node can be detected by the hardware. This test works for both NTSC and PAL.	
Technical	- Initialise the 1394 interface - Detect whether a node is in range	
Execution Time	3 or 5 seconds (3 when OK, 5 when no stream or error)	
User Input	None	
Error	Number	Description
	70500	The node was detected OK
	70501	The 1394 link chip could not be initialised properly
	70502	Unable to write to 1394 PHY chip
	70503	Unable to read from 1394 PHY chip
	70504	No node was detected
Example	DS:> 705 070500: Test OK @	

Nucleus Name	**DS_DVIO_DetectStream**	
Nucleus Number	706	
Description	Check whether a DV stream can be detected by the hardware. This test works for both NTSC and PAL.	
Technical	- Initialise the 1394 interface - Start receiving the stream - Detect whether the stream is OK	
Execution Time	3 or 5 seconds (3 when OK, 5 when no stream or error)	
User Input	None	
Error	Number	Description
	70600	The stream was detected
	70601	The 1394 link chip could not be initialised properly
	70602	No stream detected
Example	DS:> 706 070600: Test OK @	

Progressive Scan (PSCAN)

Nucleus Name	**DS_PSCAN_DencDevTypeGet**	
Nucleus Number	800	
Description	Retrieve the device type information from the progressive scan DENC IC	
Technical	-	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	80000	Retrieving the device type information succeeded
	80001	The IIC bus was not accessible
	80002	There was a timeout reading the device
	80003	The IIC acknowledge was not received
	80004	Communicating with the progressive scan DENC-IC failed
	80005	The initialisation of the IIC bus failed
Example	DS:> 800 080000: Device Type xxxx t.b.d. Test OK @	

Nucleus Name	**DS_PSCAN_CommunicationDenc**	
Nucleus Number	801	
Description	Check the communication between the IIC controller of the chrysalis and the progressive scan DENC-IC	
Technical	- Initialise IIC - Write data to a register of the DENC through IIC	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	80100	Communicating with the progressive scan DENC-IC succeeded
	80101	The IIC bus was not accessible
	80102	There was a timeout reading the device
	80103	The IIC acknowledge was not received
	80104	Communicating with the progressive scan DENC-IC failed
	80105	The initialisation of the IIC bus failed
	80106	The read data is not the same as the written data
	80107	No chip was expected
Example	DS:> 801 080100: Test OK @	

Nucleus Name	**DS_PSCAN_TestImageOn**	
Nucleus Number	802	
Description	Generate the test images that are present on the progressive scan IC.	
Technical	- Determine whether the user wanted a HATCH or a FRAME image pattern - Initialise the PIO pins of the Codec - Initialise IIC - Reset the DENC - Enable the 27Mhz clock - Send all settings for the pattern to the DENC through IIC	
Execution Time	Less than 1 second	
User Input	In case of ADV7196: When no input is given "HATCH" is the default -"HATCH" -"FRAME" Remark: "HATCH" is a crosshatch test pattern (horizontal and vertical white lines are displayed against a black background) "FRAME" is a uniform coloured frame/field test pattern (default white). In case of FLI2300: Nothing.	
Error	Number	Description
	80200	The generation of the test image succeeded
	80201	Unable to initialise PSCAN IC
	80202	Unable to reset DENC
	80203	Unable to generate image
	80204	No chip was expected
Example	DS:> 802 HATCH 080200: Test OK @	

Nucleus Name	**DS_PSCAN_TestImageOff**	
Nucleus Number	803	
Description	Switch off the generated test image	
Technical	- Initialise IIC - Send the default DENC settings to the DENC through IIC	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	80300	Turning off the test image succeeded
	80301	Unable to initialise PSCAN IC
	80302	IIC Error during writing PSCAN IC
	80303	No chip was expected

Example	DS:> 803 080300: Test OK @	

Nucleus Name	**DS_PSCAN_TestImageColourSettingsSet**	
Nucleus Number	804	
Description	Set the colour of the hatch- or the frame- field to a different value than the default white	
Technical	- Determine which colour must be set. - Initialise IIC. - Enable 27 Mhz PSCAN Clock. - Send all settings to the DENC through IIC.	
Execution Time	Less than 1 second.	
User Input	A colour string of one of the next non-case sensitive strings (WHITE, BLACK, RED, GREEN, BLUE, YELLOW, CYAN, MAGENTA) or Y Cr Cb (hexa-) decimal values.	
Error	Number	Description
	80400	Setting the new colour-settings succeeded
	80401	The user provided wrong input
	80402	Unable to initialise pscan ic
	80403	Unable to set colour
	80404	No chip was expected
Example	DS:> 804 yellow 080400: Test OK @ DS:> 804 0x6a 0xde 0xca 080400: Test OK @	

Nucleus Name	**DS_PSCAN_TestImageColourSettingsGet**	
Nucleus Number	805	
Description	Get the colour settings of the hatch- or the frame- field.	
Technical	- Initialise IIC. - Read the colour settings from the DENC through IIC.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	80500	Getting the colour-settings succeeded
	80501	The progressive scan DENC-IC was not accessible through IIC
	80502	Unable to get colour
	80503	No chip was expected
Example	DS:> 805 080500: Colour Y Cr Cb values: 0xD2 0x92 0x10 Test OK @	

Nucleus Name	**DS_PSCAN_Routing**	
Nucleus Number	806	
Description	Route a video signal from the codec host processor through the progressive scan ICs to the progressive scan output of the set. **Note:** To route the progressive scan to the output of the set, first call the nucleus to do the video routing on the analogue (part of the) board.	
Technical	- Initialise the PIO pins of the Codec - Initialise IIC - Reset the DENC - Enable the 27Mhz clock - Send all settings to the DENC through IIC.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	80600	Routing path is created successfully.
	80601	Unable to initialise the Codec.
	80602	Unable to access DENC
	80603	Unable to access de-interlacer.
	80604	Wrong chips were expected.
Example	DS:> 806 080600: Test OK @	

Nucleus Name	**DS_PSCAN_DevTypeGetDeinterlacer**	
Nucleus Number	807	
Description	Get the device (revision) type information of the progressive scan de-interlacer.	
Technical	- Initialise the dei-nterlacer. - Read the version register of the de-interlacer.	
Execution Time	1 second	
User Input	None	
Error	Number	Description
	80700	Everything went well.
	80701	The communication with the device failed
	80702	No chip was expected
Example	DS:> 807 080700: Chip name : 2300 Chip version : 1 Test OK @	

Nucleus Name	**DS_PSCAN_CommunicationDeinterlacer**	
Nucleus Number	808	
Description	Check the communication between the IIC controller of the Codec and the progressive scan De-interlacer-IC	
Technical	- Initialise IIC - Set the video source synchronisation source to the Codec - Write data to the DENC through IIC	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	80800	Communicating with the progressive scan De-interlacer-IC succeeded
	80801	The IIC bus was not accessible
	80802	There was a timeout reading the device
	80803	The communication with the device failed (no ACK)
	80804	Communicating with the progressive scan De-interlacer-IC failed
	80805	The initialisation of the IIC bus failed
	80806	The data read back is not the same as the data written
	80807	No chip was expected
Example	DS:> 808 080800: Test OK @	

Basic Engine (BE)

Nucleus Name	**DS_BE_CommunicationEcho**	
Nucleus Number	900	
Description	Check the communication between the digital board and the basic engine by issuing an *echo* command	
Technical	- Send the ECHO command - Check if the BE returned the string 0x00 0xAA 0x55	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	90000	Communicating with the BE over the S2B interface succeeded
	90001	There was a time-out while communicating
	90002	The Basic Engine returned an unexpected result
	90003	The Basic Engine returned an error code
	90004	No acknowledge received from BE
	90005	Communicating with the Basic Engine failed
	90006	Echo check failed, no echo received
	90007	Echo check failed, received wrong pattern
Example	DS:> 900 090000: Test OK @	

Nucleus Name	**DS_BE_Reset**	
Nucleus Number	901	
Description	Reset the basic engine	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Toggle the reset pin of the I2S interface - In case of an AV3 Toggle the reset pin of the IDE interface	
Execution Time	2 seconds on AV2 9 seconds on AV3 (when disc inside)	
User Input	None	
Error	Number	Description
	90100	Resetting the Basic Engine succeeded
	90101	Resetting the Basic Engine failed
Example	DS:> 901 090100: Test OK @	

Nucleus Name	**DS_BE_GetSelftestResult**	
Nucleus Number	902	
Description	Return the self-test results through the service port	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the S2B GET_SELF_TEST_RESULT command - In case of an AV3 Send the ATAPI REPORT_DRIVE_DIAGNOSTICS command - On error display the specific error codes received from the BE	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	90200	Self test succeeded, no errors
	90201	There was a time-out while communicating
	90202	The Basic Engine returned an unexpected result
	90203	The BE returned an error code
	90204	No acknowledge received from BE
	90205	Communicating with the Basic Engine failed
	90206	Basic Engine returned no info
	90207	Self test failed, errors are echoed
Example	DS:> 902 090200: Self-test result byte : 00000000 Self-test result byte : 00000000 Self-test result byte : 00000000 Test OK @	

Nucleus Name	**DS_BE_VersionGet**	
Nucleus Number	903	
Description	Get the version of the basic engine and that of the optical unit	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 send the S2B GET_VERSION_NUMBER command - In case of an AV3 send the ATAPI INQUIRY command - Send the GET_OPU_VERSION command - Display the returned version information	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	90300	BE version OK
	90301	There was a time-out while communicating
	90302	The Basic Engine returned an unexpected result
	90303	The BE returned an error code
	90304	No acknowledge received from BE
	90305	Communicating with the Basic Engine failed
	90306	The BE returned no info
Example	DS:> 903 090300: BE version = 31.30.24. PHILIPS ,VAD8031 ,31302400,REL_8031_313024 2073, Optical unit version = 00.06.82.19.00 Test OK @	

Nucleus Name	**DS_BE_TrayOut**	
Nucleus Number	904	
Description	Open the tray of the basic engine	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the S2B TRAY_OUT command - In case of an AV3 send an ATAPI START_STOP_UNIT command	
Execution Time	Approximately 2 seconds	
User Input	None	
Error	Number	Description
	90400	The command executed successfully
	90401	There was a time-out while communicating
	90402	The Basic Engine returned an unexpected result
	90403	The BE returned an error code
	90404	No acknowledge received from BE
	90405	Unable to enter normal mode
	90406	Communicating with the Basic Engine failed
Example	DS:> 904 090400: Test OK @	

Nucleus Name	**DS_BE_TrayIn**	
Nucleus Number	905	
Description	Close the tray of the basic engine	
Technical	- Check if an AV2 or AV3 is connected - Send the S2B TRAY_IN command - In case of an AV3 send an ATAPI START_STOP_UNIT command	
Execution Time	Approximately 1 - 2 seconds	
User Input	None	
Error	Number	Description
	90500	The command executed successfully
	90501	There was a time-out while communicating
	90502	The Basic Engine returned an unexpected result
	90503	The BE returned an error code
	90504	No acknowledge received from BE
	90505	Unable to enter normal mode
	90506	Communicating with the Basic Engine failed
Example	DS:> 905 090500: Test OK @	

Nucleus Name	**DS_BE_WriteReadDvdRw**
Nucleus Number	906
Description	Write data to and read data from a DVD+RW disc through the basic engine for verification of the writing
Technical	- Check if an AV2 or AV3 is connected - Execute DS_BE_GetSelftestResults - Send the TRAY_IN command - Send the READ_TOC command - Generate a random disc location - Generate test data to write to the DVD+RW - In case of an AV2 Transfer the test data to the disc location using DMA - In case of an AV3 Transfer the test data to the disc location using PIO mode ATAPI WRITE_10 - In case of an AV2 Read back the data from disc using DMA - In case of an AV3 Transfer the test data to the disc location using PIO mode ATAPI READ_10 - Compare the two data areas and check whether the areas are equal
Execution Time	Approximately 20 seconds
User Input	None

Error	Number	Description
	90600	The command executed successfully
	90601	This nucleus cannot be executed because the Self-Test failed
	90602	The BE cannot enter normal operating mode
	90603	Unable to send the tray in
	90604	Unable to read TOC from disc
	90605	Invalid disc is loaded, please insert a DVD+RW disc
	90606	Writing the test pattern to DVD+RW failed
	90607	Reading back the test pattern from DVD+RW failed
	90608	Compare check failed
	90609	Calibrating DVD+RW failed
Example	DS:> 906 090600: Testing on sector 0x5dbe0: OK Test OK @	

Nucleus Name	**DS_BE_WriteReadDvdR**	
Nucleus Number	907	
Description	Write data to and read data from a DVD+R disc through the basic engine for verification of the writing	
Technical	- Check if an AV2 or AV3 is connected - Execute DS_BE_GetSelftestResults - Send the TRAY_IN command - Send the READ_TOC command - Use the OPC area to test if the DVD+R is (still) writable - Generate test data to write to the DVD+R - In case of an AV2 Transfer the test data to the disc location using DMA - In case of an AV3 Transfer the test data to the disc location using PIO mode ATAPI WRITE_10 - In case of an AV2 Read back the data from disc using DMA - In case of an AV3 Transfer the test data to the disc location using PIO mode ATAPI READ_10 - Compare the two data areas and check whether the areas are equal	
Execution Time	Approximately 20 seconds	
User Input	None	
Error	Number	Description
	90700	The command executed successfully
	90701	This nucleus cannot be executed because the Self-Test failed
	90702	The BE cannot enter normal operating mode
	90703	Unable to send the tray in
	90704	Unable to read TOC from disc
	90705	Invalid disc is loaded, please insert a DVD+RW disc
	90706	Unable to write, the DVD+R disc is full
	90707	No writable DVD+R sector found
	90708	Writing the test pattern to DVD failed
	90709	Reading back the test pattern from DVD failed
	90710	Compare check failed
Example	DS:> 907 090700: Testing on sector 0x36210: OK Test OK @	

Nucleus Name	**DS_BE_StatisticalInformationGet**
Nucleus Number	908
Description	Retrieve the statistical information from the basic engine
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the S2B GET_STATISTICAL_INFO command - In case of an AV3 Send the transparent BIT engine GET_STATISTICAL_INFO command - Display the info returned from the BE
Execution Time	Less than 1 second on AV2 2 seconds on AV3
User Input	None

Error	Number	Description
	90800	The command executed successfully
	90801	There was a time-out while communicating
	90802	The Basic Engine returned an unexpected result
	90803	The BE returned an error code
	90804	No acknowledge received from BE
	90805	Communicating with the Basic Engine failed
	90806	The BE returned no info

Example (AV2)

```
DS:> 908
Number of times Tray went Open/Closed :  4
Total minutes the CD laser was on       : 0
Total minutes the DVD laser was on      : 0
Total minutes the write laser was on    : 0
090800:
Test OK @
```

Example (AV3)

```
DS:> 908
Number of times Tray went Open/Closed                        4
Total time the power power on (HR:MIN)                      0:0h
Total time of reading CDROM discs (HR:MIN)                  0:0h
Total time of reading high speed CD-R discs (HR:MIN)        0:0h
Total time of reading other CD-R discs (HR:MIN)             0:0h
Total time of reading high speed CD-RW discs (HR:MIN)       0:0h
Total time of reading other CD-RW discs (HR:MIN)            0:0h
Total time of reading high speed DVD SL discs (HR:MIN)      0:0h
Total time of reading other DVD SL discs (HR:MIN)           0:0h
Total time of reading high speed DVD DL discs (HR:MIN)      0:0h
Total time of reading other DVD DL discs (HR:MIN)           0:0h
Total time of reading high speed DVD+R discs (HR:MIN)       0:0h
Total time of reading other DVD+R discs (HR:MIN)            0:2h
Total time of reading high speed DVD+RW discs (HR:MIN) 0:0h
Total time of reading other DVD+RW discs (HR:MIN)           0:35h
Total time of writing DVD+R discs at 2.4 x (HR:MIN)        0:0h
Total time of writing DVD+R discs at 4 x (HR:MIN)          0:0h
Total time of writing DVD+RW discs at 2.4 x (HR:MIN)       0:0h
Total time of writing DVD+RW discs at 4 x (HR:MIN)         0:0h
090800:
Test OK @
```

Nucleus Name	**DS_BE_StatisticalInformationReSet**	
Nucleus Number	909	
Description	Reset the statistical information in the basic engine	
Technical	- Send the RESET_STATISTICAL_INFO command - Send the POWER_DOWN command - Toggle the reset pin of the I2S interface	
Execution Time	2 seconds	
User Input	None	
Error	Number	Description
	90900	The command executed successfully
	90901	There was a time-out while communicating
	90902	The Basic Engine returned an unexpected result
	90903	The BE returned an error code
	90904	No acknowledge received from BE
	90905	Communicating with the Basic Engine failed

Example

```
DS:> 909
090900:
Test OK @
```

Nucleus Name	**DS_BE_ErrorLogGet**
Nucleus Number	910
Description	Get the error log from the basic engine
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the S2B GET_ERROR command - In case of an AV3 Send the transparent BIT engine GET_ERROR and GET_FATAL commands - Display the returned info
Execution Time	Less than 1 second
User Input	None

Error	Number	Description
	91000	The command executed successfully
	91001	There was a time-out while communicating
	91002	The Basic Engine returned an unexpected result
	91003	The BE returned an error code
	91004	No acknowledge received from BE
	91005	Communicating with the Basic Engine failed
	91006	The BE returned no info
Example (AV2)	DS:> 910 Momentary errors (Byte 1 - Byte 7) : 0x00 0x00 0x00 0x00 0x00 0x00 0x00 Cumulative errors (Byte 1 - Byte 7) : 0x00 0x00 0x00 0x20 0x00 0x00 0x00 Fatal errors (Oldest - Youngest) : 0x00 0x00 0x00 0x00 0x00 091000: Test OK @	
Example (AV3)	DS:> 910 Momentary errors (0-9): 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 Cumulative errors (1-9) : 0x00 0x80 0x20 0x00 0x00 0x00 0x00 0x00 0x00 Software fatal assert : 799 engineproxy.cpp 091000: Test OK @	

Nucleus Name	**DS_BE_ErrorLogReset**	
Nucleus Number	911	
Description	Reset the error log in the basic engine	

Technical	- Check if an AV2 or AV3 is connected
	- In case of an AV2
	  - Send theS2B RESET_STATISTICAL_INFO command
	  - Send the S2B POWER_DOWN command
	  - Toggle the reset pin of the I2S interface
	- In case of an AV3 Send the transparent BIT engine RESET_STATISTICAL_INFO command	

Execution Time	2 seconds	
User Input	None	
Error	Number	Description
	91100	The command executed successfully
	91101	There was a time-out while communicating
	91102	The Basic Engine returned an unexpected result
	91103	The BE returned an error code
	91104	No acknowledge received from BE
	91105	Communicating with the Basic Engine failed
Example	DS:> 911 091100: Test OK @	

Nucleus Name	**DS_BE_JitterOptimise**
Nucleus Number	912
Description	Perform jitter optimisation: A formatted DVD must be loaded into the engine before executing this nucleus

Technical	- Check if an AV2 or AV3 is connected
	- Send the TRAY_IN command
	- Send the READ_TOC command
	- In case of an AV2
	  - Send the JITTER_COMMAND command with parameter 0x00 0x00
	  - Send the JITTER_COMMAND command with parameter 0x00 0x01
	  - Send the JITTER_COMMAND command with parameter 0x00 0x02 until offset 0x80 is received
	- In case of an AV3 Send the MEASURE_JITTER_BLER_PPN command and display the average jitter and bler values

Execution Time	Approximately 20 seconds
User Input	none

Error	Number	Description
	91200	Optimising jitter succeeded
	91201	There was a time-out while communicating
	91202	The Basic Engine returned an unexpected result
	91203	The Basic Engine returned an error code
	91204	No acknowledge received from BE
	91205	Unable to send tray in
	91206	Unable to read the disc
	91207	No disc is loaded
	91208	Unknown disc is loaded
	91209	Unable to enter service mode
Example (AV2)	DS:> 912 091200: Jitter bathtub: (-42,135)(-40,127)(-38,106)(-36,106)(-34,101)(-32,97)(-30,92)(-28,92)(-26,92)(-24,92)(-22,86)(-20,80)(-18,86)(-16,86)(-14,80)(-12,80)(-10,80)(-8,80)(-6,80)(-4,86)(-2,86)(0,86)(2,86)(4,92)(6,92)(8,101)(10,106)(12,111)(14,120)(16,123)(18,127)(20,142) Test OK @	
Example (AV3)	DS:> 912 091200: Average Jitter, Bler C1, Bler C2: (92,4,254) Test OK @	

Nucleus Name	**DS_BE_FocusOn**	
Nucleus Number	913	
Description	Put the laser of the BE into focus	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the FOCUS command with parameter 0x01 - In case of an AV3 Send the transparent BIT engine FOCUS command	
Execution Time	3 seconds	
User Input	None	
Error	Number	Description
	91300	Focus on succeeded
	91301	There was a time-out while communicating
	91302	The Basic Engine returned an unexpected result
	91303	The BE returned an error code
	91304	No acknowledge received from BE
	91305	Communicating with the Basic Engine failed
	91306	Unable to enter service mode
Example	DS:> 913 091300: Test OK @	

Nucleus Name	**DS_BE_FocusOff**	
Nucleus Number	914	
Description	Turn off putting the laser of the BE into focus	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the FOCUS command with parameter 0x00 - In case of an AV3 Send the transparent BIT engine FOCUS command	
Execution Time	Less than 1 second on AV2 2 seconds on AV3	
User Input	None	
Error	Number	Description
	91400	Focus off succeeded
	91401	There was a time-out while communicating
	91402	The Basic Engine returned an unexpected result
	91403	The BE returned an error code
	91404	No acknowledge received from BE
	91405	Communicating with the Basic Engine failed
	91406	Unable to enter service mode
Example	DS:> 914 091400: Test OK @	

Nucleus Name	**DS_BE_MotorOn**
Nucleus Number	915

Example(AV2)	DS:> 920 092000: Tilt sensor bathtub: (71,-12,145)(68,-12,135)(62,-10,120)(56,-92,97)(50,-75,86)(44,-59,80)(41,-52,80)(35,-37,86)(29,-22,86)(23,-7,92)(17,8,111)(11,23,135)(8,31,138)(5,39,158) Test OK @
Example (AV3)	DS:> 920 092010: Tilt function is not supported by the engine Error @

Nucleus Name	**DS_BE_CheckDisc**	
Nucleus Number	921	
Description	Check whether there is a disc inside the BE	
Technical	- Send the TRAY_IN command - Send the READ_TOC command - Display the Disc type info - If Disc type is a DVD+R(W), then read ADIP info. - Display manufacturer and media type.	
Execution Time	Approximately 10 seconds	
User Input	None	
Error	Number	Description
	92100	There was a disc inside the set
	92101	Unable to load the tray
	92102	Error received from BE
Example	DS:> 921 092100: Disc type: DVD+RW disc Disc manufacturer id: PHILIPS Media type id: 010 Test OK @ DS:> 921 090500: Disc type: None Test OK @ DS:> 921 092100: Disc type: DVD+R disc Disc manufacturer id: RICOHJPN Media type id: R00 Test OK @	

Nucleus Name	**DS_BE_SledgeMotor**	
Nucleus Number	922	
Description	Send the sledge to its home position, then to the middle of the disc, and then to the end.	
Technical	- Send the PCS_COMMAND command with parameter 0x03 0x00 - Send the PCS_COMMAND command with parameter 0x02 0x00 - Send the PCS_COMMAND command with parameter 0x00 0x01 - Send the PCS_JUMP_SLEGE_STEPS command for 3 times - Send the PCS_COMMAND command with parameter 0x00 0x00	
Execution Time	4 seconds on AV2 11 seconds on AV3	
User Input	None	
Error	Number	Description
	92200	The command executed successfully
	92201	There was a time-out while communicating
	92202	The Basic Engine returned an unexpected result
	92203	The BE returned an error code
	92204	No acknowledge received from BE
	92205	Communicating with the Basic Engine failed
	92206	Unable to enter service mode
Example	DS:> 922 092200: Test OK @	

Description	Turn on the turntable motor	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the TURN_TABLE_MOTOR_ON command - In case of an AV3 Send the transparent BIT engine TTM command	
Execution Time	Less than 1 second on AV2 4 seconds on AV3	
User Input	None	
Error	Number	Description
	91500	Turn table motor is on
	91501	There was a time-out while communicating
	91502	The Basic Engine returned an unexpected result
	91503	The BE returned an error code
	91504	No acknowledge received from BE
	91505	Communicating with the Basic Engine failed
	91506	Unable to enter service mode
Example	DS:> 915 091500: Test OK @	

Nucleus Name	**DS_BE_MotorOff**	
Nucleus Number	916	
Description	Turn off the turntable motor	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 Send the TURN_TABLE_MOTOR_ON command - In case of an AV3 Send the transparent BIT engine TTM command	
Execution Time	Less than 1 second on AV2 4 seconds on AV3	
User Input	None	
Error	Number	Description
	91600	Turn table motor is off
	91601	There was a time-out while communicating
	91602	The Basic Engine returned an unexpected result
	91603	The BE returned an error code
	91604	No acknowledge received from BE
	91605	Communicating with the Basic Engine failed
	91606	Unable to enter service mode
Example	DS:> 916 091600: Test OK @	

Nucleus Name	**DS_BE_Tilt**	
Nucleus Number	920	
Description	Test the tilt mechanism control loop, or allow its proper functioning to be measured. Before executing this nucleus a disc must be loaded in the recorder	

Technical	- Check if an AV2 or AV3 is connected
	- In case of an AV2
	  - Send the TRAY_IN command
	  - Send the READ_TOC command
	  - Send the TILT_COMMAND command with parameter 0x00 0x00
	  - Send the TILT_COMMAND command with parameter 0x00 0x02
	- In case of an AV3 display a “not supported” message	

Execution Time	Approximately 15 seconds	
User Input	None	
Error	Number	Description
	92000	The command executed successfully
	92001	There was a time-out while communicating
	92002	The Basic Engine returned an unexpected result
	92003	The Basic Engine returned an error code
	92004	No acknowledge received from BE
	92005	Unable to send tray in
	92006	Unable to read the disc
	92007	No disc is loaded
	92008	Unknown disc is loaded
	92009	Unable to enter service mode
	92010	This nucleus is not supported by the engine

Nucleus Name	**DS_BE_ReadTocInfo**	
Nucleus Number	924	
Description	Read the TOC from the disc. This gives a good indication if the BE works properly.	
Technical	- Send the TRAY_IN command - Send the READ_TOC command - Display the TOC info.	
Execution Time	Approximately 10 seconds	
User Input	None	
Error	Number	Description
	92400	A disc is loaded, TOC info if echoed
	92401	Unable to load the tray
	92402	The BE has not returned TOC info
	92403	Error received from BE
Example	DS:> 924 092400: TOC info [hex] = 91 3A 0C Test OK @ DS:> 924 092403: The BE returned: 0x10 #{no_disc_error} No disc is detected Error @ DS:> 924 092403: The BE returned: 0x1e #{illegal_medium_error} Engine unable to handle current disc. Probably illegal medium. Error @	

Nucleus Name	**DS_BE_DiscErase**	
Nucleus Number	925	
Description	Perform a DC-erase on a DVD+RW disc.	
Technical	-Check if an AV2 or AV3 is connected -In case of an AV2 -Execute DS_BE_GetSelftestResults -Send the TRAY_IN command -Send the READ_TOC command -Send the SET_INPUT_TYPE command with parameter DC_ERASE -Overwrite the header of the DVD+RW disc with DC erase data -Send the SET_INPUT_TYPE command with parameter NORMAL. -In case of an AV3 display a "not supported" message	
Execution Time	Approximately 1:15 minute	
User Input	None	
Error	Number	Description
	92500	A DVD+RW disc is erased
	92501	This nucleus cannot be executed because the Self-Test failed
	92502	The BE cannot enter normal operating mode
	92503	Unable to send the tray in
	92504	Unable to read TOC from disc
	92505	Invalid disc is loaded, please insert a DVD+RW disc
	92506	Calibrating DVD+RW failed
	92507	Set Input Type command failed
	92508	Erasing the DVD+RW disc failed
	92509	Erasing is aborted by user
	92510	This nucleus is not supported by the engine
Example (AV2)	DS:> 925 The entirely disc will be erased. Are you sure you want this?[y/n] 092500: Test OK @	
Example (AV3)	092510: This nucleus is not supported by the engine Error @	

Nucleus Name	**DS_BE_RegionCodeSet**
Nucleus Number	928
Description	Set the region code in the AV3.

Technical	- Check if an AV2 or AV3 is connected - In case of anAV2 display a “not supported” message - In case of an AV3 send the ATAPI SEND_KEY command	
Execution Time		
User Input	Region code	
Error	Number	Description
	92800	The command executed successfully
	92801	There was a time-out while communicating
	92802	The Basic Engine returned an unexpected result
	92803	The BE returned an error code
	92804	No acknowledge received from BE
	92805	Communicating with the Basic Engine failed
	92806	No disc is present, please insert disc
	92807	Region code out of range
	92808	User input wrong
	92809	Region counter expired
	92810	This nucleus is not supported by the engine
Example (AV2)	DS:> 928 092810: This nucleus is not supported by the engine Error @	
Example (AV3)	DS:> 928 1 092800: Test OK @	

Nucleus Name	**DS_BE_RegionCodeGet**	
Nucleus Number	929	
Description	Read the region code from the AV3.	
Technical	- Check if an AV2 or AV3 is connected - In case of anAV2 display a “not supported” message - In case of an AV3 send the ATAPI REPORT_KEY command	
Execution Time		
User Input	None	
Error	Number	Description
	92900	The command executed successfully
	92901	There was a time-out while communicating
	92902	The Basic Engine returned an unexpected result
	92903	The BE returned an error code
	92904	No acknowledge received from BE
	92905	Communicating with the Basic Engine failed
	92906	This nucleus is not supported by the engine
Example (AV2)	DS:> 929 092906: This nucleus is not supported by the engine Error @	
Example (AV3)	DS:> 929 092900: DVD region 1 Test OK @	

Nucleus Name	**DS_BE_RegionCounterReset**	
Nucleus Number	930	
Description	Reset the region counter in the AV3.	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 display a “not supported” message - In case of an AV3 send a special ATAPI RESET_REGION_COUNTER command	
Execution Time		
User Input	None	
Error	Number	Description
	93000	The command executed successfully
	93001	There was a time-out while communicating
	93002	The Basic Engine returned an unexpected result
	93003	The BE returned an error code
	93004	No acknowledge received from BE
	93005	Communicating with the Basic Engine failed
	93006	This nucleus is not supported by the engine

Example (AV2)	DS:> 930 093006: This nucleus is not supported by the engine Error @
Example (AV3)	DS:> 930 093000: Test OK @

Nucleus Name	**DS_BE_AdjustLaserControl**	
Nucleus Number	931	
Description	Adjust the DVD-M (with the OPU) with PCBA. (So adjusts the two PCBS to each other)	
Technical	- Check if an AV2 or AV3 is connected - In case of an AV2 display a "not supported" message - In case of an AV3 adjust the DVD-M (with the OPU) with PCBA by sending a S2B command to align the PCBs to each other.	
Execution Time	30 seconds	
User Input	None	
Error	Number	Description
	93100	The command executed successfully
	93101	There was a time-out while communicating
	93102	The Basic Engine returned an unexpected result
	93103	The BE returned an error code
	93104	No acknowledge received from BE
	93105	Communicating with the Basic Engine failed
	93106	Unable to enter service mode
	93107	This nucleus is not supported by the engine
Example (AV2)	DS:> 931 093107: This nucleus is not supported by the engine Error @	
Example (AV3)	DS:> 931 093100: Test OK @	

System (SYS)

Nucleus Name	**DS_SYS_HardwareVersionGet**	
Nucleus Number	1200	
Description	Get the hardware version and type of the digital board	
Technical	Initialise the PIO pins of the Codec Read the segment header in FLASH and determine hardware version	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	120000	Getting the hardware version and type of the digital board succeeded
	120001	Getting the hardware version and type of the digital board failed
	120002	Wrong hardware version read from FLASH
Example	DS:> 1200 120000: Hardware ID = 0x29 Test OK @	

Nucleus Name	**DS_SYS_SoftwareVersionBootGet**	
Nucleus Number	1201	
Description	Get the version of the boot software on the digital board	
Technical	Read the segment header in FLASH and determine Boot software version	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	120100	Getting the Boot software version succeeded
	120101	Getting the Boot software version failed
Example	DS:> 1201 120100: Software Boot Version = 0331 Test OK @	

Nucleus Name	**DS_SYS_SoftwareVersionDownloadGet**	
Nucleus Number	1202	
Description	Get the version of the download software on the digital board	
Technical	Read the segment header in FLASH and determine Download software version	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	120200	Getting the Download software version succeeded
	120201	Getting the Download software version failed
Example	DS:> 1202 120200: Software Download Version = 0001 Test OK @	

Nucleus Name	DS_SYS_SoftwareVersionApplGet	
Nucleus Number	1203	
Description	Get the version of the application software on the digital board	
Technical	Read the segment header in FLASH and determine Application software version	
Execution Time	Less than 1 second	
User Input	None	
Error	Number	Description
	120300	Getting the Application software version succeeded
	120301	Getting the Application software version failed
Example	DS:> 1203 120300: Software Application Version = 0001 Test OK @	

Nucleus Name	**DS_SYS_SoftwareVersionDiagnosticsGet**
Nucleus Number	1204
Description	Get the version of the diagnostics software on the digital board
Technical	Read the segment header in FLASH and determine Diagnostics software version
Execution Time	Less than 1 second
User Input	None

Error	Number	Description
	120400	Getting the Diagnostics software version succeeded
	120401	Getting the Diagnostics software version failed
Example	DS:> 1204 120400: Software Diagnostics Version = 0001 Test OK @	

Nucleus Name	**DS_SYS_EepromUpload**	
Nucleus Number	1205	
Description	Upload the contents of the NVRAM on the analogue board or the digital board to the service PC, by using the X-modem protocol	
Technical	- Decode the user input - Determine whether to upload the analogue board or digital board NVRAM - Start uploading using the XMODEM protocol - Determine whether all was uploaded OK	
Execution Time	Depends on the chosen NVRAM and the User.	
User Input	Choose one of the following parameters for the nucleus: 1. Upload the contents of the NVRAM of the digital board 2. Upload the contents of the NVRAM of the analogue board Choose in the terminal on the control PC -> **transfer -> receive file.** Select **X-modem** protocol. Then click **receive** in the dialogue and fill in the file name in which you want to store the data.	
Error	Number	Description
	120500	Download succeeded.
	120501	User input is not valid.
	120502	Something went wrong while copying the data from NVRAM to SDRAM .
	120503	Something went wrong while transferring the data.
	120504	User cancelled the upload.
Example	DS:> 1205 1 120500: Test OK @	

Nucleus Name	**DS_SYS_EepromDownload**	
Nucleus Number	1206	
Description	Download a file with the contents of the NVRAM for the analogue board or the digital board from the service PC to the recorder, by using the X-modem protocol	
Technical	- Decode the user input and determine what EEPROM to fill: digital / analogue - Store the downloaded (using XMODEM) bytes in SDRAM first - Then copy these contents into the EEPROM after verification	
Execution Time	Depends on the chosen NVRAM and the User.	
User Input	Choose one of the following parameters for the nucleus: 1. Download the contents of the NVRAM of the digital board 2. Download the contents of the NVRAM of the analogue board Choose in the terminal of the control **PC -> transfer -> send file.** Select **X-modem** protocol. Then choose a file with the Browse button in the dialogue and click on **send.**	
Error	Number	Description
	120600	Download succeeded
	120601	The write to NVRAM failed.
	120602	Timeout. Too many retries.
	120603	A file was sent with a wrong header.
	120604	User cancelled the download.
	120605	User input is not valid.
	120606	Unknown Error
Example	DS:> 1206 1 120600: Test OK @	

Nucleus Name	**DS_SYS_DvIdNumberSet**
Nucleus Number	1207
Description	Set the IEEE 1394 unique ID
Technical	- Decode the user input - Store the id into NVRAM - Validate the segment of storage by updating the checksum
Execution Time	Less than 1 second.

User Input	The unique ID to be set.	
Error	Number	Description
	120700	Setting the unique DV ID succeeded
	120701	User input is not valid.
	120702	Setting the unique DV ID failed.
	120703	Write succeeded, but checksum is corrupt.
Example	DS:> 1207 1234567890 120700: Test OK @	

Nucleus Name	**DS_SYS_DvIdNumberGet**	
Nucleus Number	1208	
Description	Get the IEEE1394 unique ID	
Technical	- Read out the ID from the configuration segment and return this info to the user	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	120800	Getting the unique DV ID succeeded
	120801	Getting the unique DV ID failed
	120802	Reading an unexpected section version in NVRAM
Example	DS:> 1208 120800: The DvIdNumber is: 1234567890 Test OK @	

Nucleus Name	**DS_SYS_IicWrite**	
Nucleus Number	1209	
Description	Perform an IIC write action on the digital board	
Technical	- Determine bus ID, slave address, number of bytes to be written and the byte array of data from the user input - Initialise IIC - Write the data to the slave specified through IIC	
Execution Time	Less than 1 second	
User Input	The user input the number of bytes to write followed by the bytes to write: <..> Where the bus id is either 0 (normally used) or 1	
Error	Number	Description
	120900	Writing the data over IIC succeeded
	120901	The IIC bus was not accessible
	120902	There was a timeout writing to the device
	120903	The IIC acknowledge was not received
	120904	The communication with the device failed
	120905	Got unknown IIC bus error:
	120906	Unable to initialise IIC bus
	120907	Decoding bus ID unsigned value failed
	120908	Decoding slaveAddr unsigned value failed
	120909	Decoding nrBytes unsigned value failed
	120910	Bus ID out of range
	120911	nrBytes out of range
	120912	Unable to decode parameters
Example	DS:> 1209 0 0xa0 1 0x6 120900: 1 Bytes written Test OK @	

Nucleus Name	**DS_SYS_IicRead**
Nucleus Number	1210
Description	Perform an IIC read action on the digital board
Technical	- Determine the bus ID, slave address and number of bytes to read from the user input - Initialise IIC - Read the data form the slave specified
Execution Time	Less than 1 second

User Input	The user inputs the bus number, the address to read them from and the number of bytes to read: <BusID><Slave address to read from><Number of bytes to read>Where the bus id is either 0 (normally used) or 1	
Error	Number	Description
	121000	Reading the data over IIC succeeded
	121001	The IIC bus was not accessible
	121002	There was a timeout writing to the device
	121003	The IIC acknowledge was not received
	121004	The communication with the device failed
	121005	There was an unknown IIC bus error
	121006	IIC bus initialisation failed
	121007	Decoding bus ID unsigned value failed
	121008	Decoding slave address unsigned value failed
	121009	Decoding number of bytes unsigned value failed
	121010	Bus ID out of range
	121011	nrBytes out of range
Example	DS:> 1210 0 0xa0 0x20 Read : 0x0000: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0008: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0010: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0018: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 121000: 0 0xa0 0x20 Test OK @	

Nucleus Name	**DS_SYS_UartWrite**	
Nucleus Number	1211	
Description	Perform an UART write action on the digital board on a specified UART	
Technical	- Decode the user input for the proper port to use - Write out the bytes through the indicated port	
Execution Time	Less than 1 second.	
User Input	The user inputs the UART to write to, the number of bytes and the bytes to be written to the UART. 1=UART port 1 : not used 2=UART port 2 : Bit Engine 3=UART port 3 : Analogue board <UartNr><Number of bytes to write><d1><d2><..><dx>	
Error	Number	Description
	121100	Writing the bytes to the UART succeeded
	121101	The user provided wrong input
	121102	Writing to the UART failed
Example	DS:> 1211 2 2 0xd1 0x01 121100: Test OK @	

Nucleus Name	**DS_SYS_UartRead**	
Nucleus Number	1212	
Description	Perform an UART read action on the digital board on a specified UART	
Technical	- Decode the user input for the port to read from - Read from the port and return data read to the user	
Execution Time	Less than 1 second.	
User Input	The user inputs the UART to read from. 1=UART port 1 : not used 2=UART port 2 : Bit Engine 3=UART port 3 : Analogue board <UartNr >	
Error	Number	Description
	121200	Reading the data from the UART succeeded
	121201	The user provided wrong input

	121202	Reading the data from the UART failed
Example	DS:> 1212 2 121200: The HEX value that was read is: 0x50 0xD1 0x00 Test OK @	

Nucleus Name	**DS_SYS_VideoLoopThroughStart**	
Nucleus Number	1213	
Description	The video signal, which is conform the user input, is routed from the input to the output. The input is set using the proper nucleus to route the signal on the board(s). All outputs are enabled.	
Technical	- Decode the videosignal: PAL / NTSC and Y/C, RGB, CVBS,YUV - Initialise the Video Input Processor and check for valid signal - Initialise the Video Front End and start capturing frames to memory - Initialise the SYNC module - Initialise the Video Post Processing and retrieve frames from memory - Initialise the mixer - Initialise the DENC module - Route the signal to all outputs	
Execution Time	Less than 1 second, but stays running.	
User Input	<vipInput> <VideoOutput> <VideoStandard> 1. vipInput (CVBS, YC, YUV, RGB, 1 to 9(see table below)). LECO Premier specific User input Video input Data path to VIP 1 RGB SCART aux RGB in 2 YC SCART aux Y/C in 3 CVBS SCART aux CVBS 4 CVBS Tuner 5 YC Front Y/C 6 CVBS Front CVBS 7 CVBS SCART TV CVBS 8 YC CE mode Y/C in 9 CVBS CE mode CVBS in 10 XPORT XPORT 2. VideoOutput (YUV, RGB). 3. VideoStandard (PAL, NTSC).	
Error	Number	Description
	121300	Video LoopthroughStart succeeded
	121301	User input is not valid.
	121302	Initialisation of the VIP failed.
	121303	Unable to stop the loop through before restarting.
	121304	Video Signal on the input is not a valid signal.
	121305	Initialisation of the VFE failed.
	121306	The digital board hardware information is corrupt
Example	DS:> 1213 CVBS RGB PAL 121300: Test OK @	

Nucleus Name	**DS_SYS_VideoLoopThroughStop**	
Nucleus Number	1214	
Description	Stop routing the video input to all the outputs.	
Technical	Stop the DENC and the Video Front End	
Execution Time	Less than 1 second.	
User Input	-	
Error	Number	Description
	121400	VideoLoopthroughStop succeeded
	121401	DENC module on Codec failed.
Example	DS:> 1214 121400: Test OK @	

Nucleus Name	**DS_SYS_VideoLoop**
Nucleus Number	1215

<table>
<tr><td>Description</td><td colspan="2">The Codec generates a video signal with a specific signature and sends it to the output of the digital board. The user selects which video input path must be routed on the digital board and a video standard. The Codec encodes the video signal, checks the signature, and returns a conclusion.
Note: Before executing this nucleus the user must route the video signal on the analog board with the proper nucleus.</td></tr>
<tr><td>Technical</td><td colspan="2">- Evaluate user input.
- Reset the global variables, video memory.
- Fill the video memory with a vertical colourbar.
- Initialise the Codec SYNC-module.
- Initialise the Codec MIXER-module.
- Initialise the Codec VPP-module.
- Initialise the Codec DENC-module.
- Display the original image.
- Initialise the VIP.
- Initialise the Codec VFE-module.
- Try to detect a sync in the VIP input.
- Catch the received image in memory.
- Display the received image.
- Compare the received image with original image.
- Create a conclusion.</td></tr>
<tr><td>Execution Time</td><td colspan="2">3 seconds.</td></tr>
<tr><td>User Input</td><td colspan="2">Video input of the digital board:
- CVBS
- YC
- YUV
- RGB
- TEST (The video output will be routed to the video input on the digital board.)
- 1 to 9 - LECO Premier specific (see table below)
<table>
<tr><th>User input</th><th>Video input</th><th>Data path to VIP</th></tr>
<tr><td>1</td><td>RGB</td><td>SCART aux RGB in</td></tr>
<tr><td>2</td><td>YC</td><td>SCART aux Y/C in</td></tr>
<tr><td>3</td><td>CVBS</td><td>SCART aux CVBS</td></tr>
<tr><td>4</td><td>CVBS</td><td>Tuner</td></tr>
<tr><td>5</td><td>YC</td><td>Front Y/C</td></tr>
<tr><td>6</td><td>CVBS</td><td>Front CVBS</td></tr>
<tr><td>7</td><td>CVBS</td><td>SCART TV CVBS</td></tr>
<tr><td>8</td><td>YC</td><td>CE mode Y/C in</td></tr>
<tr><td>9</td><td>CVBS</td><td>CE mode CVBS in</td></tr>
<tr><td>10</td><td>XPORT</td><td>XPORT</td></tr>
</table>
Video standard:- PAL
- NTSC

When no input is given, the nucleus will take TEST for video input and PAL for video standard.</td></tr>
<tr><td>Error</td><td>Number</td><td>Description</td></tr>
<tr><td></td><td>121500</td><td>Videoloop test succeeded.</td></tr>
<tr><td></td><td>121501</td><td>Wrong user input.</td></tr>
<tr><td></td><td>121502</td><td>The Codec SYNC-module cannot be initialised.</td></tr>
<tr><td></td><td>121503</td><td>The Codec MIXER-module cannot be initialised.</td></tr>
<tr><td></td><td>121504</td><td>The Codec VideoPostProcessor-module cannot be initialised.</td></tr>
<tr><td></td><td>121505</td><td>The Codec DENC-module cannot be initialised.</td></tr>
<tr><td></td><td>121506</td><td>The VideoInputProcessor cannot be initialised.</td></tr>
<tr><td></td><td>121507</td><td>The VideoInputProcessor cannot detect a sync-signal.</td></tr>
<tr><td></td><td>121508</td><td>The Codec VideoFrontEnd-module cannot be initialised.</td></tr>
<tr><td></td><td>121509</td><td>The Codec VideoFrontEnd-module cannot capture a video field.</td></tr>
<tr><td></td><td>121510</td><td>When selected the RGB video input: Error in colour red signal and/or Error in colour green signal and/or Error in colour blue signal. When selected one of the other video inputs: Error in luminance signal (Y) and/or Error in chrominance signal (U) and/or Error in chrominance signal (V).</td></tr>
</table>

	121511	The digital board hardware information is corrupt
Example	DS:> 1215 cvbs ntsc 121500: Test OK @ DS:> 1215 cvbs pal 121508: The VideoInputProcessor cannot detect a sync-signal. Error @ DS:> 1215 yuv ntsc 121511: Error in luminance signal(Y) Error in chrominance signal(U) Error in chrominance signal(V) Error @	

Nucleus Name	**DS_SYS_AudioLoop**	
Nucleus Number	1216	
Description	The user first needs to select how the audio path must be routed on the analogue board and/or digital board before calling this nucleus. The user also has to route the audio outputs back to the inputs by means of cables. In this nucleus the Codec generates an audio sine signal with a specific signature and sends it to the output of the digital board. The Codec encodes the audio signal to MPEG I layer II and after this the signature of the signal will be checked.	
Technical	- The user needs to route the signal to the audio inputs so the test can encode the audio to MPEG I layer II - An audio signal is generated, resulting in a sine of 6kHz on the left and 12kHz on the right channel. - Then the signal is decoded in memory. - When both signals are detected correctly in the MPEG, the test succeeded.	
Execution Time	Approximately 9 seconds	
User Input	None	
Error	Number	Description
	121600	Testing the components on the audio signal path succeeded
	121601	The audio encoder did not initialise.
	121602	No audio could be generated.
	121603	The audio encoder did not encode audio.
	121604	The audio could not be decoded.
	121605	Frequency on left channel out of range.
	121606	Frequency on right channel out of range.
	121607	The frequencies on both channels are out of range.
	121608	Frequency on left channel out of range. Right channel silent.
	121609	Right channel is silent.
	121610	Frequency on right channel out of range. Left channel silent.
	121611	Left channel is silent.
	121612	Both channels are silent.
Example	DS:> 1216 121600: Test OK @	

Nucleus Name	**DS_SYS_SlashVersionSet**	
Nucleus Number	1217	
Description	Set the slash version of the system	
Technical	- Decode the user input for the slash version to set - Issue the command to set the slash version to the analogue board	
Execution Time	Less than 1 second.	
User Input	The slash version	
Error	Number	Description
	121700	Setting the slash version succeeded
	121701	Invalid slash version, no slash version is set.
	121702	Setting the slash version on the Analogue Board fails.
	121703	Invalid input.

	121704	The returned error code from the analogue board is unknown:
	121705	No DS error code known for analogue board error:
	121706	There was no response from the analogue board.
	121707	Retrieving the current version failed
	121708	Unknown recorder layout type
	121709	Validating the section where the version is stored failed
	121710	Getting the configuration section from NVRAM failed
	121711	Initialisation of IIC or reaching NVRAM failed
Example	DS:> 1217 82 121700: Test OK @	

Nucleus Name	**DS_SYS_SlashVersionGet**	
Nucleus Number	1218	
Description	Get the slash version of the system	
Technical	- Issue the command to get the slash version to the analogue board - Return the received information to the user	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	121800	Getting the slash version succeeded
	121801	Getting the slash version failed
	121802	The IIC write failed
	121803	The IIC read failed
	121804	There was no response from the analogue board.
	121805	No DS error code known for analogue board error:
	121806	Reading the slash version failed
	121807	Initialisation of IIC or reaching NVRAM failed
	121808	Reading an unexpected section version in NVRAM
Example	DS:> 1218 121800: The slash version is: 82 Test OK @	

Nucleus Name	**DS_SYS_Virginize**	
Nucleus Number	1219	
Description	(Re-) Virginize the recorder. User data in the NVRAM of the analogue board is cleared	
Technical	Issue the command to return to the factory defaults to the analogue board	
Execution Time	1 second.	
User Input	None	
Error	Number	Description
	121900	Virginization succeeded
	121901	Virginization on the Analogue Board failed.
	121902	The returned error code from the analogue board is unknown:
	121903	No DS error code known for analogue board error:
	121904	There was no response from the analogue board.
Example	DS:> 1219 121900: Test OK @	

Nucleus Name	**DS_SYS_VirginModeOn**	
Nucleus Number	1220	
Description	Turn on the virgin mode functionality (e.g. the auto channel search upon start-up)	
Technical	Issue the command to set the bit for the virgin mode to the analogue board	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	122000	Turning on the virgin mode succeeded
	122001	Turning on VirginMode on the Analogue Board failed.
	122002	The returned error code from the analogue board is unknown:
	122003	No DS error code known for analogue board error:

	122004	There was no response from the analogue board.
	122005	Section validation or write failed in NVRAM
	122006	Reading the CONFIG section from NVRAM failed
	122007	Initialisation of IIC or reaching NVRAM failed
Example	DS:> 1220 122000: Test OK @	

Nucleus Name	**DS_SYS_VirginModeOff**	
Nucleus Number	1221	
Description	Turn off the virgin mode functionality (e.g. the auto channel search upon start-up)	
Technical	Issue the command to reset the bit for the virgin mode to the analogue board	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	122100	Turning off the virgin mode succeeded
	122101	Turning off VirginMode on the Analogue Board failed.
	122102	The returned error code from the analogue board is unknown:
	122103	No DS error code known for analogue board error:
	122104	There was no response from the analogue board.
	122105	Section validation or write failed in NVRAM
	122106	Reading the CONFIG section from NVRAM failed
	122107	Initialisation of IIC or reaching NVRAM failed
Example	DS:> 1221 122100: Test OK @	

Nucleus Name	**DS_SYS_VirginModeGet**	
Nucleus Number	1222	
Description	Get the virgin mode functionality status (e.g. the auto channel search upon start-up)	
Technical	Issue the command to reset the bit for the virgin mode to the analogue board	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	122200	Getting the virgin mode succeeded
	122201	Reading the Virgin Mode flag from NVRAM failed
	122202	Initialisation of IIC or reaching the NVRAM failed
	122203	Reading an unexpected version of the section in NVRAM
Example	DS:> 1222 122200: The Virgin Mode functionality is: ON Test OK @	

Nucleus Name	**DS_SYS_DisplayFatalOn**	
Nucleus Number	1223	
Description	Turn on the display-fatal functionality which displays debug-information on the display when encountering a fatal error condition from which could not be recovered automatically	
Technical	Issue the command to use the display-fatal functionality to the analogue board	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	122300	Turning on the display-fatal functionality succeeded
	122301	Turning on the display-fatal functionality failed
	122302	The returned error code from the analogue board is unknown:
	122303	No DS error code known for analogue board error:
	122304	There was no response from the analogue board.
	122305	Section validation or write failed in NVRAM
	122306	Reading the section from NVRAM failed
	122307	Initialisation of IIC or reaching NVRAM failed
Example	DS:> 1223 122300: Test OK @	

Nucleus Name	**DS_SYS_DisplayFatalOff**	
Nucleus Number	1224	
Description	Turn off the display-fatal functionality which displays debug-information on the display when encountering a fatal error condition from which could not be recovered automatically	
Technical	Issue the command to stop using the display-fatal functionality to the analogue board	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	122400	Turning off the display-fatal functionality succeeded
	122401	Turning off the display-fatal functionality failed
	122402	The returned errorcode from the analogue board is unknown:
	122403	No DS errCode known for analogue board error:
	122404	There was no response from the analogue board.
	122405	Section validation or write failed in NVRAM
	122406	Reading the section from NVRAM failed
	122407	Initialisation of IIC or reaching NVRAM failed
Example	DS:> 1224 122400: Test OK @	

Nucleus Name	**DS_SYS_DisplayFatalGet**	
Nucleus Number	1225	
Description	Get the display-fatal flag of the recorder	
Technical	Issue the command to get the status of the display-fatal functionality to the analogue board	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	122500	Getting the display-fatal flag succeeded
	122501	Getting the display-fatal flag failed
	122502	The returned errorcode from the analogue board is unknown:
	122503	No DS errCode known for analogue board error:
	122504	There was no response from the analogue board.
	122505	Reading the display fatal flag failed
	122506	Initialisation of IIC or reaching NVRAM failed
	122507	Unexpected version read from NVRAM section
	122508	Reading the fatal flag from NVRAM failed
Example	DS:> 1225 122500: The Display Fatal functionality is ON Test OK @	

Nucleus Name	**DS_SYS_SettingsSet**	
Nucleus Number	1226	
Description	Programs the digital board settings into the boot EEPROM on the digital board.	
Technical	Evaluate user input. Set-up IIC-bus. Write data to boot EEPROM. Update checksum.	
Execution Time	1 second	
User Input	A large hexadecimal value that represents the digital board settings obtained from the XDIVTOOL.exe program or from a reference set.	
Error	Number	Description
	122600	The settings were successfully programmed.
	122601	User input is invalid.
	122602	IIC access failed.
Example	DS:> 1226 6469616774737462010102000101010101000020080000 122600: Test OK @	

Nucleus Name	**DS_SYS_SettingsDisplay**
Nucleus Number	1228
Description	Show the settings that are programmed in the BROM on the digital board.
Technical	Set-up IIC-bus. Read Digital Board Settings from boot EEPROM. Display the settings.

Execution Time	1 second	
User Input	None.	
Error	Number	Description
	122800	The settings were successfully displayed.
	122801	IIC access failed.
	122802	Invalid settings

Example

```
DS:> 1228
Settings
ID:
444248491D9420014E46332B0000000029040303000101020001010040080800
Board name:                       NF3+
Hardware ID:                      29
Codec IC:                         PNX7100_C2/C3
Video Input Processor IC:         SAA7118
Progressive Scan Deinterlacer IC:  S2301
Progressive Scan Denc IC:          None
I-Link physical layer circuit IC:  PDI1394P25
I-Link link layer circuit IC:      PDI1394P40
Audio clock:                       Clock scheme 1
Bit engine connector:              not available
IDE connector 1:                   available
IDE connector 2:                   available
PCI connector:                     not available
RAM size                           64MByte
ROM size (NOR FLASH bank 1)        8MByte
ROM size (NOR FLASH bank 2)        8MByte
ROM size (NAND FLASH)              Not available
Bit Engine:                        AV 3.1

122800:
Test OK @
```

Nucleus Name	**DS_SYS_SettingsGet**	
Nucleus Number	1229	
Description	Get the digital board diversity settings string that is programmed in the BROM on the digital board.	
Technical	- Set-up IIC-bus. - Read Digital Board Settings from boot EEPROM. - Read System Settings from boot EEPROM.-Display the settings.	
Execution Time	1 second	
User Input	None.	
Error	Number	Description
	122900	The settings were successfully displayed.
	122901	IIC access failed.
	122902	The settings are invalid

Example

```
DS:> 1229
122900: 6D7920626F61726400020300010101020101000020080000
Test OK @
```

Nucleus Name	**DS_SYS_AudioLoopThroughStart**	
Nucleus Number	1230	
Description	Description: The audio input is routed from the input to all outputs. The input is set routing the signal with the proper nucleus. All outputs are enabled.	
Technical	- Encode the audio to AC3 in memory - Decode the AC3 in memory to audio on the outputs	
Execution Time	1second buffer time and 30 seconds playing.	
User Input	None.	
Error	Number	Description
	123000	AudioLoopthroughStart succeeded
	123001	Resetting the audio decoder failed
	123002	Resetting the audio encoder failed
	123003	Encoding the audio failed
	123004	Decoding the audio failed

Example

```
DS:> 1230
123000:
Test OK @
```

Nucleus Name	**DS_SYS_AudioLoopThroughStop**	
Nucleus Number	1231	
Description	Stop routing the audio input to all the outputs	
Technical	Send the Mute command to the audio decoder and reset the audio decoder	
Execution Time	Less than 1 second.	
User Input	-	
Error	Number	Description
	123100	AudioLoopthroughStop succeeded
	123101	Resetting the audio decoder failed
	123102	Resetting the audio encoder failed
Example	DS:> 1231 123100: Test OK @	

Nucleus Name	**DS_SYS_SettingsHwIdSet**	
Nucleus Number	1232	
Description	This nucleus sets the HW-Id in the HW-diversity string	
Technical	- Read out the HW-diversity string - Modify the HW-ID in that string as requested - Write the modified HW-diversity string to the EEPROM	
Execution Time	Less than 1 second.	
User Input	- The hardware ID to set No input - The user will be asked for the ID	
Error	Number	Description
	123200	Setting the hardware ID succeeded
	123201	Setting the hardware ID failed
	123202	The user aborted setting the hardware ID, no changes made
Example	DS:> 1232 Enter the new HW ID of the digital board (Currently equals 21) Enter a value between 0 and 99: > 22 The HW ID will be set to: 22. Is that correct? ([Y/N]):y 123200: Test OK @ DS:> 1232 Enter the new HW ID of the digital board (Currently equals 22) Enter a value between 0 and 99: > The HW ID will be set to: 0. Is that correct? ([Y/N]):N 123202: Setting the HW ID was aborted by the user. Error @ DS:> 1232 99 123200: Test OK @	

Nucleus Name	**DS_SYS_SettingsDoubleCheck**	
Nucleus Number	1233	
Description	Double check whether stored HW-string equals actual HW as far as we can automatically detect this. An automatic and a manual mode is supported.	
Technical	- Read out the HW diversity string - Check whether these settings correspond the actual hardware - In case of modification: Write back the new HW-diversity settings.	
Execution Time	4 seconds in auto mode when everything matches	
User Input	- 'manual' or 'MANUAL' to enter manual mode - default is automatic mode where the nucleus stops upon and reports the first encountered error	
Error	Number	Description
	123300	Double checking the HW-diversity settings succeeded
	123301	Double check failed, a difference in settings was encountered
	123302	Reading the HW-diversity settings failed

	123303	Writing the modified HW-diversity settings failed

Example

```
DS:> 1233
123300:
Test OK @

DS:> 1233 manual
123300:
Test OK @

DS:> 1233
123301:
Hardware ID mismatch: in HW-Diversity string:99, actual in FLASH:0
Error @

DS:> 1233 manual
Hardware ID mismatch! in HW-Diversity string:99, actual in FLASH:0

Enter the correct HW ID of the digital board.
>  0
The HW-diversity string has been modified by you. Settings:
Board name:                          DIAG
Hardware ID:                         0
Codec IC:                            PNX7100_MF3
Video Input Processor IC:            SAA7118
Progressive Scan Deinterlacer IC:    None
Progressive Scan Denc IC:            ADV7196
I-Link physical layer circuit IC:    PDI1394P25
I-Link link layer circuit IC:        PDI1394P40
Audio clock:                         Clock scheme 1
Bit engine connector:                available
IDE connector 1:                     available
IDE connector 2:                     not available
PCI connector:                       not available
RAM size                             32MByte
ROM size (NOR FLASH bank 1)          8MByte
ROM size (NOR FLASH bank 2)          Not available
ROM size (NAND FLASH)                Not available

Is it OK to program this inthe new HW-diversity string? ([y]es/[n]o):y
Diversity HW-string programmed successfully.

123300:
Test OK @

DS:>
```

Nucleus Name	**DS_SYS_SettingsDlTableFilenameSet**	
Nucleus Number	1234	
Description	This nucleus sets the Download table filename in the HW-diversity string	
Technical	- Retrieve the new filename from the user - Ask the user whether the filename is correct before setting it - Update the diversity settings to use the newly entered filename	
Execution Time	Dependent on the user confirmation	
User Input	- The filename to be set - No input - No new filename will be set	
Error	Number	Description
	123400	Setting the new filename succeeded
	123401	Unsupported setting of the current HW-diversity settings

	123402	Setting the filename was aborted by the user.
Example	DS:> 1234 Enter the new Download Table Filename (Currently equals DVDR2001.001) Enter a filename: > The Download Table Filename will be set to: DVDR2001.001. Is that correct? ([Y/N]): 123402: Setting the filename was aborted by the user. Error @ DS:> 1234 Enter the new Download Table Filename (Currently equals DVDR2001.001) Enter a filename: >DVDR2002.001 The Download Table Filename will be set to: DVDR2002.001. Is that correct? ([Y/N]):Y 123400: Test OK @	

Nucleus Name	**DS_SYS_IicWriteRead**	
Nucleus Number	1235	
Description	Perform an IIC write-read action on the digital board	
Technical	- Determine bus ID, slave address, number of bytes to be written and the byte array of data from the user input - Initialise IIC - Write the data to the IIC slave - Read the data from the IIC slave	
Execution Time	Less than 1 second	
User Input	The user inputs the Bus ID, Slave Address, number of bytes to read, number of bytes to write and the bytes to be written <NucNr><BusId><SlaveAddr><ReadLen><WriteLen><WrByte0...WrByteN> Max number of bytes to write: 255 Max number of bytes to read: 255	
Error	Number	Description
	123500	Writing data to and reading data from the IIC slave succeeded
	123501	The IIC bus was not accessible
	123502	There was a bus timeout reading the device
	123503	The IIC acknowledge was not received
	123504	Unable to initialise IIC bus
	123505	The communication with the device failed
	123506	Unknown IIC bus error received
	123507	Decoding bus ID unsigned value failed
	123508	Decoding slave address unsigned value failed
	123509	Decoding number of bytes unsigned value failed
	123510	Bus ID out of range
	123511	Number of bytes out of range
Example	DS:> 1235 0 0xa0 0xf 1 0 0x0000: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0008:0x00 0x00 0x00 0x00 0x00 0x00 0x00 121000: Test OK @	

Nucleus Name	**DS_SYS_UartSetup**
Nucleus Number	1236
Description	Set up a configuration for the selected UART
Technical	- Parse user input - Use MIS_UART_Setup to setup the selected UART with the requested parameters
Execution Time	Less than 1 second

User Input	The user inputs 6 parameters: <UartNr><baudrate><flowcontrol><databits><parity><stopbits> UartNr: 1=UART port 1 : not used (Chrysalis only) 2=UART port 2 : Bit Engine or DTTM (Chrysalis only) 3=UART port 3 : Analogue board baudrate: 115200,62500,57600,38400,19200,9600,4800,2400,1200 flowcontrol: 0=disabled 1=enabled databits: 7 or 8 parity: "NO", "ODD" or "EVEN" stopbits: 1 or 2	
Error	Number	Description
	123600	Setting up the selected UART succeeded
	123601	User provided Invalid setup parameters
	123602	Setting up the selected UART Failed
	123603	Selected UART is not available
Example (Chrysalis)	DS:> 1236 2 38400 0 8 NO 1 123600: Test OK @	
Example (Leco)	DS:> 1236 2 38400 0 8 NO 1 123603: The selected UART is not available Error @	

Electronic Program Guide Board (EPGB)

Nucleus Name	**DS_EPGB_VersionGet**	
Nucleus Number	1300	
Description	Returns the version of the EPG board.	
Technical	- Issue the command to get the version of the EPG board to the analogue board - Return the received information to the user	
Execution Time	3 seconds.	
User Input	None	
Error	Number	Description
	130000	Getting the version succeeded
	130001	Communication with the analog board failed.
	130002	Communication with the EPG board failed.
	130003	There was no response from the analogue board.
	130004	No DS error code known for analogue board error.
Example	DS:> 1300 130000: Version : 6.1.9 Test OK @	

ANALOGUE SLAVE PROCESSOR (ASP)

Nucleus Name	**DS_ASP_Communication**	
Nucleus Number	1600	
Description	This nucleus checks the communication between the IIC controller of the Codec and the ASP.	
Technical	- Initialise IIC-bus. - Read something from ASP. - Handle the errorcode.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	160000	Communicating with the ASP succeeded
	160001	The IIC bus was not accessible
	160002	There was a timeout reading the device
	160003	The IIC acknowledge was not received
	160004	An IIC-bus error occurred
	160005	Got unknown IIC bus error

	160006	The IIC bus initialisation failed
Example	DS:> 1600 160000: Test OK @	

Nucleus Name	**DS_ASP_Version**	
Nucleus Number	1601	
Description	This nucleus returns the version number of the software running on the ASP and if available that of the display driver.	
Technical	Read versions from ASP and display it.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	160100	Retrieving the software versions succeeded
	160101	The IIC bus initialisation failed.
	160102	The IIC bus failed.
	160103	The CRC checksum of the message is wrong.
Example	DS:> 1601 160100: Software version : 0.9 Display driver version: 0.1 Hardware version : 0x02 Hardware layout : 0x03 Hardware revision : 0x00 Test OK @	

Nucleus Name	**DS_ASP_RealTimeClockSetValues**	
Nucleus Number	1602	
Description	This nucleus is used to set the real time clock to the correct values.	
Technical	- Decode the user input. - Write RTC value to ASP.	
Execution Time	Less than 1 second.	
User Input	User must give time and date like this: hh:mm:ss dd/mm/yy	
Error	Number	Description
	160200	Setting the real time clock succeeded
	160201	The ASP initialisation failed.
	160202	The IIC bus failed.
	160203	Wrong user input.
Example	DS:> 1602 03:20:01 22/06/03 160200: Test OK @	

Nucleus Name	**DS_ASP_RealTimeClockGetValues**	
Nucleus Number	1603	
Description	This nucleus is used to retrieve the actual real time from the ASP	
Technical	- Read RTC value from ASP. - Decode the RTC value.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	160300	Retrieving the real time succeeded
	160301	The ASP initialisation failed.
	160302	The IIC bus failed.
	160303	The CRC checksum of the message is wrong.
	160304	The Real Time Clock has been found invalid and thus set to default values.
Example	DS:> 1603 Time: 03:20:17 Date: 22/06/03 (dd/mm/yy) 160300: Test OK @	

Nucleus Name	**DS_ASP_RealTimeClockSetCorrection**
Nucleus Number	1604
Description	This nucleus sets the correction value needed for the real time clock

Technical	T.B.D. !!	
Execution Time	Less than 1 second.	
User Input	none	
Error	Number	Description
	160400	Setting the correction values succeeded
Example	DS:> 1604 160400: T.B.D. !! Test OK @	

Nucleus Name	**DS_ASP_RealTimeClockAdjustment**	
Nucleus Number	1605	
Description	This nucleus sets a test signal for clock crystal measurement. The signal with a frequency of 1 kHz and duty cycle of 50% appears on pin RCC.	
Technical	Send Clock Adjustment command to the ASP.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	160500	The test succeeded
	160501	The ASP initialisation failed.
	160502	The IIC bus failed.
Example	DS:> 1605 160500: Test OK @	

Nucleus Name	**DS_ASP_NTCGet**	
Nucleus Number	1606	
Description	This nucleus reads the value of the NTC-resistor connected to the ASP, which tells the ambient temperature to the processor.	
Technical	- Read the ADC input pin of the ASP that is connected to the NTC-resistor. - Display this value.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	160600	Getting the NTC-value succeeded
	160601	The IIC bus failed
Example	DS:> 1606 160600: Temperature(NTC) ADC input value = 0x94 Test OK @	

Nucleus Name	**DS_ASP_FanSpeedSet**	
Nucleus Number	1607	
Description	This nucleus sets the speed of the fan that controls the temperature within the set.	
Technical	- Decode user input. - Set pio-pins FAN_C1 and FAN_C2.	
Execution Time	Less than 1 second.	
User Input	Speed to be set: off, low, medium, high	
Error	Number	Description
	160700	Setting the new fan speed succeeded
	160701	The IIC bus failed
	160702	The user provided wrong input
Example	DS:> 1607 low 160700: Test OK @	

Nucleus Name	**DS_ASP_LightDisplay**	
Nucleus Number	1608	
Description	This nucleus lights the entire display.	
Technical	- Set all segments on in the display buffer. - Set the grids correct in the display buffer. - Send the display buffer to the ASP.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	160800	Lighting the entire display succeeded

	160801	IIC-bus communication failed
Example	DS:> 1608 160800: Test OK @	

Nucleus Name	**DS_ASP_BlinkDisplay**	
Nucleus Number	1609	
Description	This nucleus lights the entire display, and lets it blink.	
Technical	- Set all segments on in the blink buffer. - Set the grids correct in the blink buffer. - Send the blink buffer to the ASP.	
Execution Time	Less than 1 second.	
User Input	None or on to start the blinking of the display. off To stop the blinking of the display.	
Error	Number	Description
	160900	The test succeeded
	160901	IIC-bus communication failed
	160902	The user provided wrong input
Example	DS:> 1609 160900: Test OK @ DS:> 1609 off 160900: Test OK @	

Nucleus Name	**DS_ASP_DimmingDisplay**	
Nucleus Number	1610	
Description	This nucleus lights the entire display, and dims it.	
Technical	Change in a loop the display brightness from maximum to minimum.	
Execution Time	Less than 1 second.	
User Input	ON or OFF	
Error	Number	Description
	161000	The test succeeded
	161001	IIC-bus communication failed
	161002	The user provided wrong input
Example	DS:> 1610 ON 161000: Test OK @	

Nucleus Name	**DS_ASP_ClearDisplay**	
Nucleus Number	1611	
Description	This nucleus clears the display and deactivates dimming/blinking functionality	
Technical	- Make the display buffer empty. - Make the blink buffer empty. - Send the display buffer to the ASP. - Send the blink buffer to the ASP.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	161100	The test succeeded
	161101	IIC-bus communication failed
Example	DS:> 1611 161100: Test OK @	

Nucleus Name	**DS_ASP_KeyBoard**
Nucleus Number	1612
Description	This nucleus checks all keys of the keyboard by having the user confirm the key-code displayed of all keys. If the user presses a or A the test is aborted. If the user presses o or O the test is indicated as OK. If the user holds down PLAY for more than a second the test is indicated as OK, if the user holds down RECORD the test is indicated as failed.

Technical	- Initialise the display. - Display the key pressed by the user on the display. - Monitor the service port for an abort and get the next key pressed. - Update the display and repeat previous steps until user stops / confirms. - Display the number of keys that were pressed.	
Execution Time	Depends on the user.	
User Input	None	
Error	Number	Description
	161200	Checking all keys succeeded
	161201	IIC-bus communication failed
	161202	The user signals a failure of the keyboard
	161203	The user aborted the test
Example	DS:> 1612 161200: Test OK @	

Nucleus Name	**DS_ASP_RemoteControl**	
Nucleus Number	1613	
Description	This nucleus checks the interface to the remote control by having the user confirm the key-code displayed. At least one key must be tested. If the user presses a or A the test is aborted. If the user presses o or O the test is indicated as OK. If the user holds down PLAY for more than a second the test is indicated as OK, if the user holds down RECORD the test is indicated as failed.	
Technical	- Initialise the display. - Display the key pressed by the user on the display. - Monitor the service port for an abort and get the next key pressed. - Update the display and repeat previous steps until user stops / confirms. - Display the number of keys that were pressed.	
Execution Time	Depends on the user.	
User Input	None	
Error	Number	Description
	161300	The test succeeded
	161301	IIC-bus communication failed
	161302	The user signals a failure of the remote control
	161303	The user aborted the test
Example	DS:> 1613 161300: Test OK @	

Nucleus Name	**DS_ASP_LEDsOn**	
Nucleus Number	1614	
Description	This nucleus switches on the RECORD, TRAY, and EPG-LED, when available	
Technical	- Check if the analogue board is a MOBO board, if so: - Read the ASP pio port. - Set the RECORD-LED bit on in this port. - Write the ASP pio port. - Read the ASP pio port. - Set the TRAY-LED bit on in this port. - Write the ASP pio port. - Read the ASP pio port. - Set the EPG-LED bit on in this port. - Write the ASP pio port. - Else - Set the RECORD-LED bit on. - Write the external ASP pio port. - Set the TRAY-LED bit on. - Write the external ASP pio port. - Set the EPG-LED bit on. - Write the external ASP pio port.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	161400	Switching on the LEDs succeeded
	161401	IIC-bus communication failed
Example	DS:> 1614 161400: Test OK @	

Nucleus Name	**DS_ASP_LEDsOff**	
Nucleus Number	1615	
Description	This nucleus switches off the RECORD, TRAY, and EPG-LED, when available	
Technical	- Check if the analogue board is a MOBO board, if so: - Read the ASP pio port. - Set the RECORD-LED bit off in this port. - Write the ASP pio port. - Read the ASP pio port. - Set the TRAY-LED bit off in this port. - Write the ASP pio port. - Read the ASP pio port. - Set the EPG-LED bit off in this port. - Write the ASP pio port. - Else - Set the RECORD-LED bit off. - Write the external ASP pio port. - Set the TRAY-LED bit off. - Write the external ASP pio port. - Set the EPG-LED bit off. - Write the external ASP pio port.	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	161500	Switching off the LEDs succeeded
	161501	IIC-bus communication failed
Example	DS:> 1615 161500: Test OK @	

Nucleus Name	**DS_ASP_Reset**	
Nucleus Number	1616	
Description	This nucleus resets the ASP.	
Technical	- Reset the ASP by toggling the reset wire by a GPIO pin of the codec. - Wait 500ms according to the HSI.-Read Status from ASP. - Put ASP in normal mode.-Configure general ASP PIO. - Make a ASP pio pin low to read the version. - Get GPP40 - GPP47 and GPP48 - GPP55. - Decode hardware version, revision, and layout. - Configure the ASP clock. - Configure display, part 1. - Configure display, part 2. - Configure blinking. - Configure external ASP PIO. - Configure ADC input. - Configure remote control input. - Enable power on the AV3.	
Execution Time	3 seconds.	
User Input	None	
Error	Number	Description
	161600	Reset command succeeded
	161601	IIC-bus communication failed
Example	DS:> 1616 161600: Test OK @	

ANALOGUE BOARD EEPROM (AROM)

Nucleus Name	**DS_AROM_Communication**	
Nucleus Number	1700	
Description	Check the communication between the IIC controller of the Codec and the EEPROM	
Technical	- Initialise IIC - Read from a location in AROM	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	170000	Something is properly read so the communication is OK
	170001	The IIC bus was not accessible
	170002	There was a timeout reading the device

	170003	The IIC acknowledge was not received
	170004	The communication with the device failed
	170005	The IIC bus failed
	170006	The IIC bus initialisation failed
Example	DS:> 1700 170000: Test OK @	

VIDEO MATRIX (VMIX)

Nucleus Name	**DS_VMIX_Communication**	
Nucleus Number	1800	
Description	This nucleus checks the communication between the IIC controller of the Codec and the Video Matrix on the analogue board	
Technical	Try to read anything from the video matrix by means of IIC	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	180000	Communicating wit the Video Matrix succeeded
	180001	An IIC-bus error occurred
	180002	There was a timeout reading the device
	180003	The IIC bus was not accessible
	180004	The IIC acknowledge was not received
	180005	There was an IIC error upon the stop-condition
	180006	The IIC bus was chosen wrong
	180007	The IIC functionality is not running
	180008	An unknown error was returned
Example	DS:> 1800 180000: Test OK @	

Nucleus Name	**DS_VMIX_Routing**	
Nucleus Number	1801	
Description	This nucleus performs the routing of the video signals in the set. It sets the video path according to the user input.	
Technical	- Determine whether the set is NAFTA/APAC or EUROPE - Switch the videomatrix according to the input specified by the user	
Execution Time	Less than 1 second.	
User Input	The user inputs the path Id of choice, as specified in tables below for Europe/NAFTA-APAC	
Error	Number	Description
	180100	Routing the video path succeeded
	180101	The user provided wrong input
	180102	There was no response from the video matrix
	180103	Could not retrieve region from analogue slave processor
Example	DS:> 1801 00 180100: Test OK @	

Table 5-3 Available VIDEO path-Ids for EUROPE routing

EURO Path ID	Description
	(DbOut=Digital Board Output, DbIn = Digital Board Input)
00	DbOut-CVBS/YC/RGB to RearOut-CVBS/YC and Scart_1-RGB.
01	- DbOut-CVBS to RearOut-CVBS. - FrontIn-CVBS to DbIn-CVBS.
02	- DbOut-YC to RearOut-YC. - FrontIn-YC to DbIn-YC.
03	- DbOut-CVBS to Scart_1-CVBS. - Scart_2-CVBS to DbIn-CVBS.
04	- DbOut-YC to Scart_1-YC. - Scart_2-YC to DbIn-YC.
05	- DbOut-RGB to Scart_1-RGB. - Scart_2-RGB to DbIn-RGB.
06	- DbOut-CVBS to RearOut-CVBS. - Tuner-CVBS to DbIn-CVBS.
07	DbOut-CVBS to DbIn-CVBS.
08	DbOut-PSCAN to RearOut-YUV.
09	DbOut-YUV to RearOut-YUV.
10	- DbOut-CVBS to Scart_2-CVBS. - Scart_1-CVBS to DbIn-CVBS.
11	- DbOut-YC to Scart_2-YC. - Scart_1-YC to DbIn-YC.
12	Scart_2-RGB to Scart_1-RGB.
13	Scart_2-CVBS to Scart_1-CVBS.
14	Scart_1-CVBS to Scart_2-CVBS.

Table 5-4 Available VIDEO path-Ids for NAFTA / APAC routing

NAFTA Path ID	Description
	(DbOut=Digital Board Output, DbIn = Digital Board Input)
00	DbOut-CVBS/YC/YUV to RearOut-CVBS/YC/YUV.
01	- DbOut-CVBS to RearOut-CVBS. - FrontIn-CVBS to DbIn-CVBS.
02	- DbOut-YC to RearOut-YC. - FrontIn-YC to DbIn-YC.
03	- DbOut-CVBS to RearOut-CVBS. - RearIn-CVBS to DbIn-CVBS.
04	- DbOut-YC to RearOut-YC. - RearIn-YC to DbIn-YC.
05	- DbOut-YUV to RearOut-YUV. - RearIn-YUV to DbIn-YUV.
06	- DbOut-CVBS to RearOut-CVBS. - Tuner-CVBS to DbIn-CVBS.
07	DbOut-CVBS to DbIn-CVBS.
08	DbOut-PSCAN to RearOut-YUV.

AUDIO MATRIX (SOUND PROCESSOR) (AMIX)

Nucleus Name	**DS_AMIX_Communication**	
Nucleus Number	1900	
Description	This nucleus checks the communication between the IIC controller of the Codec and the Audio Matrix (sound processor) on the analogue board	
Technical	Test whether anything can be read from the sound processor	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	190000	Communicating wit the Audio Matrix succeeded
	190001	An IIC-bus error occurred
	190002	There was a timeout reading the device
	190003	The IIC bus was not accessible
	190004	The IIC acknowledge was not received
	190005	There was an IIC error upon the stop-condition
	190006	The IIC bus was chosen wrong
	190007	The IIC functionality is not running

	190008	An unknown error was returned
Example	DS:> 1900 190000: Test OK @	

Nucleus Name	**DS_AMIX_Routing**	
Nucleus Number	1901	
Description	This nucleus performs the routing of the audio signals in the set. It sets the audio path according to the user input.	
Technical	- Determine whether the set is of type NAFTA-APAC or EUROPE - Parse the user input to determine the routing - According to parameters set the sound processor and multiplexers	
Execution Time	Less than 1 second.	
User Input	The user inputs the path ID of his/her choice, as specified in tables below for Europe/ NAFTA	
Error	Number	Description
	190100	Routing the audio path succeeded
	190101	Routing the audio path failed
	190102	There was an error resetting the sound processor
	190103	The user provided wrong input
	190104	There was no response from the ASP
Example	DS:> 1901 00 190100: Test OK @	

Table 5-5 *Available AUDIO path-Ids for* ***EUROPE*** *routing*

EURO Path ID	Description
	(DbOut=Digital Board Output, DbIn = Digital Board Input)
00	DbOut to All Outs.
01	- DbOut to RearOut for CVBS/YC, and RearOut for YUV. - FrontIn to DbIn.
02	- DbOut to Scart_1-AOut. - Scart_2-AIn to DbIn.
03	- DbOut to Scart_2-AOut. - Scart_1-AIn to DbIn.
04	- DbOut to RearOut for CVBS/YC. - Tuner to DbIn.
05	DbOut to RearOut-5.1.
06	DbOut to DbIn
07	Scart_2-AIn to Scart_1-AOut.
08	Scart_1-AIn to Scart_2-AOut.

Table 5-6 *Available AUDIO path-Ids for* ***NAFTA/APAC*** *routing*

NAFTA Path ID	Description
	(DbOut=Digital Board Output, DbIn = Digital Board Input)
00	DbOut to All Outputs.
01	- DbOut to RearOut for CVBS/YC, and RearOut for YUV. - FrontIn to DbIn.
02	- DbOut to RearOut for CVBS/YC, and RearOut for YUV. - RearIn1 (EXT2) for CVBS/YC to DbIn.
03	- DbOut to RearOut for CVBS/YC, and RearOut for YUV. - RearIn2 (EXT1) for YUV to DbIn.
04	- DbOut to RearOut for CVBS/YC, and RearOut for YUV. - Tuner to DbIn.
05	DbOut to RearOut-5.1.
06	DbOut to DbIn.

Nucleus Name	**DS_AMIX_VersionGet**
Nucleus Number	1902
Description	This nucleus gets the version information from the sound processor.
Technical	Read the information from the sound processor using IIC
Execution Time	Less than 1 second
User Input	-

Error	Number	Description
	190200	Getting the version info from the sound processor succeeded
	190201	Getting the version info from the sound processor failed
Example	DS:> 1902 Hardware Version:0x 2, Revision Code :0x 7 MSP Product Code:0x19, ROM Version Code:0x48 190200: Test OK @	

Nucleus Name	**DS_AMIX_Control**	
Nucleus Number	1903	
Description	Test the controllability of the sound processor by performing a controlled reset	
Technical	Test the control register, contains 0x80 after reset and 0x0 after first read of this control register. MSP is reset and the control register is tested for the 0x80 reset indication	
Execution Time	1 second	
User Input	-	
Error	Number	Description
	190300	Testing the controllability succeeded
	190301	Accessing the MSP failed
	190302	Accessing the MSP succeeded, but wrong data was returned
Example	DS:> 1903 190300: Test OK @	

Note	**European sets only !!**	
Nucleus Name	**DS_AMIX_Beep**	
Nucleus Number	1904	
Description	Test the beeper functionality of the sound processor	
Technical	-	
Execution Time	3 seconds	
User Input	-	
Error	Number	Description
	190400	Testing the beeper succeeded
	190401	Testing the beeper failed
	190402	There was an error routing the test path
	190402	The user provided the wrong input
Example	DS:> 1904 ON 190400: Test OK @	

Nucleus Name	**DS_AMIX_CommunicationAdcDac**	
Nucleus Number	1906	
Description	This nucleus checks the communication between the IIC controller of the Codec and the ADC/DAC chip (UDA 1380) on the analogue board	
Technical	Test whether anything can be read from the ADC/DAC	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	190600	Communicating with the ADC/DAC succeeded
	190601	The IIC bus was not accessible
	190602	There was a timeout reading the device
	190603	The IIC acknowledge was not received
	190604	An IIC-bus error occurred
	190605	Got unknown IIC bus error
	190606	The IIC bus initialisation failed
Example	DS:> 1906 190600: Test OK @	

Nucleus Name	**DS_AMIX_Mute**
Nucleus Number	1907
Description	Set or unset the master mute of the ADC/DAC chip (UDA 1380) on the analogue board

Technical	Send the master mute command via IIC	
Execution Time	Less than 1 second.	
User Input	'ON' or 'OFF'	
Error	Number	Description
	190700	Muting the sound processor succeeded
	190701	Muting sound processor failed
Example	DS:> 1907 190700: Test OK @	

FRONTEND TUNER (FRE)

Nucleus Name	**DS_FRE_Communication**	
Nucleus Number	2000	
Description	This nucleus checks the communication between the IIC controller of the Codec and the Front End (Tuner) on the analogue board	
Technical	Determine whether anything can be read from the FRE through IIC	
Execution Time	Less than 1 second.	
User Input	None	
Error	Number	Description
	200000	Communicating with the front end succeeded
	200001	The IIC bus was not accessible
	200002	There was a timeout reading the device
	200003	The IIC acknowledge was not received
	200004	An IIC-bus error occurred
	200005	Got unknown IIC bus error
	200006	The IIC bus initialisation failed
Example	DS:> 2000 200000: Test OK @	

Nucleus Name	**DS_FRE_ChannelSelect**	
Nucleus Number	2001	
Description	This nucleus sets the tuner to receive a valid audio and video signal	
Technical	-Parse the user input to determine all parameters to set -Pass these parameters to the respective parts using IIC	
Execution Time	Less than 1 second	
User Input	<Frequency*16> <video standard id> <Tuner> Tuner frequency: to tune the tuner to e.g. 216 MHz, this parameter must be 3456. (Since 216*16 = 3456. This is to avoid the decimal points to the parameter list.) Name Colour system Transmission standard Sound modulation PAL_BG_S PAL BG FM-Stereo PAL_BG_M PAL BG FM-Mono / NICAM PAL_I_M PAL I FM-Mono / NICAM PAL_DK_S PAL DK FM-Stereo PAL_DK_M PAL DK FM-Mono / NICAM NTSC_M_S NTSC M FM-Stereo Video Standard ID: The table below shows which video standards are possible ID Europe NAFTA / APAC 0 PAL_BG_S NTSC 1 PAL_BG_M Invalid 2 PAL_I_M Invalid 3 PAL_DK_S Invalid 4 PAL_DK_M Invalid Tuner: Select the tuner type that you want to tune. This input is not mandatory. (If no input is detected, tuner will be defined run-time (if recognised).) Tuner Tuner ID 1 FE1316 (Europe Philips) 2 FE1319 (Europe Philips) 3 TMQZ2-403A (Europe ALPS) 4 JS6B2-L121 (Europe Xuguang) 5 TCPK0601 (APAC Samsung) 6 TCMN0682 (NAFTA Samsung)	
Error	Number	Description
	200100	Setting the tuner channel succeeded
	200101	Invalid user input

Nucleus Name	**DS_FRE_ChannelSelect**	
	200102	Getting the version of the set failed
	200103	Configuration of the tuner failed
	200104	Configuration of the IF module failed
Example	DS:> 2001 3456 0 1200100: Test OK @	

Nucleus Name	**DS_FRE_AFCReferenceVoltage**	
Nucleus Number	2002	
Description	This nucleus stores the reference voltage for the tuner in the factory settings	
Technical	- Parse the user input - Initialise IIC and NVRAM-connection - Put the new values in NVRAM	
Execution Time	Less than 1 second.	
User Input	The reference voltage to store, in a range between 0 and 255. (dec.)	
Error	Number	Description
	200200	Storing the reference voltage for the tuner succeeded
	200201	The user provided wrong input
	200202	The section in NVRAM could not be validated after write
	200203	Writing the value to NVRAM failed
	200204	Initialisation of IIC failed or NVRAM unreachable
Example	DS:> 2002 0xaa 200200: Test OK @	

Note	**European sets only!!**	
Nucleus Name	**DS_FRE_CommunicationIfModule**	
Nucleus Number	2003	
Description	This nucleus checks the communication with the IF(Intermediate Frequency) module of the front end	
Technical	Determine whether the IF module can be read through IIC	
Execution Time	Less than 1 second	
User Input	-	
Error	Number	Description
	200300	Communicating with the front end succeeded
	200301	The IIC bus was not accessible
	200302	There was a timeout reading the device
	200303	The IIC acknowledge was not received
	200304	An IIC-bus error occurred
	200305	Got unknown IIC bus error
	200306	The IIC bus initialisation failed
	200307	Not a Europe set
Example	DS:> 2003 200300: Test OK @	

Nucleus Name	**DS_FRE_TunerTypeGet**	
Nucleus Number	2004	
Description	This nucleus retrieves the tuner type information and translates this to the region involved as well.	
Technical	- Check the region through the ASP - Read out the tuner type through IIC	
Execution Time	Less than 1 second	
User Input	-	
Error	Number	Description
	200400	Getting the tuner type information succeeded
	200401	Getting the type of the tuner OK, but unknown type returned
	200402	Getting the tuner type information failed
Example	DS:> 2004 200400: NAFTA Tuner: TCMN0682 Test OK @	

SCRIPT

Nucleus Name	**DS_IH_ScriptHandler**
Nucleus Number	Script
Description	The test requires no user interaction. A number of nuclei will be run before a message is returned indicating if there is a failure in the DVD Recorder. When a nucleus failed, the script stops and displays the message "**FAIL**". Otherwise it displays "**PASS**" at the end when all nuclei are executed. During the execution of a script, a progress indicator is displayed on the display of the DVD Recorder.
Technical	Execute the included nuclei one by one If a nucleus fails quit and display the failed nucleus on the local display and service port
Execution Time	16 seconds
Included tests:	1. DS_ANAB_COMMUNICATIONECHO_NUC 2. DS_DCB_COMMUNICATIONECHO_NUC 3. DS_BROM_COMMUNICATION_NUC 4. DS_SYS_SETTINGSDISPLAY_NUC 5. DS_CHR_DEVTYPEGET_NUC 6. DS_CHR_INT_PIC_NUC 7. DS_CHR_DMA_NUC 8. DS_BROM_WRITEREAD_NUC 9. DS_NVRAM_COMMUNICATION_NUC 10. DS_NVRAM_WRITEREAD_NUC 11. DS_SDRAM_WRITEREADFAST_NUC 12. DS_FLASH_WRITEREAD_NUC 13. DS_FLASH_CHECKSUMPROGRAM_NUC 14. DS_SYS_HARDWAREVERSIONGET_NUC 15. DS_VIP_DEVTYPEGET_NUC 16. DS_VIP_COMMUNICATION_NUC 17. DS_DVIO_LINKDEVTYPEGET_NUC 18. DS_DVIO_PHYDEVTYPEGET_NUC 19. DS_DVIO_LINKCOMMUNICATION_NUC 20. DS_DVIO_PHYCOMMUNICATION_NUC 21. DS_PSCAN_COMMUNICATIONDENC_NUC 22. DS_PSCAN_COMMUNICATIONDEINTERLACER_NUC 23. DS_BE_COMMUNICATIONECHO_NUC 24. DS_ANAB_COMMUNICATIONIICNVRAM_NUC 25. DS_ANAB_COMMUNICATIONIICTUNER_NUC 26. DS_ANAB_COMMUNICATIONIICSOUNDPROCESSOR_NUC 27. DS_ANAB_COMMUNICATIONIICAVSELECTOR_NUC 28. DS_ANAB_CHECKSUMPROGRAM_NUC
Note!	**Invocation by holding down the PLAY button when powering up the system**
Note!	The following example is for a generation 2.1 DVD+RW recorder. The variant you test may behave differently. For a detailed description of the script-behaviour of your variant under test refer to the [RW2_1_SWA_DS].

Example

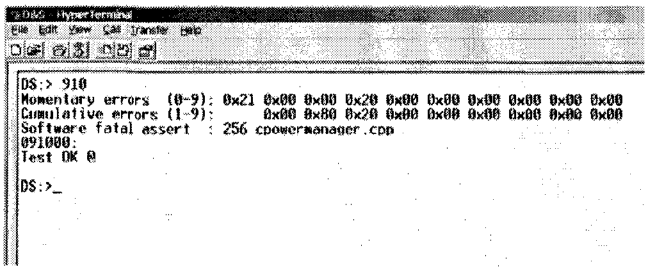
```
DS:> script
Executing User/Dealer script.
Busy executing NUC1100 1-28
Hello Analogue Board
Busy executing NUC1000 2-28
Busy executing NUC200 3-28
Busy executing NUC1228 4-28
Settings ID: 4C4541440D00000000030300010101020101000020080000
Board name: LEAD
Hardware ID: 0
Codec IC: PNX7100_MF3
Video Input Processor IC: SAA7118
Progressive Scan Deinterlacer IC: None
Progressive Scan Denc IC: ADV7196
I-Link physical layer circuit IC: PDI1394P25
I-Link link layer circuit IC: PDI1394P40
Audio clock: Clock scheme 1
Bit engine connector: available
IDE connector 1: available
IDE connector 2: not available
PCI connector: not available
RAM size 32MByte
ROM size (NOR FLASH bank 1) 8MByte
ROM size (NOR FLASH bank 2) Not available
ROM size (NAND FLASH) Not available
Bit Engine: AV 2.0
```

Example

```
Busy executing NUC100 5-28
Device ID 7100
Codec ID PNX7100_MF3 F-BCU (0x0102) 1.0 INTC (0x011d) 1.0 PCI-XIO(0x0113) 1.0
SIF (0x013b) 1.0 EJTAG (0x0104) 0.0 S-BCU (0x0102) 1.0
BOOT (0x010a) 1.0 CONFIG (0x013f) 1.0 RESET (0x0123) 1.0
DEBUG (0x0116) 0.0 UART0 (0x0107) 0.1 UART1 (0x0107) 0.1
UART2 (0x0107) 0.1 UART3 (0x0107) 0.1 I2C0 (0x0105) 0.1
I2C1 (0x0105) 0.1 GPIO (0x013c) 1.0 SYNC (0x013a) 1.0
DISP0 (0xa015) 0.2 DISP1 (0xa00f) 0.0 OSD (0x0136) 0.1
SPU (0xa00e) 0.0 MIXER (0x0137) 1.0 DENC (0x0138) 0.1
CCIR (0x0139) 1.0 VDEC (0x0133) 0.1 PARSER (0xa00d) 0.0
DV (0xa00c) 0.0 BEI (0xa00a) 0.0 IDE (0xa009) 0.0
SGDX (0xa008) 0.0 BYTE (0xa00b) 0.0 OUTPUT (0xa003) 0.0
ACOMP (0xa000) 0.0 VFE (0xa001) 0.0 VCOMP (0xa002) 0.0
SCR (0x0000) 0.0 SIFF (0xa011) 0.0 WMD (0xa010) 0.0
AUDIO0 (0xa015) 0.2 AUDIO1 (0xa00f) 0.0 PSCAN (0xa018) 0.0

Busy executing NUC114 6-28

Busy executing NUC115 7-28

Busy executing NUC201 8-28

Busy executing NUC300 9-28

Busy executing NUC301 10-28

Busy executing NUC401 11-28

Busy executing NUC501 12-28

Busy executing NUC503 13-28
BootCode checksum is: 0xBABEB432, which is correct
Diagnostics checksum is: 0xBABED22B, which is correct
Download checksum is: 0xBABE025F, which is correct
Application checksum is: 0xBABE2825, which is correct

Busy executing NUC1200 14-28
Hardware ID = 00
Busy executing NUC600 15-28
Found SAA7118
Busy executing NUC601 16-28
Busy executing NUC700 17-28
Device type of the link layer IC: ffc00301
Busy executing NUC701 18-28
Device type of the phy layer IC: 0
Busy executing NUC702 19-28

Busy executing NUC703 20-28

Busy executing NUC801 21-28

Busy executing NUC808 22-28
The IIC acknowledge was not received, which is correct
Busy executing NUC900 23-28

Busy executing NUC1101 24-28

Busy executing NUC1102 25-28

Busy executing NUC1104 26-28

Busy executing NUC1105 27-28

Busy executing NUC1111 28-28

BootCode checksum is: 0xBABE6240, which is correct
Diagnostics checksum is: 0xBABEDC9A, which is correct
Download checksum is: 0xBABEA6B7, which is correct
Application checksum is: 0xBABE5968, which is correct

PASS
DS:>
```

5.4 DVD Module Error code

With DSW command 910 the set software can retrieve an overview of all occurred engine errors.



```
DS:> 910
Momentary errors  (0-9): 0x21 0x00 0x00 0x20 0x00 0x00 0x00 0x00 0x00 0x00
Cumulative errors (1-9):      0x00 0x80 0x20 0x00 0x00 0x00 0x00 0x00 0x00
Software fatal assert  : 256 cpowermanager.cpp
091000:
Test OK 0

DS:>_
```

5.4.1 Momentary Errors

Byte 0: latest error:

Overview of the BE error codes.

error code	error	meaning
0x00	no_error	No error has occurred
0x01	illegal_command_error	Command not allowed in this state or unknown command
0x02	illegal_parameter_error	Parameter(s) not valid for this command
0x03	command_timeout_error	The maximum execution time for the command has exceeded
0x04	sledge_home_error	The sledge could not be moved home
0x05	sledge_calibration_error	An error occurred during calibration of the sledge
0x06	sledge_unstable_error	The sledge detected unstable control
0x07	speed_timeout_error	Spindle motor could not reach its target speed within timeout
0x08	speed_window_error	Measured spinning speed is not within expected window
0x09	focus_timeout_error	Focus could not be achieved within the timeout
0x0A	focus_retries_error	The amount of focus retries expired
0x0B	focus_agc_error	The focus agc results are out of range
0x0C	radial_timeout_error	Servo didn't get on track within the timeout
0x0D	radial_retries_error	Servo didn't get on track after several retries
0x0E	radial_agc_error	The radial agc results are out of range
0x0F	radial_init_error	Unreliable signal scaling after the radial initialisation
0x10	hf_pll_error	HF-decoder pll could not lock to HF signal
0x11	wobble_pll_error	Wobble pll could not lock to wobble signal
0x12	subcode_timeout_error	Subcode information could not be read
0x13	subcode_notfound_error	Requested subcode item could not be found
0x14	header_timeout_error	Header information could not be read
0x15	adip_timeout_error	Adip information could not be read
0x16	adip_window_error	Adip address was not within expected window
0x17	adip_sync_error	No adip sync was detected
0x18	atip_timeout_error	Atip information could not be read
0x19	atip_notfound_error	Requested atip item could not be found
0x1A	atip_window_error	Atip address was not within expected window
0x1B	atip_sync_error	No atip sync was detected
0x1C	tray_error	Tray could not be closed or opened within the timeout
0x1D	seek_error	The requested seek couldn't be performed within the timeout
0x1E	no_hf_present_error	Attempt to read from a blank area
0x1F	record_error	An error occurred during the recording
0x20	illegal_stopaddress_error	The requested stopaddress with modify-stop-address is not valid
0x21	no_disc_error	No disc is detected
0x22	not_initialised_error	The system is not initialised (e.g. seek on unknown disctype)
0x23	illegal_medium_error	BE detected an unsupported medium during disc recognition
0x24	cd_frequency_error	Measured HF frequency is not within CD frequency range
0x25	dvd_frequency_error	Measured HF frequency is not within DVD frequency range
0x26	reserved(non_existing_bca_error)	Attempt to read non-existing bca information
0x27	reserved(bca_read_error)	An error occurred during reading of bca information
0x28	selftest_error	An error occurred during the selftest of the BE
0x29	i2c_error	The I2C interface does not operate
0x2A	laser_pll_error	Laser control pll did not lock or lost lock on write clock
0x2B	laser_forward_sense_error	Forward sense value didn't change with changing laser power
0x2C	jitter_optimisation_error	An error occurred during optimisation of the jitter
0x2D	tilt_calibration_error	An error occurred during calibration of the tilt frame
0x2E	reserved	
0x2F	frontend_offset_calib_error	The offset in the frontend couldn't be calibrated
0x30	reserved	
0x31	wsg_calculation_error	An error occurred in the calculation of the write strategy
0x32	buffer_overrun_error	The buffer input stream overran the buffer output stream
0x33	return_value_invalid_error	The requested information is not available for this inquiry
0x34	illegal_recording_speed_error	The selected speed is not allowed for a recording on this medium
0x35	opc_media_parameter_error	The media parameters (info in ATIP/ADIP) are invalid or not read
0x36	opc_record_power_error	The final optimum power was not reached
0x37	opc_start_power_low_error	OPC start power too low (optimum power is higher)
0x38	opc_start_power_high_error	OPC start power too high (optimum power is lower)

error code	error	meaning
0x39	opc_power_calculation_error	Error during OPC power calculation (samples are wrong)
0x3A	opc_test_zone_full_error	OPC can't be performed because test zone is full
0x3B	opc_bad_jitter_measurement_error	The jitter measurement during OPC samples readback failed
0x3C	opc_read_samples_error	An error occurred during OPC readback sampling
0x3D	ropc_alpha_overflow_error	The determined value for the optimum power is too high
0x3E	ropc_alpha_ref_current_error	The alpha measurement reference current is wrong (IAN)
0x3F	ropc_alpha_gain_error	The alpha measurement alpha gain is wrong
0x40	beta_over_under_flow_error	During the walking OPC a beta over-/under-flow was detected
0x41	not_enough_calib_points_error	Not enough valid calibration points available for re-calibration
0x42	not_enough_power_error	The calculated power during re-calibration exceeds max power
0x43	illegal_reading_speed_error	The selected speed is not allowed for the requested command
0x44	servo_fatal_error	The actuator dissipation became too high during a servo recovery

This error is overwritten by the next player / inquiry command.

Format of the BE error bytes.

Byte 1 - 9: cumulative errors of previous error occurences. Every individual error has its own bit in the 9-byte structure as described in the drawing below:

byte 1

b7	b6	b5	b4	b3	b2	b1	b0
reserved	FOCUS AGC ERROR	FOCUS RETRIES ERROR	FOCUS TIMEOUT ERROR	RADIAL AGC ERROR	RADIAL RETRIES ERROR	RADIAL TIMEOUT ERROR	RADIAL INIT ERROR

byte 2

TRAY ERROR	reserved	JITTER OPTIMIZATION ERROR	SLEDGE HOME ERROR	SLEDGE UNSTABLE ERROR	SLEDGE CALIBRATION ERROR	TILT SENSOR OFFSET CALIBRATION ERROR	TILT CALIBRATION ERROR

byte 3

RECORD ERROR	SEEK ERROR	NO DISC ERROR	NOT INITIALISED ERROR	ILLEGAL STOPADDRESS ERROR	ILLEGAL PARAMETER ERROR	ILLEGAL COMMAND ERROR	COMMAND TIMEOUT ERROR

byte 4

SERVO FATAL ERROR	reserved	reserved	HF PLL ERROR	NO HF PRESENT ERROR	HEADER TIMEOUT ERROR	SUBCODE NOTFOUND ERROR	SUBCODE TIMEOUT ERROR

byte5

WOBBLE PLL ERROR	ADIP SYNC ERROR	ADIP WINDOW ERROR	ADIP TIMEOUT ERROR	ATIP NOTFOUND ERROR	ATIP SYNC ERROR	ATIP WINDOW ERROR	ATIP TIMEOUT ERROR

byte6

WSG CALCULATION ERROR	DVD FREQUENCY ERROR	CD FREQUENCY ERROR	ILLEGAL RECORDING SPEED ERROR	SPEED WINDOW ERROR	SPEED TIMEOUT ERROR	NON EXISTING BCA ERROR	BCA READ ERROR

byte7

LASER FORWARD SENSE ERROR	NVRAM CHECKSUM UPDATE ERROR	FRONTEND OFFSET CALIBRATION ERROR	LASER PLL ERROR	ILLEGAL READING SPEED ERROR	ILLEGAL MEDIUM ERROR	SELFTEST ERROR	I^2C ERROR

byte8

OPC READ SAMPLES ERROR	OPC BAD JITTER MEASUREMENT ERROR	OPC TEST ZONE FULL ERROR	OPC POWER CALCULATION ERROR	OPC START POWER HIGH ERROR	OPC START POWER LOW ERROR	OPC RECORD POWER ERROR	OPC MEDIA PARAMETER ERROR

byte9

RETURN VALUE INVALID ERROR	BUFFER OVERRUN ERROR	BETA OVER/UNDER FLOW ERROR	NOT ENOUGH CALIB POINTS ERROR	NOT ENOUGH POWER ERROR	ROPC ALPHA GAIN ERROR	ROPC ALPHA REF CURRENT ERROR	ROPC ALPHA OVERFLOW ERROR

These errors are kept in memory until a power down of the drive (e.g. when recorder goes to standby) or reset of the drive.

5.4.2 Cumulative errors

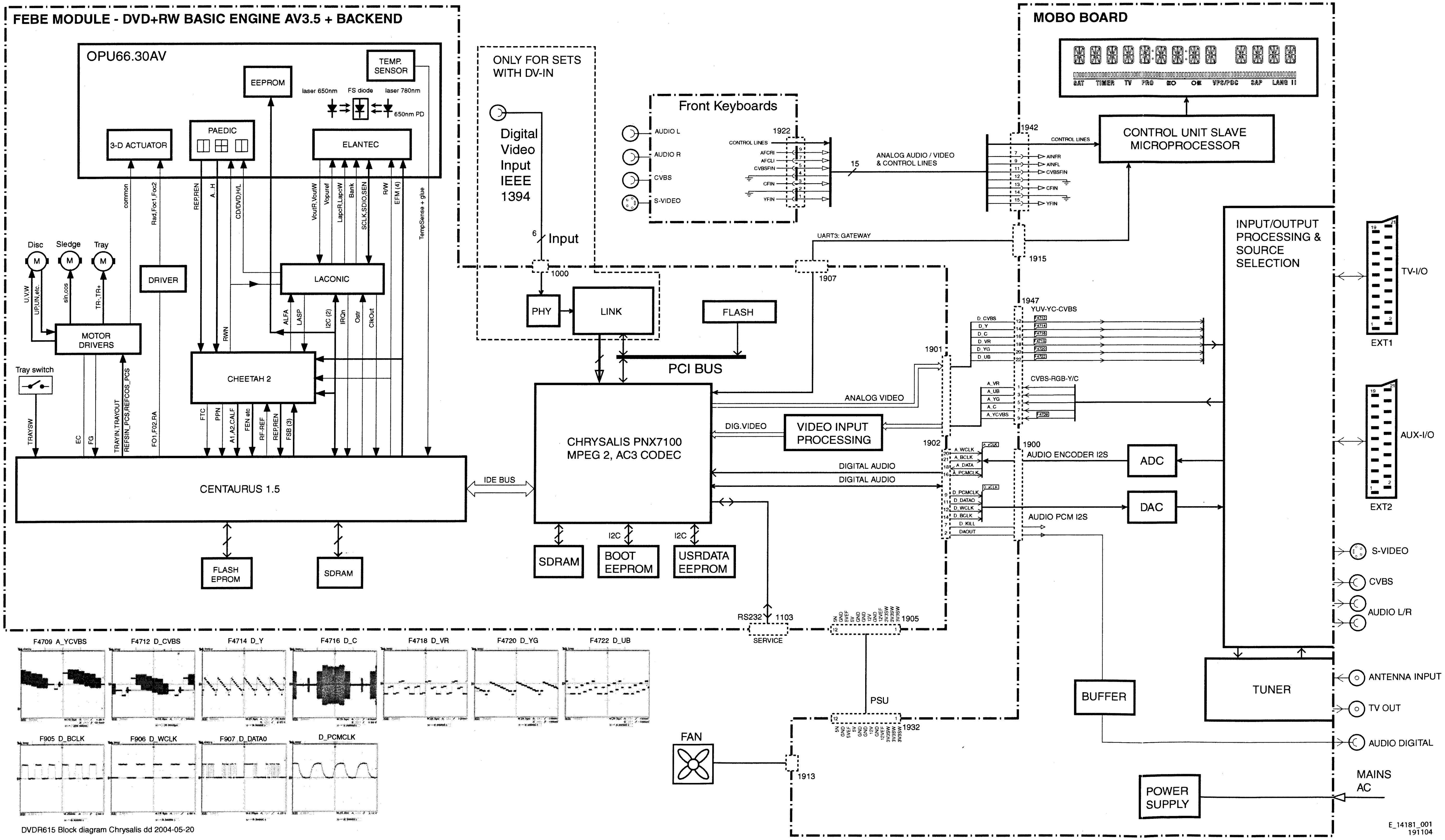
These errors are stored in EEPROM and are thus non-volatile showing the complete error history of the drive.
Byte 1 - 9: cumulative errors of previous player / inquiry error occurences. These bytes are the same as the nine bytes (1-9) of the Momentary errors

5.4.3 Software fatal assert

Gives row number and file name in the source code of the firmware of the data path of the AV3

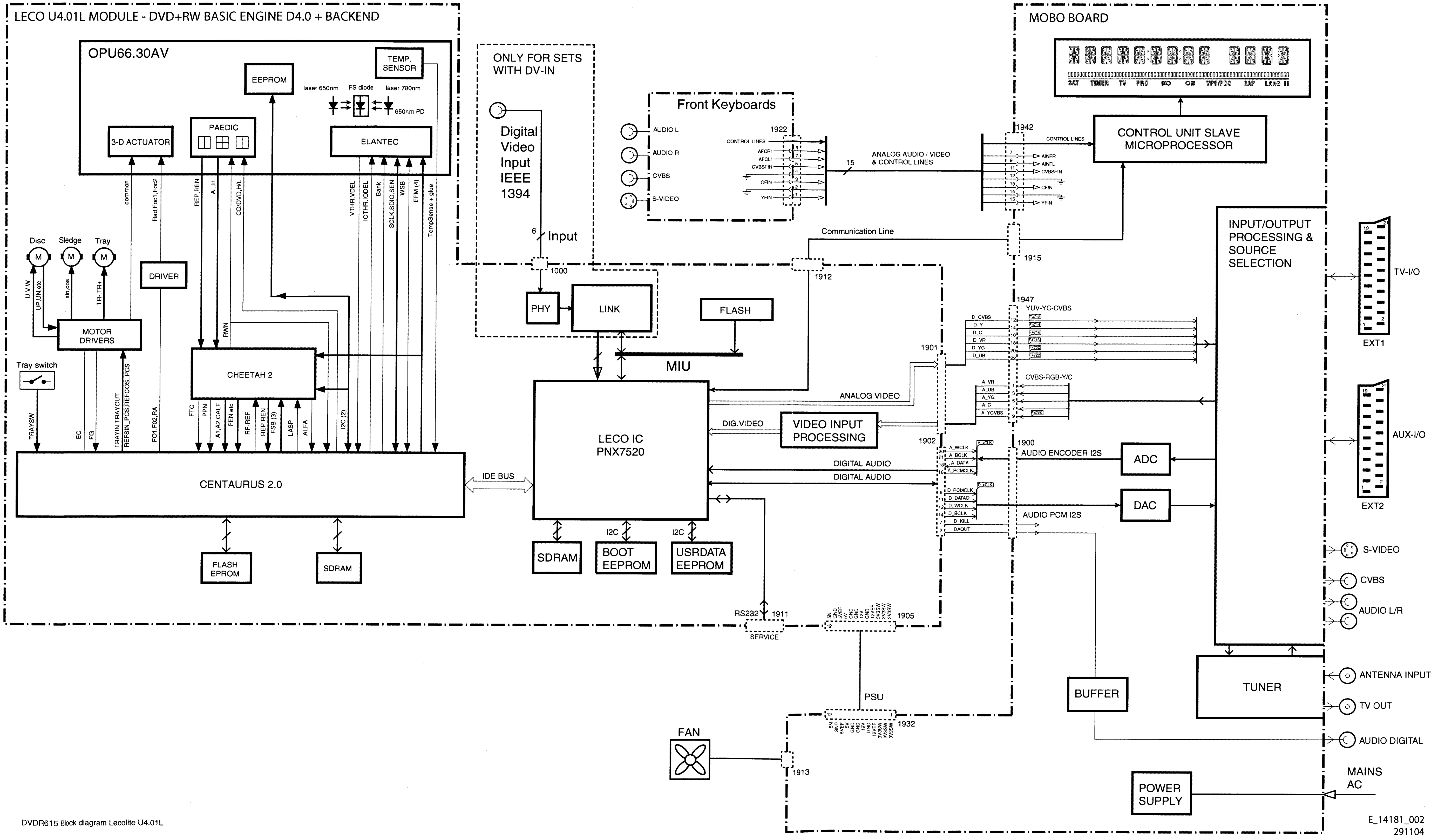
6. Block Diagrams, Waveforms, Wiring Diagram.

Overall Block Diagram of the Set


FEBE MODULE - DVD+RW BASIC ENGINE AV3.5 + BACKEND
OPU66.30AV
EEPROM
TEMP. SENSOR
laser 650nm
FS diode
laser 780nm
650nm PD
3-D ACTUATOR
PAEDIC
ELANTEC
common
Rad,Foc1,Foc2
REP,REN
A..H
CD/DVD,H/L
VoutR,VoutW
Vopuref
LapcR,LapcW
Bank
SCLK,SDIO,SEN
R/W
EFM (4)
TempSense + glue
Disc
Sledge
Tray
U,V,W
UPUN,etc.
sin,cos
TR-,TR+
DRIVER
LACONIC
MOTOR DRIVERS
RWN
ALFA
LASP
I2C (2)
IRQn
Ostr
ClkOut
Tray switch
CHEETAH 2
TRAYSW
EC
FG
TRAYIN,TRAYOUT
REFSIN_PCS,REFCOS_PCS
FO1,F02,RA
FTC
PPN
A1..A2,CALF
FEN etc
RF-REF
REP,REN
FSB (3)
CENTAURUS 1.5
IDE BUS
FLASH EPROM
SDRAM
ONLY FOR SETS WITH DV-IN
Digital Video Input IEEE 1394
6
Input
1000
PHY
LINK
FLASH
PCI BUS
Front Keyboards
AUDIO L
AUDIO R
CVBS
S-VIDEO
1922
CONTROL LINES
AFCRI
AFCLI
CVBSFIN
CFIN
YFIN
15
ANALOG AUDIO / VIDEO & CONTROL LINES
UART3: GATEWAY
1907
1915
CHRYSALIS PNX7100 MPEG 2, AC3 CODEC
ANALOG VIDEO
DIG.VIDEO
VIDEO INPUT PROCESSING
DIGITAL AUDIO
DIGITAL AUDIO
SDRAM
I2C
BOOT EEPROM
I2C
USRDATA EEPROM
RS232
1103
SERVICE
1905
PSU
1932
FAN
1913
MOBO BOARD
SAT TIMER TV PRG MO OK VPS/PDC SAP LANG II
CONTROL UNIT SLAVE MICROPROCESSOR
1942
CONTROL LINES
AINFR
AINFL
CVBSFIN
CFIN
YFIN
1947
YUV-YC-CVBS
D_CVBS
D_Y
D_C
D_VR
D_YG
D_UB
1901
CVBS-RGB-Y/C
A_VR
A_UB
A_YG
A_C
A_YCVBS
1902
1900
A_WCLK
A_BCLK
A_DATA
A_PCMCLK
AUDIO ENCODER I2S
ADC
D_PCMCLK
D_DATAO
D_WCLK
D_BCLK
D_KILL
DAOUT
AUDIO PCM I2S
DAC
INPUT/OUTPUT PROCESSING & SOURCE SELECTION
TV-I/O
EXT1
AUX-I/O
EXT2
S-VIDEO
CVBS
AUDIO L/R
BUFFER
TUNER
ANTENNA INPUT
TV OUT
AUDIO DIGITAL
POWER SUPPLY
MAINS AC
F4709 A_YCVBS
F4712 D_CVBS
F4714 D_Y
F4716 D_C
F4718 D_VR
F4720 D_YG
F4722 D_UB
F905 D_BCLK
F906 D_WCLK
F907 D_DATAO
D_PCMCLK
E_14181_001 191104

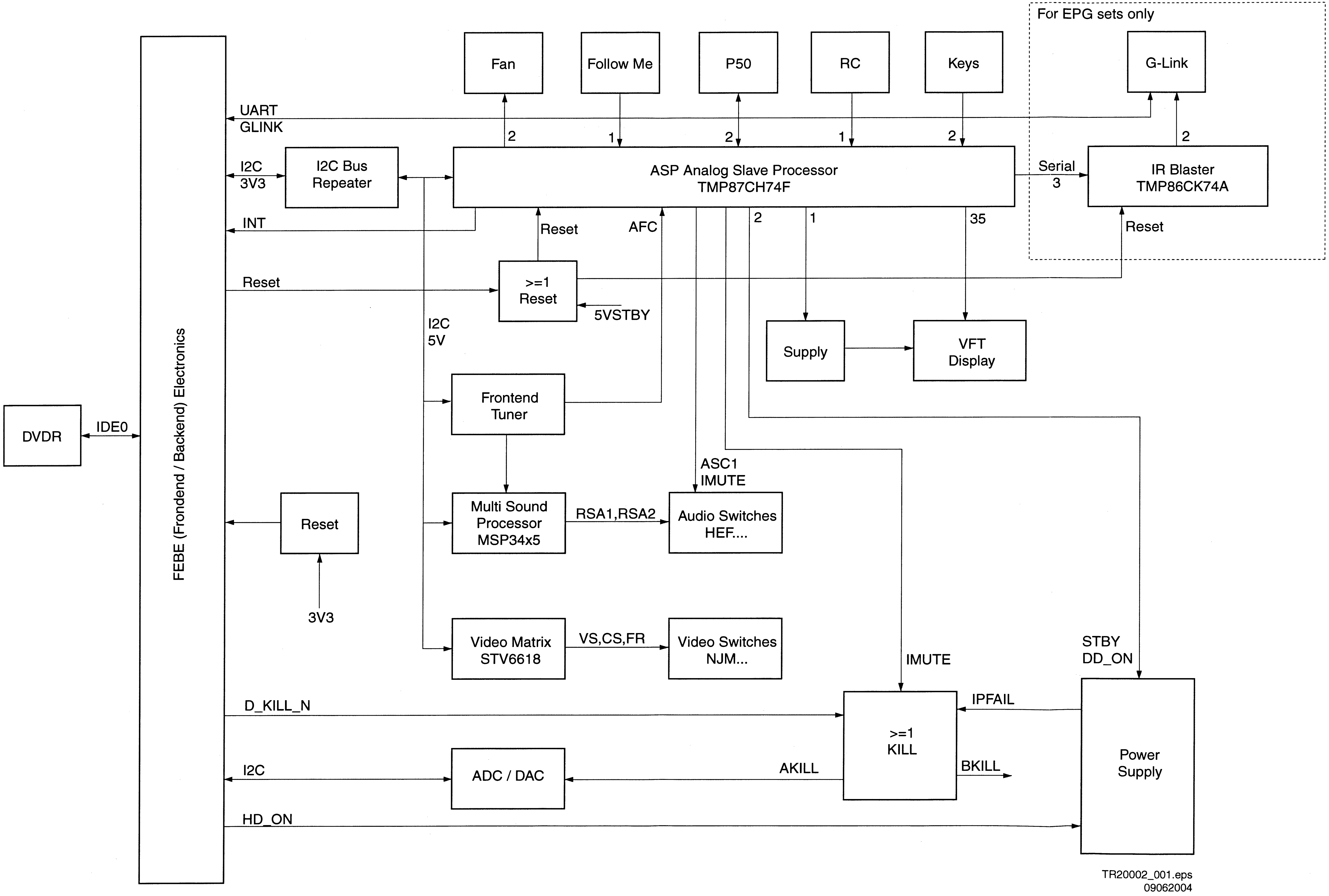
DVDR615 Block diagram Chrysalis dd 2004-05-20

Overall Blockdiagram Lecolite

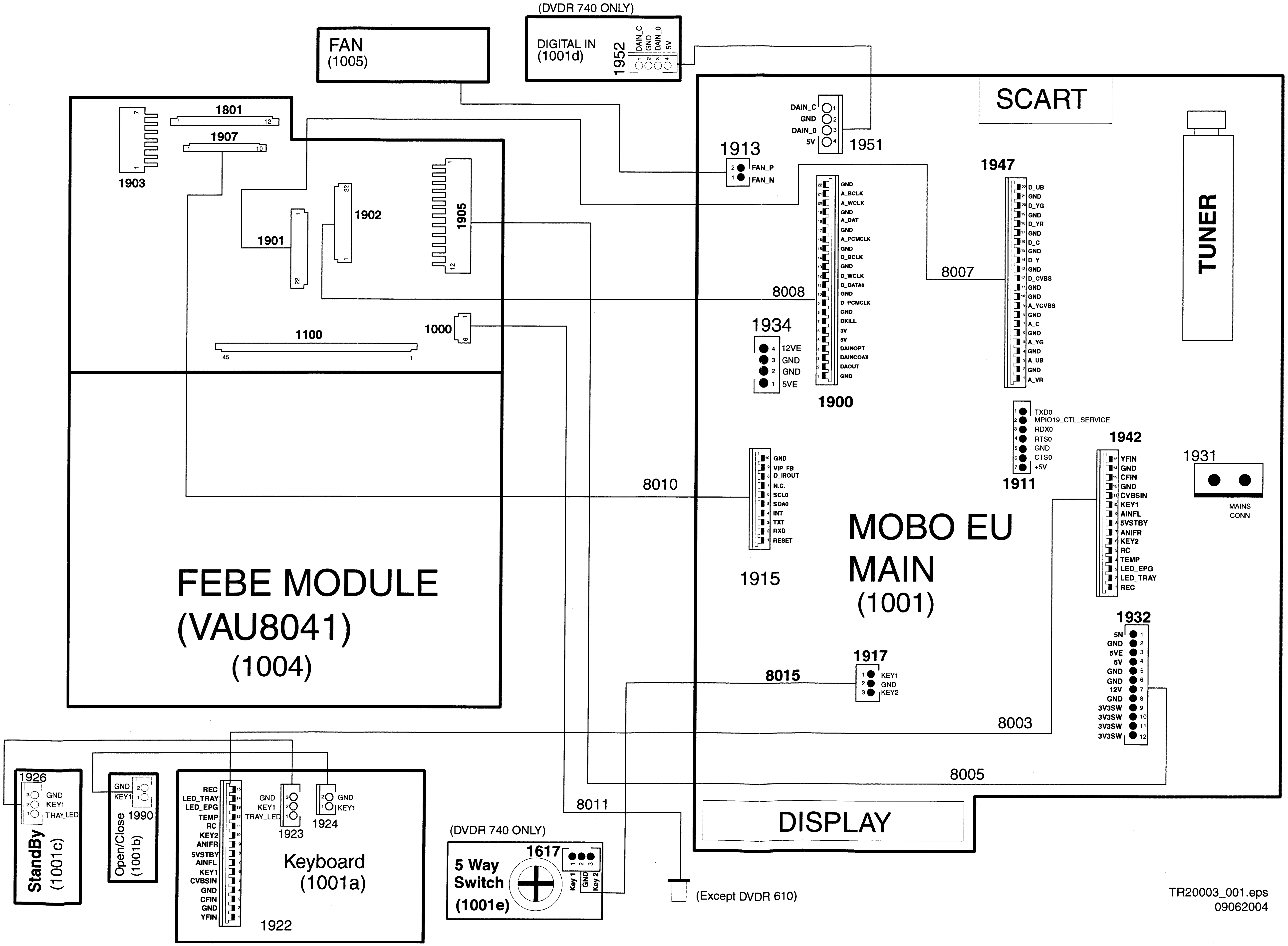

LECO U4.01L MODULE - DVD+RW BASIC ENGINE D4.0 + BACKEND
OPU66.30AV
TEMP. SENSOR
EEPROM
laser 650nm
FS diode
laser 780nm
650nm PD
3-D ACTUATOR
PAEDIC
ELANTEC
common
Rad,Foc1,Foc2
REP.REN
A..H
CD/DVD,H/L
VTHR,VDEL
IOTHR,IODEL
Bank
SCLK,SDIO,SEN
WSB
EFM (4)
TempSense + glue
Disc
Sledge
Tray
M
DRIVER
U,V,W
UP,UN,etc
sin,cos
TR-,TR+
MOTOR DRIVERS
Tray switch
RWN
CHEETAH 2
TRAYSW
EC
FG
TRAYIN,TRAYOUT
REFSIN_PCS,REFCOS_PCS
FO1,F02,RA
FTC
PPN
A1..A2,CALF
FEN etc
RF-REF
REP.REN
FSB (3)
LASP
ALFA
I2C (2)
CENTAURUS 2.0
IDE BUS
FLASH EPROM
SDRAM
ONLY FOR SETS WITH DV-IN
Digital Video Input IEEE 1394
6
Input
1000
PHY
LINK
FLASH
MIU
LECO IC PNX7520
SDRAM
I2C
BOOT EEPROM
I2C
USRDATA EEPROM
RS232
1911
SERVICE
1905
Front Keyboards
AUDIO L
AUDIO R
CVBS
S-VIDEO
1922
CONTROL LINES
AFCRI
AFCLI
CVBSFIN
CFIN
YFIN
15
ANALOG AUDIO / VIDEO & CONTROL LINES
Communication Line
1912
1915
ANALOG VIDEO
DIG.VIDEO
VIDEO INPUT PROCESSING
DIGITAL AUDIO
DIGITAL AUDIO
1901
1902
MOBO BOARD
SAT TIMER TV PRO REC OK VPS/PDC SAP LANG II
1942
CONTROL LINES
AINFR
AINFL
CVBSFIN
CFIN
YFIN
CONTROL UNIT SLAVE MICROPROCESSOR
1947
YUV-YC-CVBS
D_CVBS
D_Y
D_C
D_VR
D_YG
D_UB
CVBS-RGB-Y/C
A_VR
A_UB
A_YG
A_C
A_YCVBS
1900
AUDIO ENCODER I2S
A_WCLK
A_BCLK
A_DATA
A_PCMCLK
D_PCMCLK
D_DATAO
D_WCLK
D_BCLK
D_KILL
DAOUT
AUDIO PCM I2S
ADC
DAC
INPUT/OUTPUT PROCESSING & SOURCE SELECTION
TV-I/O
EXT1
AUX-I/O
EXT2
S-VIDEO
CVBS
AUDIO L/R
TUNER
ANTENNA INPUT
TV OUT
AUDIO DIGITAL
BUFFER
PSU
1932
FAN
1913
POWER SUPPLY
MAINS AC
E_14181_002
291104

DVDR615 Block diagram Lecolite U4.01L

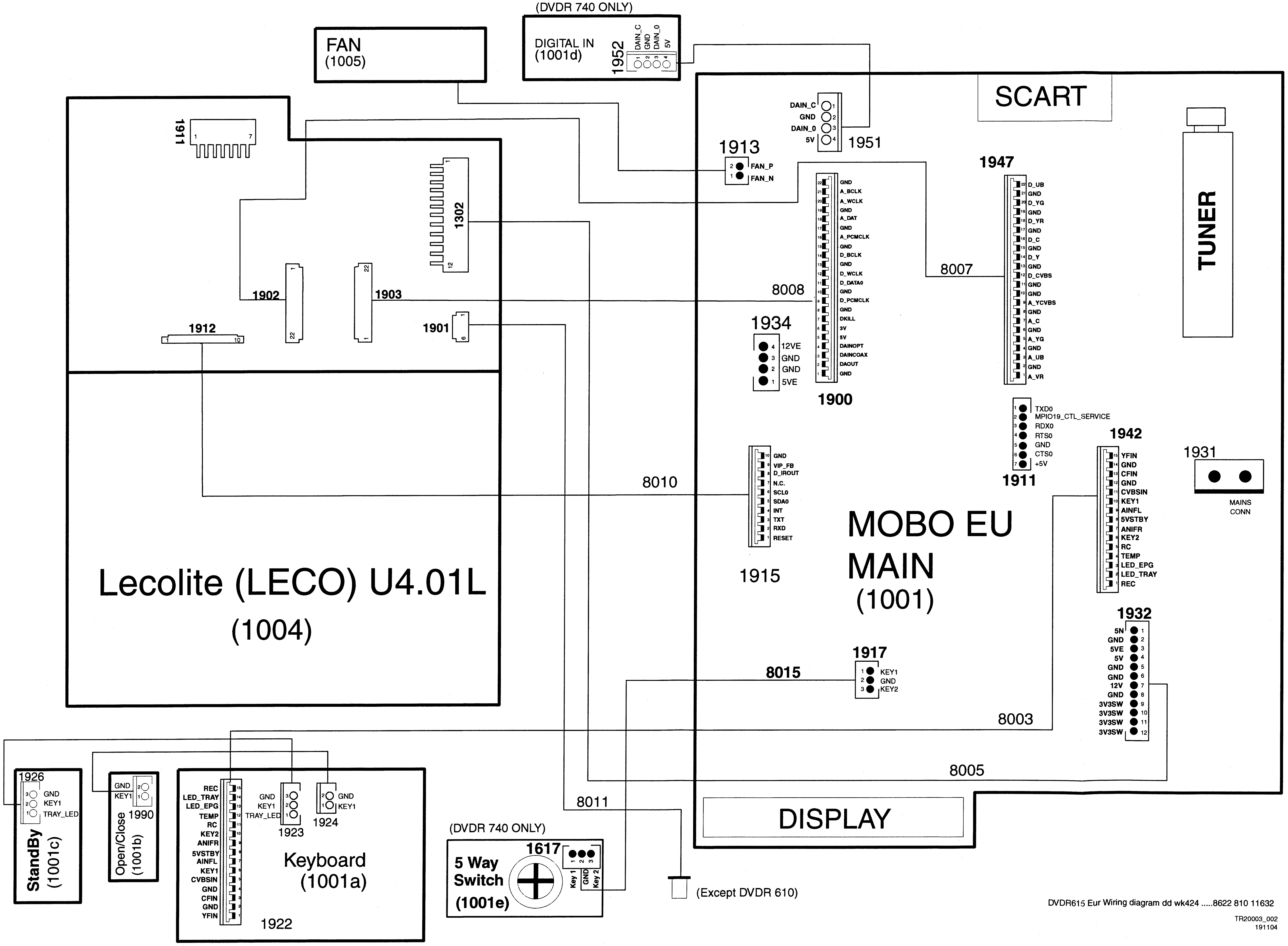
Control Block Diagram MOBO Board


For EPG sets only
Fan
Follow Me
P50
RC
Keys
G-Link
UART
GLINK
2
1
2
1
2
2
I2C
3V3
I2C Bus
Repeater
ASP Analog Slave Processor
TMP87CH74F
Serial
3
IR Blaster
TMP86CK74A
INT
Reset
AFC
2
1
35
Reset
Reset
>=1
Reset
5VSTBY
I2C
5V
Supply
VFT
Display
DVDR
IDE0
FEBE (Frontend / Backend) Electronics
Frontend
Tuner
ASC1
IMUTE
Multi Sound
Processor
MSP34x5
RSA1,RSA2
Audio Switches
HEF....
Reset
3V3
Video Matrix
STV6618
VS,CS,FR
Video Switches
NJM...
IMUTE
STBY
DD_ON
D_KILL_N
IPFAIL
>=1
KILL
I2C
ADC / DAC
AKILL
BKILL
Power
Supply
HD_ON
TR20002_001.eps
09062004

Wiring Diagram


(DVDR 740 ONLY)
DIGITAL IN
(1001d)
1952
DAIN_C
GND
DAIN_0
5V
FAN
(1005)
SCART
TUNER
1801
1907
1903
1902
1901
1905
1000
1100
FEBE MODULE
(VAU8041)
(1004)
DAIN_C
GND
DAIN_0
5V
1951
1913
FAN_P
FAN_N
1947
D_UB
GND
D_YG
GND
D_YR
GND
D_C
GND
D_Y
GND
D_CVBS
GND
GND
A_YCVBS
GND
A_C
GND
A_YG
GND
A_UB
GND
A_VR
8007
8008
GND
A_BCLK
A_WCLK
GND
A_DAT
GND
A_PCMCLK
GND
D_BCLK
GND
D_WCLK
D_DATA0
GND
D_PCMCLK
GND
DKILL
3V
5V
DAINOPT
DAINCOAX
DAOUT
GND
1900
1934
12VE
GND
GND
5VE
TXD0
MPIO19_CTL_SERVICE
RDX0
RTS0
GND
CTS0
+5V
1911
1942
YFIN
GND
CFIN
GND
CVBSIN
KEY1
AINFL
5VSTBY
ANIFR
KEY2
RC
TEMP
LED_EPG
LED_TRAY
REC
1931
MAINS CONN
8010
GND
VIP_FB
D_IROUT
N.C.
SCL0
SDA0
INT
TXT
RXD
RESET
1915
MOBO EU
MAIN
(1001)
1932
5N
GND
5VE
5V
GND
GND
12V
GND
3V3SW
3V3SW
3V3SW
3V3SW
1917
KEY1
GND
KEY2
8015
8003
8005
8011
DISPLAY
1926
GND
KEY1
TRAY_LED
StandBy
(1001c)
GND
KEY1
Open/Close
(1001b)
1990
REC
LED_TRAY
LED_EPG
TEMP
RC
KEY2
ANIFR
5VSTBY
AINFL
KEY1
CVBSIN
GND
CFIN
GND
YFIN
1922
GND
KEY1
TRAY_LED
1923
GND
KEY1
1924
Keyboard
(1001a)
(DVDR 740 ONLY)
1617
5 Way
Switch
(1001e)
Key 1
GND
Key 2
(Except DVDR 610)
TR20003_001.eps
09062004

Wiring Diagram LECO

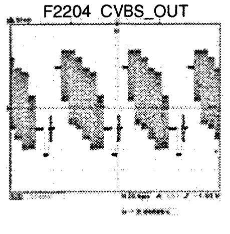

(DVDR 740 ONLY)
DIGITAL IN (1001d)
1952
DAIN_C GND DAIN_0 5V
FAN (1005)
SCART
TUNER
1911
1302
1902
1903
1912
1901
Lecolite (LECO) U4.01L (1004)
1951
DAIN_C GND DAIN_0 5V
1913
FAN_P FAN_N
1934
12VE GND GND 5VE
1900
GND A_BCLK A_WCLK GND A_DAT GND A_PCMCLK GND D_BCLK GND D_WCLK D_DATA0 GND D_PCMCLK GND DKILL 3V 5V DAINOPT DAINCOAX DAOUT GND
8008
8007
1947
D_UB GND D_YG GND D_YR GND D_C GND D_Y GND D_CVBS GND GND A_YCVBS GND A_C GND A_YG GND A_UB GND A_VR
1911
TXD0 MPIO19_CTL_SERVICE RDX0 RTS0 GND CTS0 +5V
1942
YFIN GND CFIN GND CVBSIN KEY1 AINFL 5VSTBY ANIFR KEY2 RC TEMP LED_EPG LED_TRAY REC
1931
MAINS CONN
8010
1915
GND VIP_FB D_IROUT N.C. SCL0 SDA0 INT TXT RXD RESET
MOBO EU MAIN (1001)
1932
5N GND 5VE 5V GND GND 12V GND 3V3SW 3V3SW 3V3SW 3V3SW
1917
KEY1 GND KEY2
8015
8003
8005
8011
DISPLAY
1926
GND KEY1 TRAY_LED
StandBy (1001c)
GND KEY1
1990
Open/Close (1001b)
REC LED_TRAY LED_EPG TEMP RC KEY2 ANIFR 5VSTBY AINFL KEY1 CVBSIN GND CFIN GND YFIN
GND KEY1 TRAY_LED
1923
GND KEY1
1924
Keyboard (1001a)
1922
(DVDR 740 ONLY)
5 Way Switch (1001e)
1617
Key1 GND Key2
(Except DVDR 610)

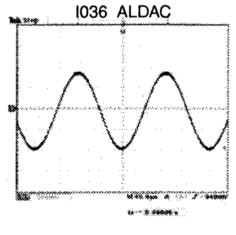
DVDR615 Eur Wiring diagram dd wk424 .....8622 810 11632

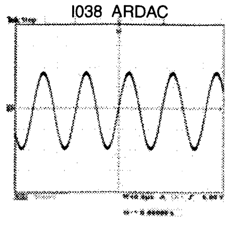
TR20003_002
191104

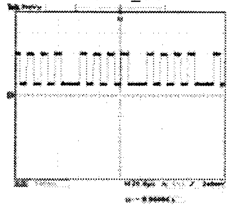
Waveforms

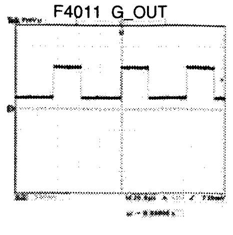
MOBO Board Waveforms

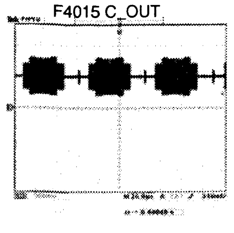

F2204 CVBS_OUT

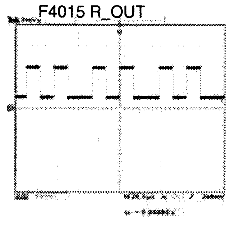

I036 ALDAC

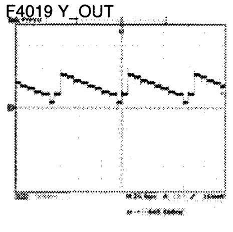

I038 ARDAC

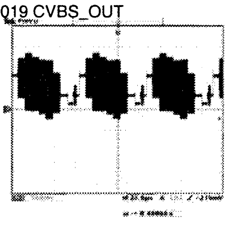

F4007 B_OUT

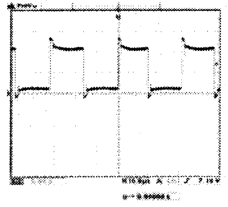

F4011 G_OUT

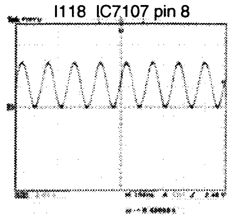

F4015 C_OUT

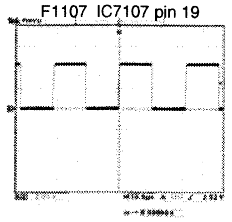

F4015 R_OUT

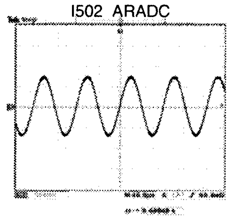

F4019 Y_OUT

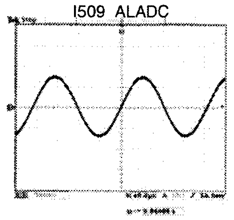

F4019 CVBS_OUT

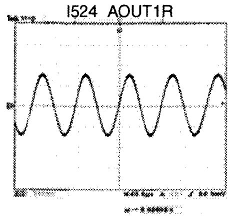

I115 7102/7104 Emmitter

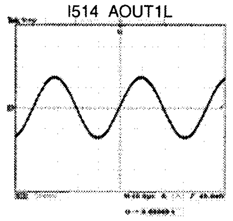

I118 IC7107 pin 8

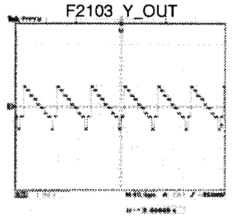

F1107 IC7107 pin 19

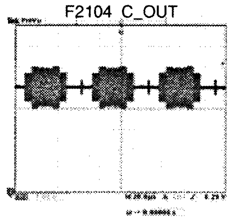

I502 ARADC

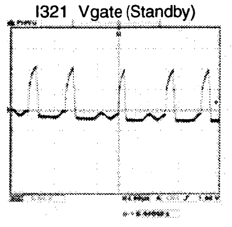

I509 ALADC

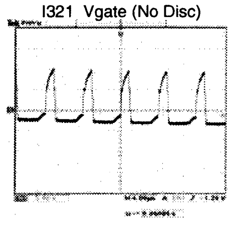

I524 AOUT1R

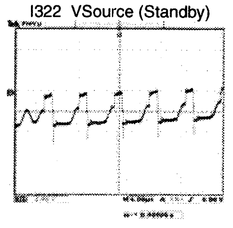

I514 AOUT1L

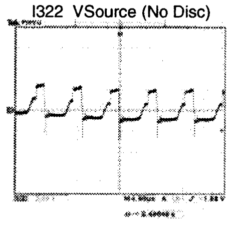

F2103 Y_OUT

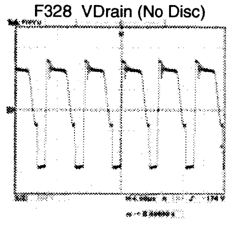

F2104 C_OUT

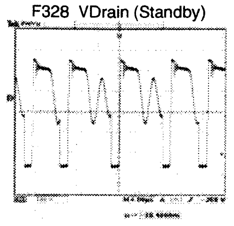

I321 Vgate (Standby)

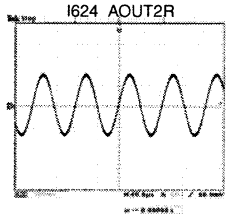

I321 Vgate (No Disc)

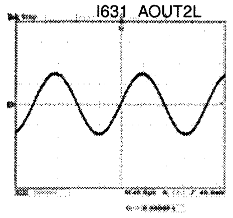

I322 VSource (Standby)


I322 VSource (No Disc)

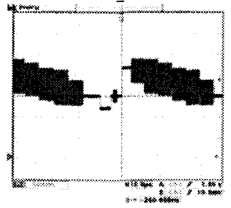

F328 VDrain (No Disc)

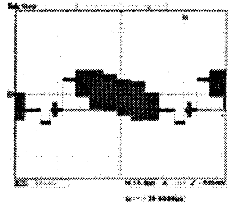

F328 VDrain (Standby)

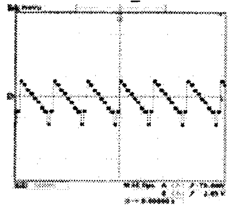

I624 AOUT2R

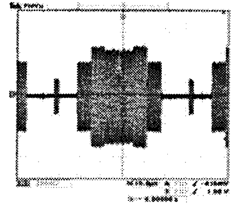

I631 AOUT2L

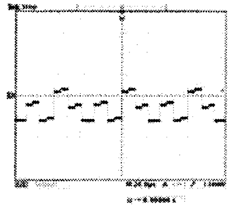
FEBE Board Waveforms

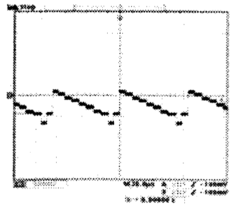

I922 A_YCVBS

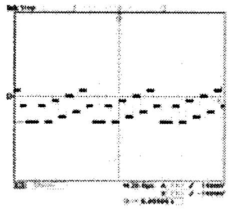

I926 D_CVBS

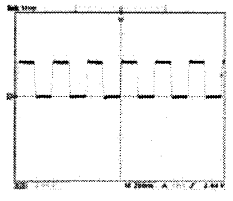

I928 D_Y

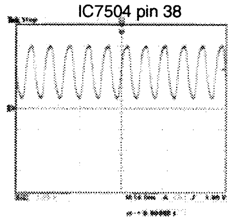

I930 D_C

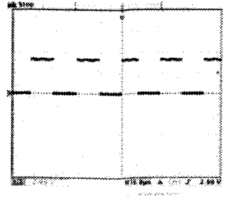

I931 D_VR

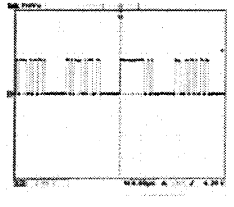

I932 D_YG

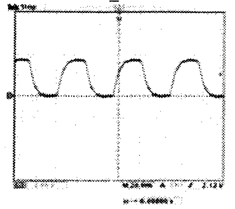

I933 D_UB

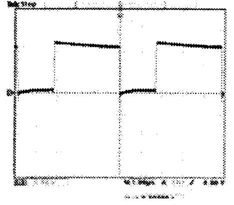

F905 D_BCLK

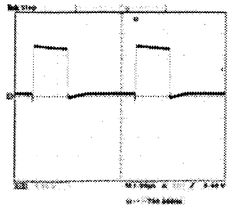

IC7504 pin 38

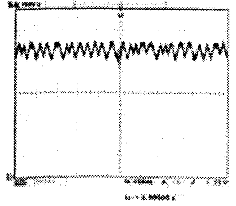

F906 D_WCLK

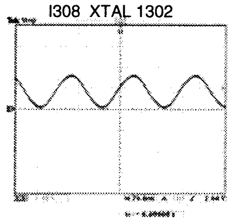

F907 D_DATA0

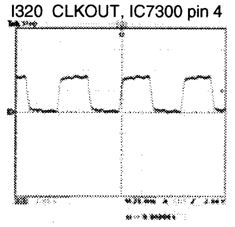

F908 D_PCMCLK

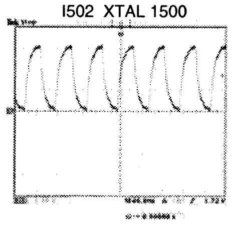

IC7929 pin 5

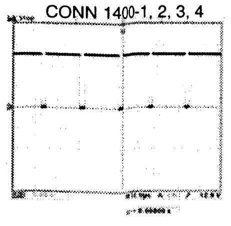

IC7929 pin 6

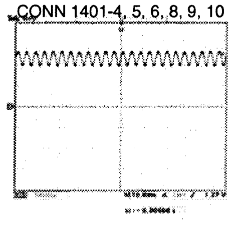

I257 / I259 RFN3 / RFP3,
IC7201 pin 31, 32

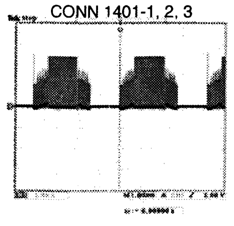

I308 XTAL 1302


I320 CLKOUT, IC7300 pin 4


I502 XTAL 1500


CONN 1400-1, 2, 3, 4


CONN 1401-4, 5, 6, 8, 9, 10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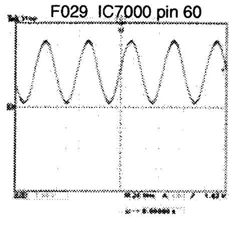
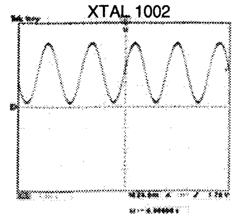
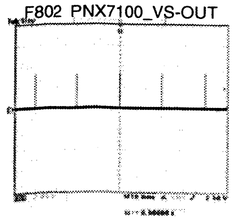
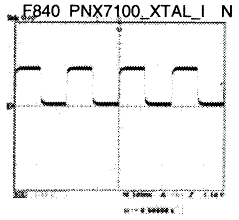
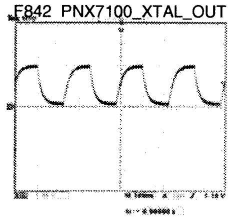
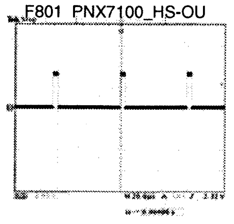

F029 IC7000 pin 60


XTAL 1002


F802 PNX7100_VS-OUT


F840 PNX7100_XTAL_IN


F842 PNX7100_XTAL_OUT


F801 PNX7100_HS-OU

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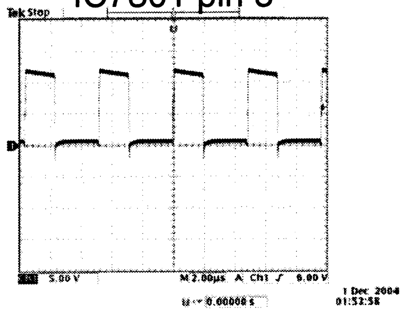
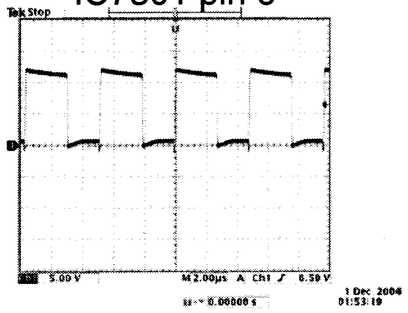
WAVEFORMS Lecolite Board

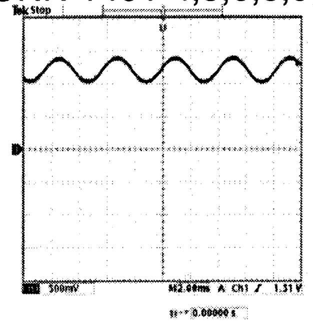
IC7301 pin 5



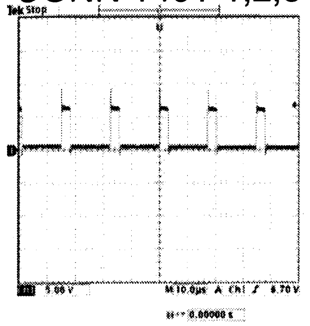
IC7301 pin 6



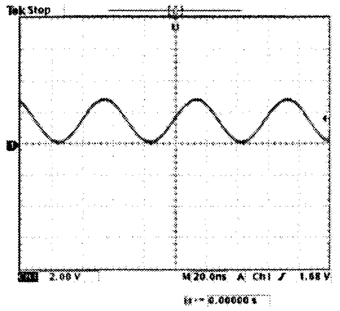
CONN 1401-4,5,6,8,9,10



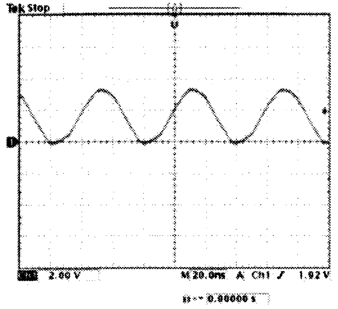
CONN 1401-1,2,3



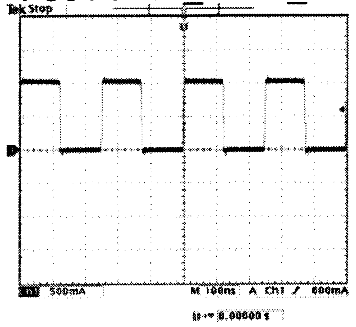
IC 7501-1 XTAL IN I502



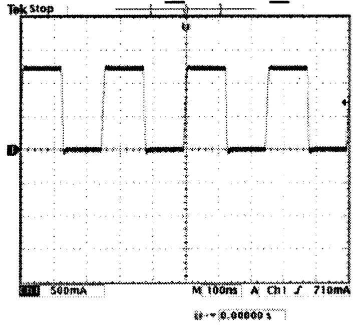
IC 7501-1 XTAL OUT I501



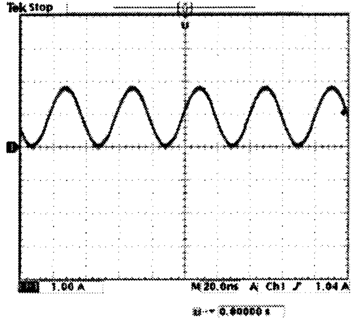
F801 PNX_XTAL_IN



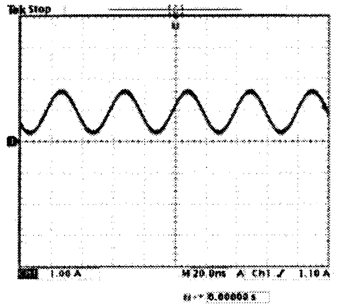
F802 PNX_XTAL_OUT



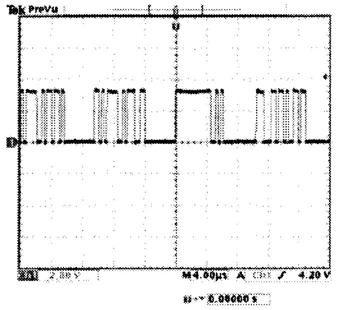
1002 XTAL(2078 side)



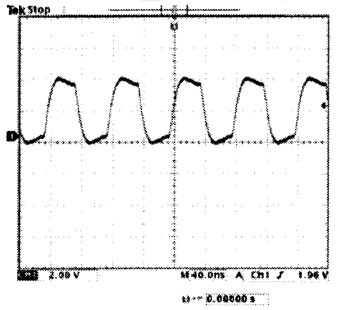
1002 XTAL(2079 side)



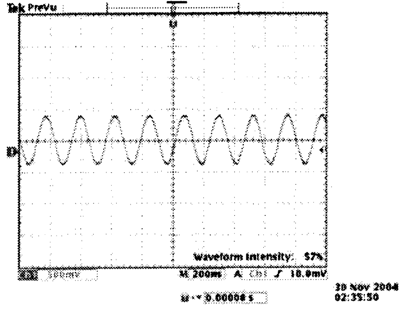
F916 PNX_SDO_OUT



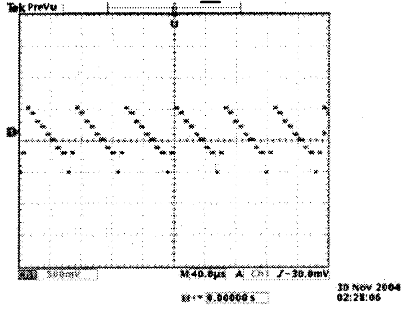
F917 PNX_FSCLK_OUT



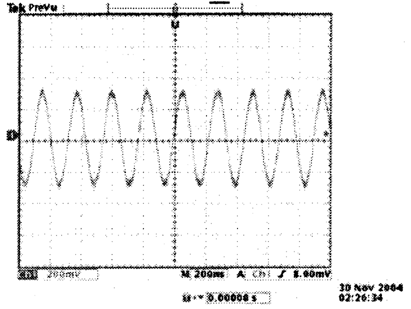
I917 D_CVBS



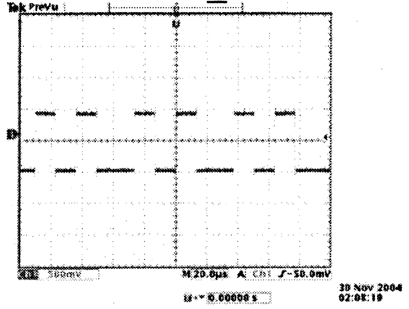
I919 D_Y



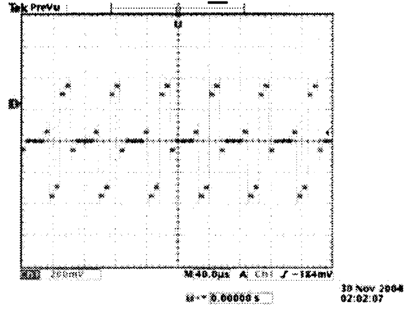
I921 D_C



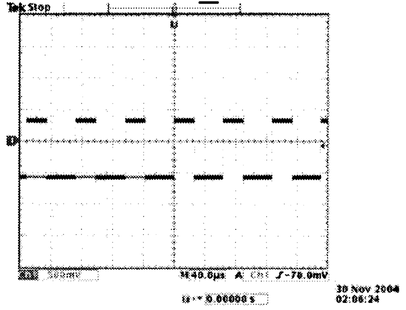
I922 D_V



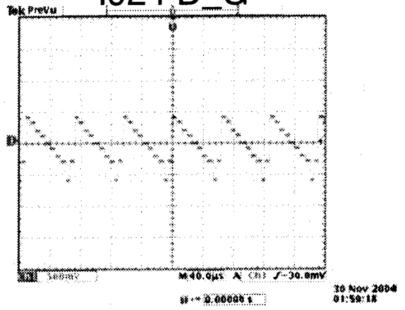
I922 D_R



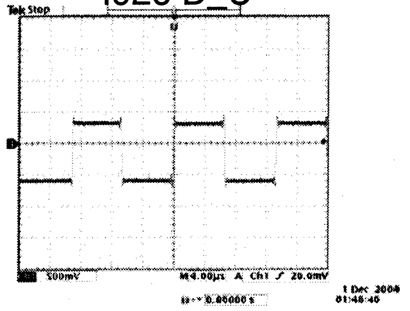
I922D_Y



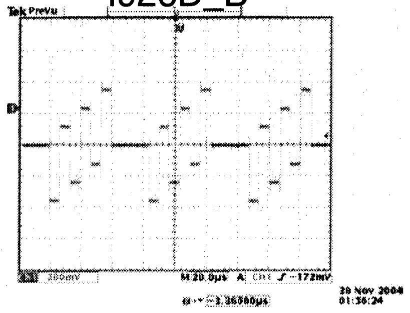
I924 D_G



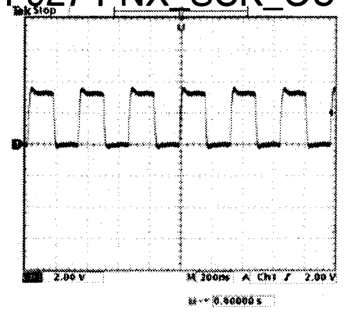
I926 D_U



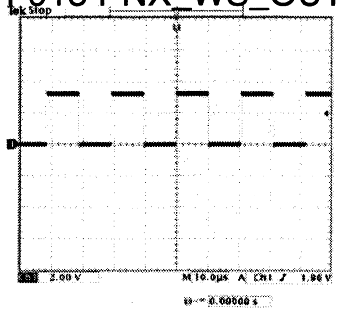
I926D_B



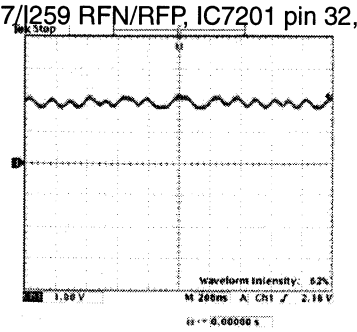
F927 PNX_SCK_OUT



F915 PNX_WS_OUT



I257/I259 RFN/RFP, IC7201 pin 32,31



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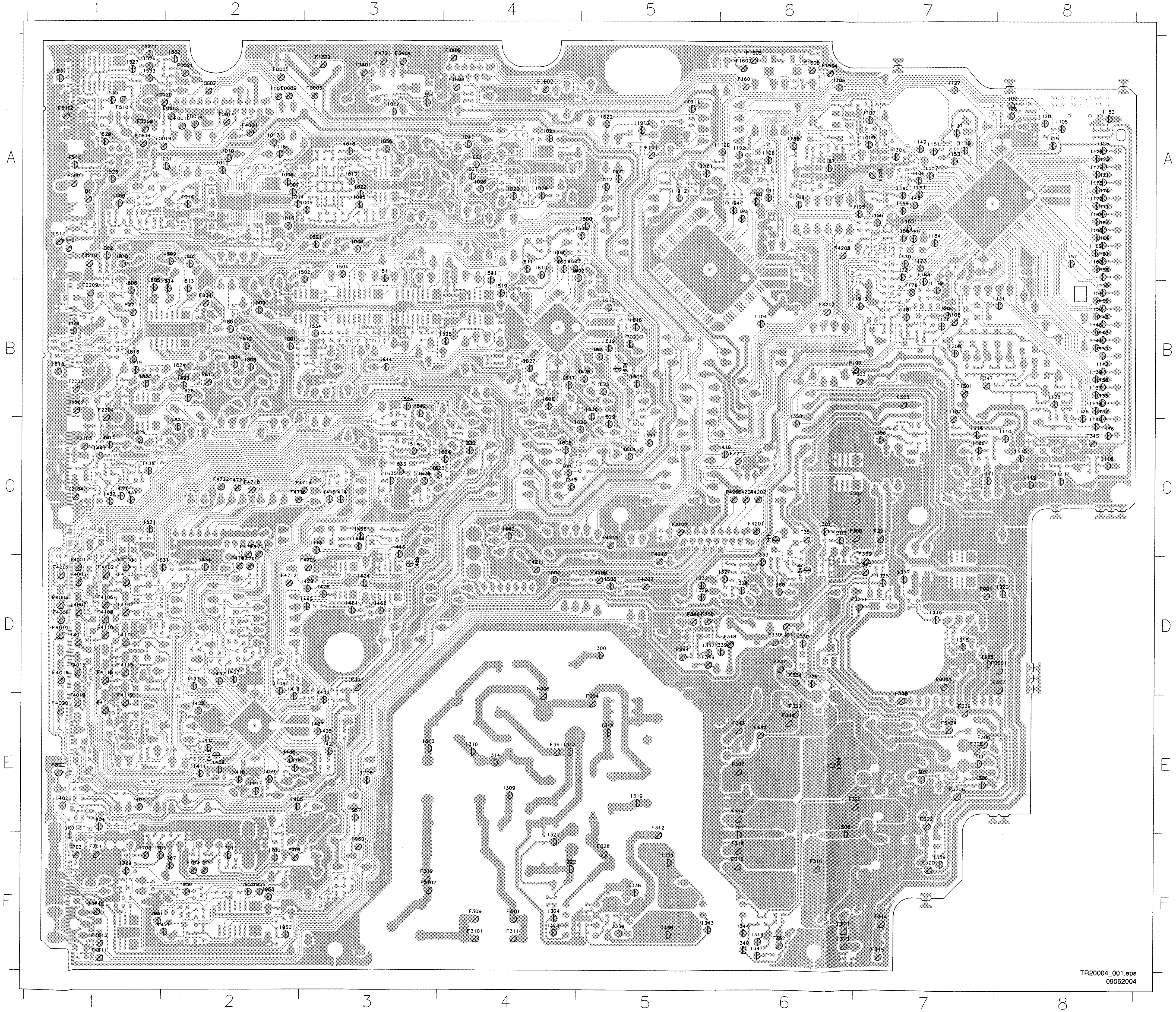
Test points overview MOBO Board



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F0002	A2	F4007	D1	I114	C7	I319	E5	I534	B3
F0003	A3	F4008	D1	I115	C8	I320	D8	I535	A1
F0005	A2	F4010	D1	I116	C8	I321	F4	I541	A4
F0007	A2	F4011	D1	I117	A7	I322	F4	I542	B3
F0009	A2	F4015	D1	I118	A7	I323	F4	I602	A4
F001	D7	F4016	D1	I119	A8	I324	F4	I603	A4
F0011	A2	F4019	E1	I120	A8	I325	D7	I604	B5
F0012	A2	F4020	E1	I121	A8	I326	D6	I605	C4
F0014	A2	F4021	A2	I122	A8	I327	D6	I606	B4
F0016	A2	F4101	D1	I123	A8	I328	D6	I607	A4
F0019	A1	F4102	D1	I124	A8	I329	D5	I608	A4
F0020	A1	F4103	D1	I125	A8	I330	D6	I609	B5
F0021	A2	F4106	D1	I126	A8	I331	F5	I610	A4
F100	B6	F4107	D1	I127	A7	I332	D5	I611	A4
F108	B7	F4108	D1	I128	B8	I333	C6	I613	B5
F1107	B7	F4110	D1	I129	B8	I334	F5	I614	B3
F111	A5	F4111	D1	I130	A7	I336	F5	I616	B5
F1301	B7	F4115	D1	I131	B8	I337	D5	I617	B4
F1302	A3	F4116	D1	I132	B8	I338	F5	I618	C5
F1601	A6	F4119	E1	I134	B8	I339	D6	I619	B5
F1602	A4	F4120	E1	I135	B8	I340	F6	I620	C5
F1603	A6	F4201	C6	I136	A7	I341	C6	I621	B5
F1604	A6	F4202	C6	I137	B8	I343	F5	I622	C4
F1605	A6	F4203	B6	I138	B8	I344	F6	I623	C3
F1606	A6	F4204	C6	I139	B8	I345	C4	I624	C4
F1608	A4	F4205	A6	I140	A7	I346	D6	I625	B5
F1609	A4	F4206	C6	I141	A7	I347	F6	I626	B5
F1611	F1	F4207	D5	I142	B8	I349	F6	I627	B4
F1612	F1	F4209	D5	I143	B8	I353	C5	I628	C3
F1613	F1	F4210	C6	I144	B8	I354	A3	I629	B5
F1614	A1	F4211	D4	I145	A7	I355	D7	I630	B5
F2102	C5	F4213	C5	I146	B8	I356	C7	I631	D1
F2103	C1	F4215	C5	I147	B8	I358	B6	I633	C3
F2104	C1	F4701	C2	I148	B8	I359	F7	I635	C3
F2202	B1	F4703	C2	I149	A7	I360	D6	I700	F2
F2203	B1	F4705	D2	I150	B8	I361	C4	I701	F2
F2204	B1	F4707	D2	I151	A7	I401	E1	I702	B5
F2209	B1	F4709	D3	I152	B8	I402	E1	I703	F1
F2210	A1	F4712	D2	I153	A7	I403	E1	I704	F1
F2211	B1	F4714	C3	I154	B8	I404	E1	I705	F1
F300	C7	F4716	C2	I155	B8	I405	E2	I706	E3
F301	D3	F4718	C2	I156	A7	I406	C3	I707	F2
F302	C7	F4720	C2	I157	A8	I407	D2	I801	B2
F303	B7	F4721	A3	I158	A8	I408	D2	I802	A2
F304	E5	F4722	C2	I159	A7	I409	E2	I804	B2
F305	E7	F509	A1	I160	A8	I410	C6	I805	B1
F306	E7	F510	A1	I161	A8	I411	E2	I806	B1
F307	E6	F5101	A1	I162	A8	I413	E2	I808	B2
F308	D4	F5102	A1	I163	A7	I414	C3	I809	A2
F309	F4	F5104	E7	I164	A8	I415	E2	I810	A1
F310	F4	F511	A1	I165	A8	I416	C3	I812	B2
F3101	F4	F512	A1	I166	A7	I417	E2	I813	B2
F3102	F3	F701	F1	I167	A8	I418	E2	I814	B2
F311	F4	F702	F2	I168	A8	I419	D2	I815	C1
F312	F6	F703	F1	I169	A7	I421	E3	I816	B1
F313	F6	F704	F2	I170	A7	I422	E2	I818	B1
F314	F7	F705	F2	I171	A8	I424	D3	I819	B1
F315	F7	F801	B2	I172	A8	I425	E3	I820	B1
F316	F6	F802	E1	I173	A7	I426	D3	I821	A3
F317	F6	F815	B2	I174	A8	I427	E3	I823	B2
F318	F6	F950	F3	I175	A8	I428	D3	I824	B2
F319	F3	I000	A1	I176	C8	I429	D3	I825	C1
F320	F7	I001	B2	I177	A7	I430	D3	I826	B2
F3201	D8	I002	A1	I178	B7	I431	C1	I827	C2
F3206	E7	I006	A2	I179	B7	I432	D2	I828	B1
F3209	A1	I007	A2	I180	C8	I433	D2	I829	A5
F321	C7	I009	A3	I181	B7	I434	D2	I950	F2
F3211	D7	I010	A2	I182	A8	I435	C1	I951	F2
F322	E7	I011	A2	I183	A7	I436	E2	I952	F2
F323	B7	I012	A3	I184	A7	I437	C1	I953	F2
F324	E6	I013	A3	I185	A6	I438	E2	I954	F1
F325	E7	I014	A2	I186	A6	I439	C1	I955	F2
F326	A7	I015	A2	I187	A6	I440	D3	I956	F2
F327	D8	I016	A3	I188	A6	I441	C1	I957	E3
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F331	D6	I020	A4	I1911	A5	I445	C3		
F332	E6	I021	A4	I1912	A5	I459	E2		
F333	E6	I022	A3	I1913	B7	I461	D3		
F334	D6	I023	A4	I192	A6	I462	D3		
F336	E6	I025	A3	I193	A6	I500	A5		
F337	D6	I026	A4	I194	A6	I501	A5		
F338	D7	I027	A4	I195	A7	I502	A3		
F339	C7	I029	A4	I200	B7	I504	A3		
F340	D7	I031	A2	I202	B7	I505	D5		
F3401	A3	I036	A3	I300	D5	I507	D4		
F3404	A3	I038	A3	I301	C6	I509	B2		
F341	E4	I041	A4	I302	E6	I510	A5		
F342	E5	I101	A5	I303	C6	I511	A3		
F343	E6	I102	A8	I304	E6	I512	A5		
F344	D5	I104	B6	I305	E7	I514	C3		
F345	C8	I105	A8	I306	E7	I519	B4		
F346	D5	I106	C7	I308	E6	I521	C1		
F347	B7	I107	A7	I309	E4	I5211	A1		
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F349	D5	I109	A7	I311	E7	I525	B4		
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F351	C6	I1107	A7	I313	E3	I527	A1		
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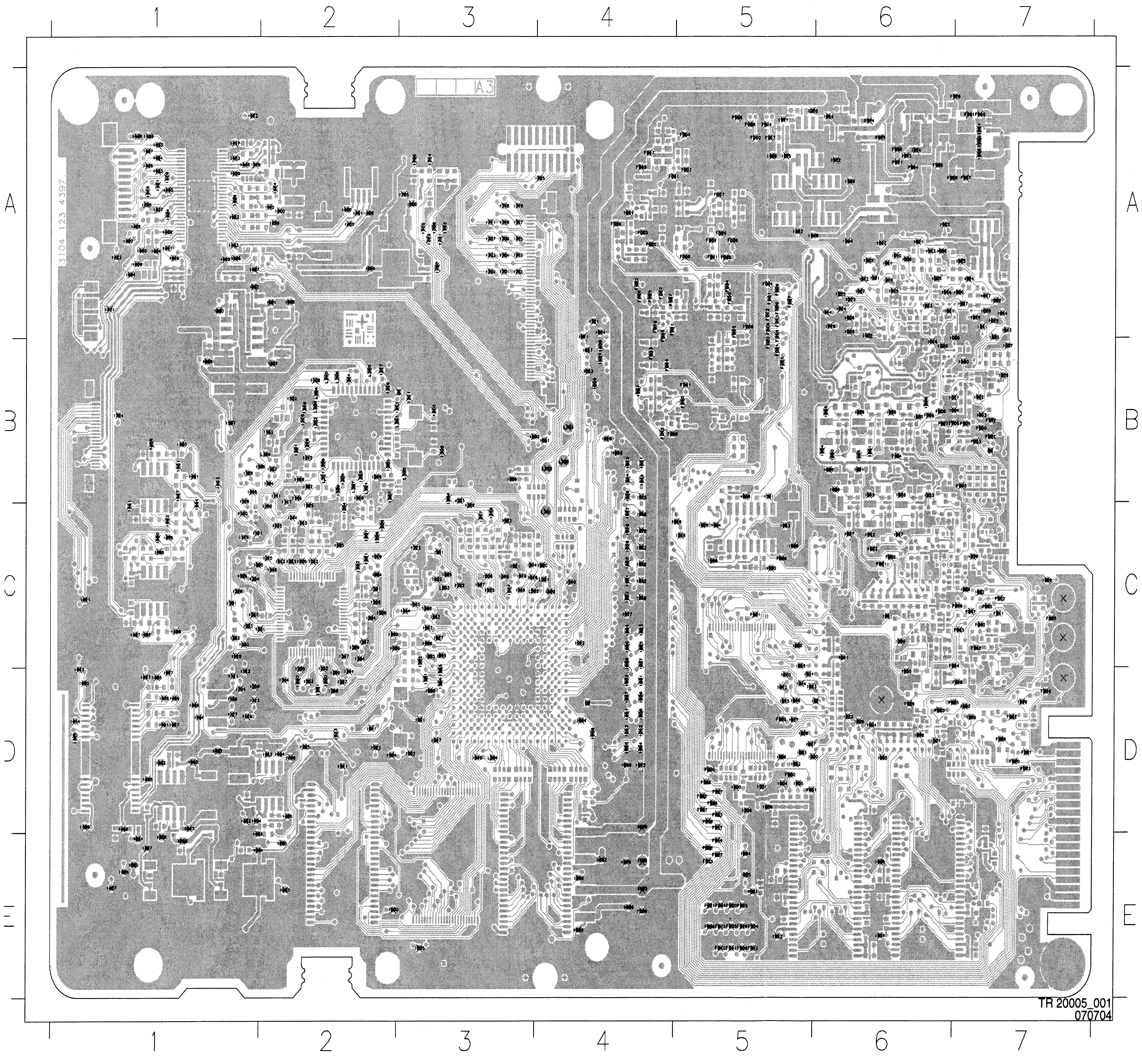
F4001	D1	I112	C8	I315	D7	I529	A1		
F4002	D1	I1120	A6	I316	D7	I531	A1		

Test points overview FEBE Board



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Test points overview LECO Board

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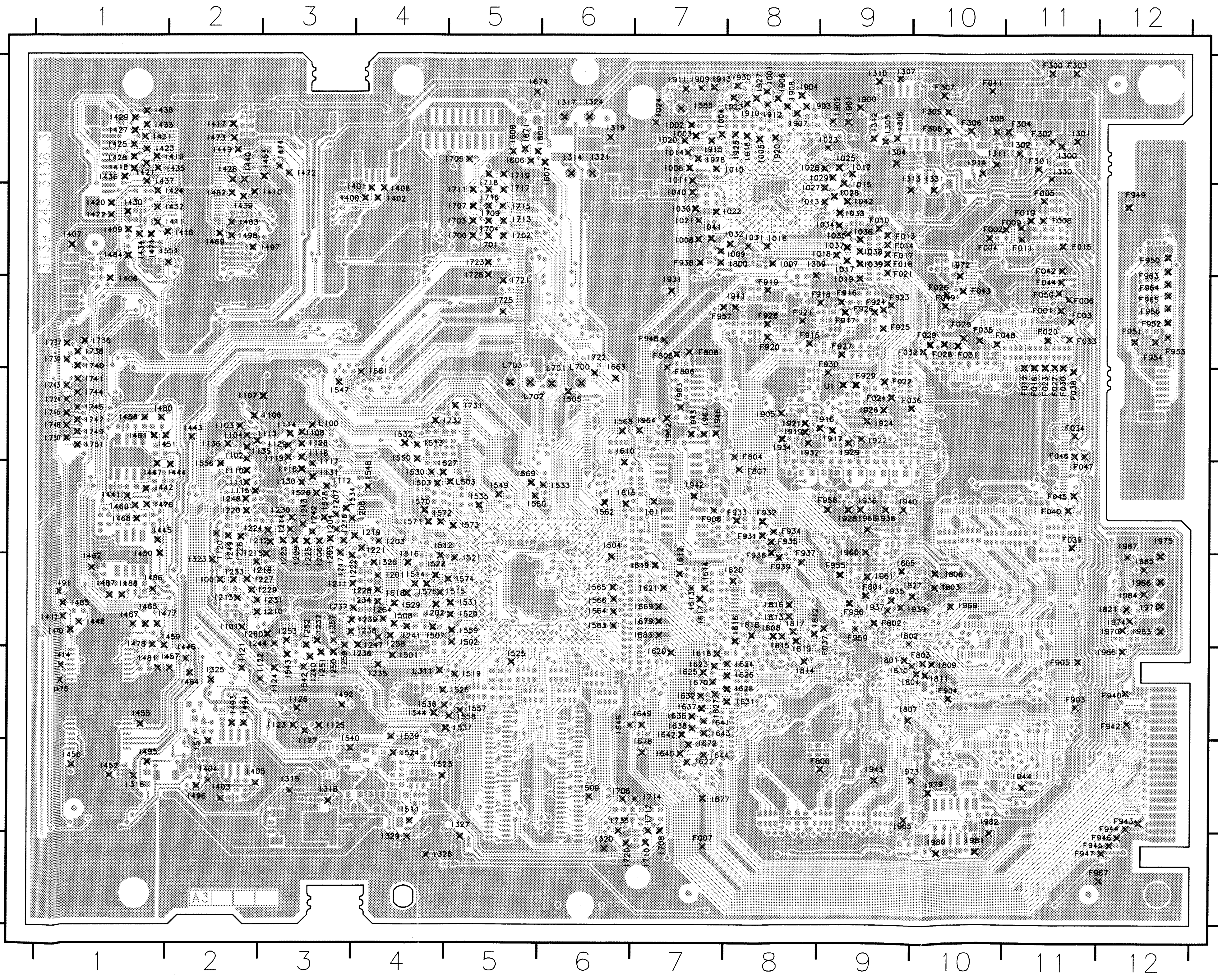

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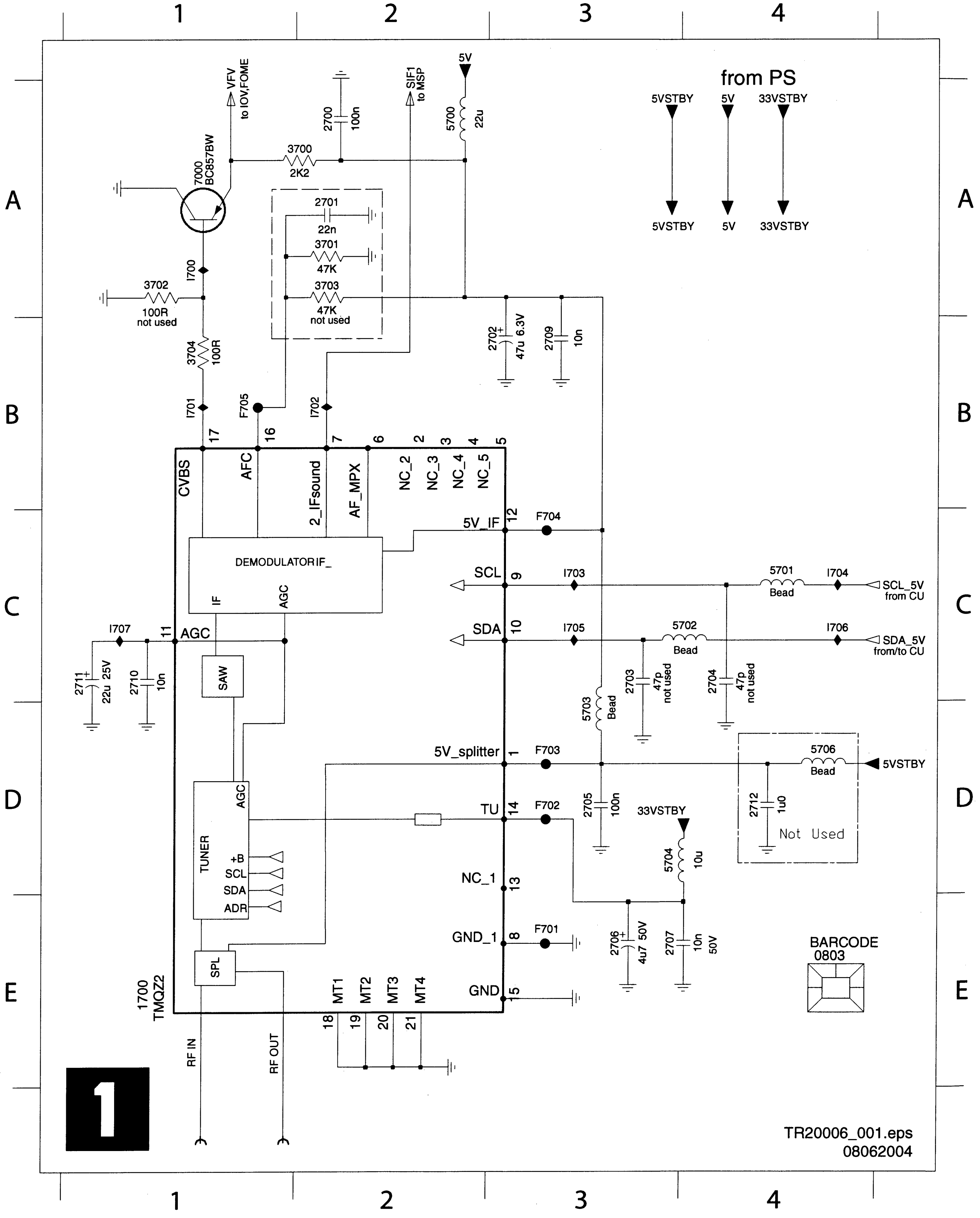
I801 G9
I802 F9
I803 F10
I804 G10
I805 F9
I806 F10
I807 G9
I808 F8
I809 G10
I810 G10
I811 G10
I812 F8
I813 F8
I814 G8
I815 F8
I816 F8
I817 F8
I818 F8
I819 F8
I820 F8
I821 F12
I827 F10
I900 A9
I901 A9
I902 A9
I903 A8
I904 A8
I905 D8
I906 A8
I907 A8
I908 A8
I909 A7
I910 A8
I911 A7
I912 A8
I913 A7
I914 A10
I915 A7
I916 D9
I917 D9
I918 A8
I919 D8
I920 A8
I921 D8
I922 D9
I923 A8
I924 D9
I925 A8
I926 D9
I927 A8
I928 E9
I929 D9
I930 A8
I931 C7
I932 D8
I934 D8
I935 F9
I936 E9
I937 F9
I938 E9
I939 F9
I940 E9
I941 C8
I942 E7
I943 D7
I944 H11
I945 H9
I946 D7
I960 E9
I961 F9
I962 D7
I963 D7
I964 D7
I965 H9
I966 G12
I967 D7
I968 E9
I969 F10
I970 F12
I971 F12
I972 C10
I973 H10
I974 F12
I975 F12
I978 A7
I979 H10
I980 I10
I981 I10
I982 I10
I983 F12
I984 F12
I985 F12
I986 F12
I987 F12
L100 D3
L311 G4
L503 E5
L700 D6
L701 D6
L702 D5
L703 D5

E_14181_005
191104

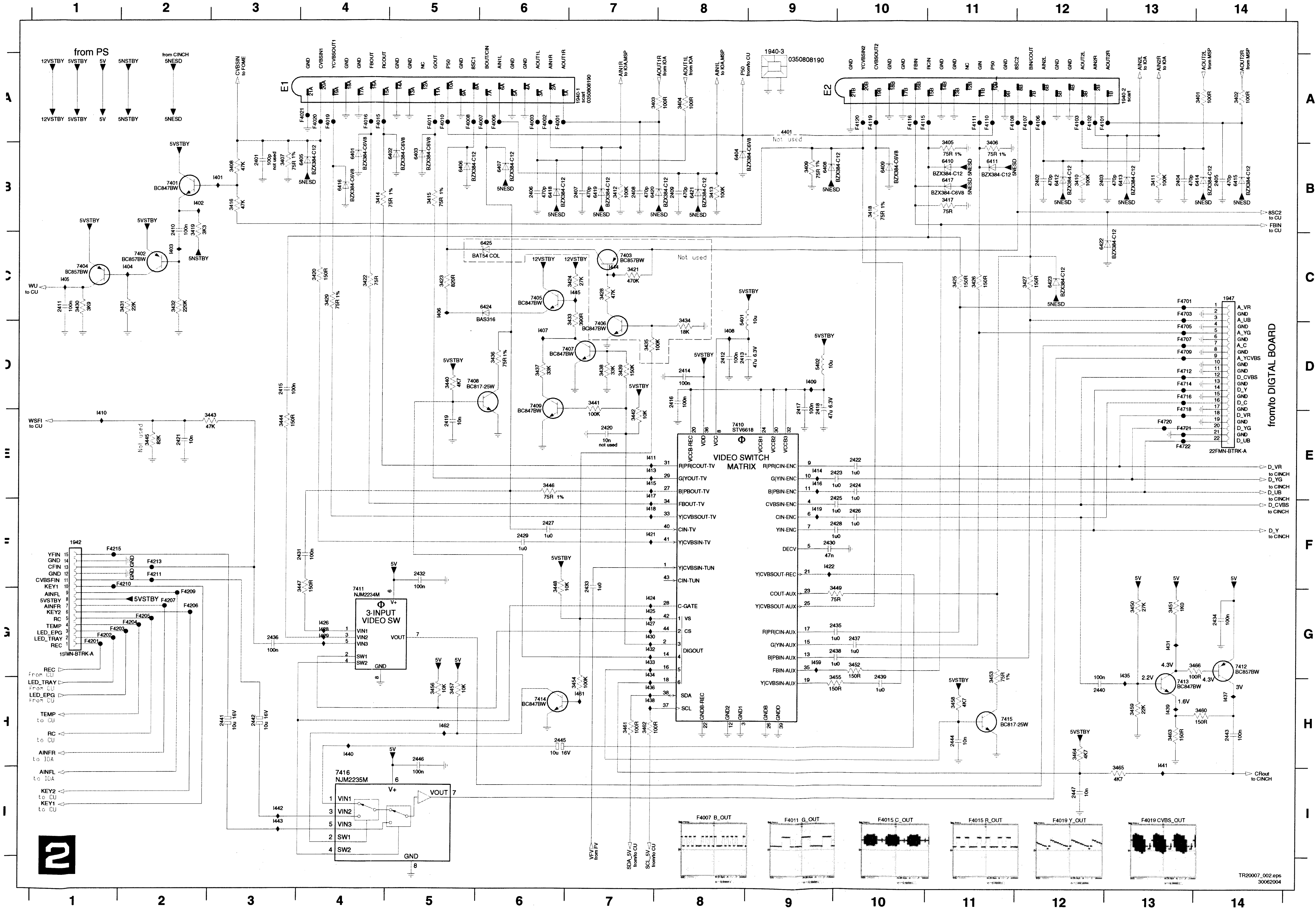
7. Circuit Diagrams and PWB Layouts

MOBO: Frontend Video (FV)

0803	E4
1700	E1
2700	A2
2701	A2
2702	B3
2703	C3
2704	C4
2705	D3
2706	E3
2707	E3
2709	B3
2710	C1
2711	C1
2712	D4
3700	A2
3701	A2
3702	A1
3703	A2
3704	B1
5700	A2
5701	C4
5702	C4
5703	D3
5704	D3
5706	D4
7000	A1
F701	E3
F702	D3
F703	D3
F704	C3
F705	B1
I700	A1
I701	B1
I702	B2
I703	C3
I704	C4
I705	C3
I706	C4
I707	C1

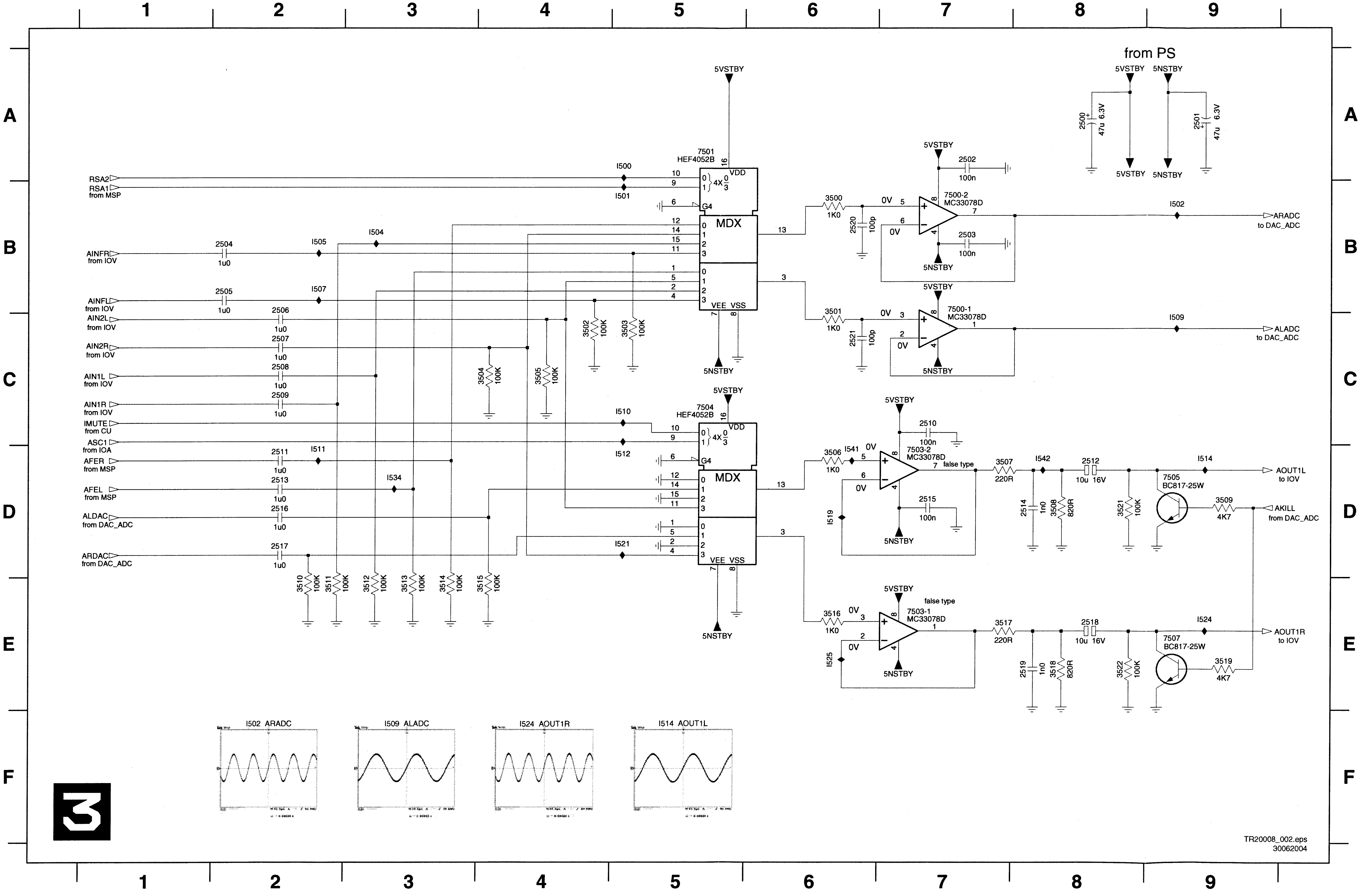

1
2
3
4
A
B
C
D
E
VFV to IOV,FOME
SIF1 to MSP
5V
from PS
5VSTBY
5V
33VSTBY
7000 BC857BW
3700 2K2
2700 100n
5700 22u
2701 22n
3701 47K
3703 47K not used
3702 100R not used
I700
3704 100R
2702 47u 6.3V
2709 10n
I701
F705
I702
17
16
7
6
2
3
4
5
CVBS
AFC
2_IFsound
AF_MPX
NC_2
NC_3
NC_4
NC_5
5V_IF
12
F704
DEMODULATORIF_
IF
AGC
SCL
9
I703
5701 Bead
I704
SCL_5V from CU
SDA
10
I705
5702 Bead
I706
SDA_5V from/to CU
I707
11
AGC
2711 22u 25V
2710 10n
SAW
2703 47p not used
2704 47p not used
5703 Bead
5V_splitter
1
F703
5706 Bead
5VSTBY
2705 100n
2712 1u0
Not Used
TUNER
AGC
+B
SCL
SDA
ADR
TU
14
F702
33VSTBY
5704 10u
NC_1
13
GND_1
8
F701
2706 4u7 50V
2707 10n 50V
SPL
GND
15
MT1
MT2
MT3
MT4
18
19
20
21
1700 TMQZ2
RF IN
RF OUT
BARCODE 0803
TR20006_001.eps 08062004

MOBO: Video In/Out (IOV)


1 2 3 4 5 6 7 8 9 10 11 12 13 14
A B C D E F G H I
from PS
12VSTBY 5VSTBY 5V 5NSTBY
from CINCH 5NESD
CVBSIN to FOME
E1
1940-1 scart 0350808190
E2
1940-2 scart
1940-3 0350808190
AIN1R to IOA,MSP
AOUT1R from IOA
AOUT1L from IOA
AIN1L to IOA,MSP
P50 from/to CU
AIN2L to IOA
AIN2R to IOA
AOUT2L from MSP
AOUT2R from MSP
4401 Not used
7401 BC847BW
7402 BC857BW
7403 BC857BW
7404 BC857BW
7405 BC847BW
7406 BC847BW
7407 BC847BW
7408 BC817-25W
7409 BC847BW
7412 BC857BW
7413 BC847BW
7414 BC847BW
7415 BC817-25W
6425 BAT54 COL
6424 BAS316
Not used
WU to CU
WSFI to CU
7410 STV6618
VIDEO SWITCH MATRIX
7411 NJM2234M
3-INPUT VIDEO SW
VIN1 VIN2 VIN3 SW1 SW2 VOUT GND V+
7416 NJM2235M
1942
15MN-BTRK-A
YFIN GND CFIN GND CVBSFIN KEY1 AINFL 5VSTBY AINFR KEY2 RC TEMP LED_EPG LED_TRAY REC
REC from CU
LED_TRAY from CU
LED_EPG from CU
TEMP to CU
RC to CU
AINFR to IOA
AINFL to IOA
KEY2 to CU
KEY1 to CU
1947
22FMN-BTRK-A
A_VR GND A_UB GND A_YG GND A_C GND A_YCVBS GND GND D_CVBS GND D_Y GND D_C GND D_VR GND D_YG GND D_UB
from/to DIGITAL BOARD
8SC2 to CU
FBIN to CU
D_VR to CINCH
D_YG to CINCH
D_UB to CINCH
D_CVBS to CINCH
D_Y to CINCH
CRout to CINCH
VFV from FV
SDA_5V from/to CU
SCL_5V from/to CU
F4007 B_OUT
F4011 G_OUT
F4015 C_OUT
F4015 R_OUT
F4019 Y_OUT
F4019 CVBS_OUT
TR20007_002.eps 30062004
2

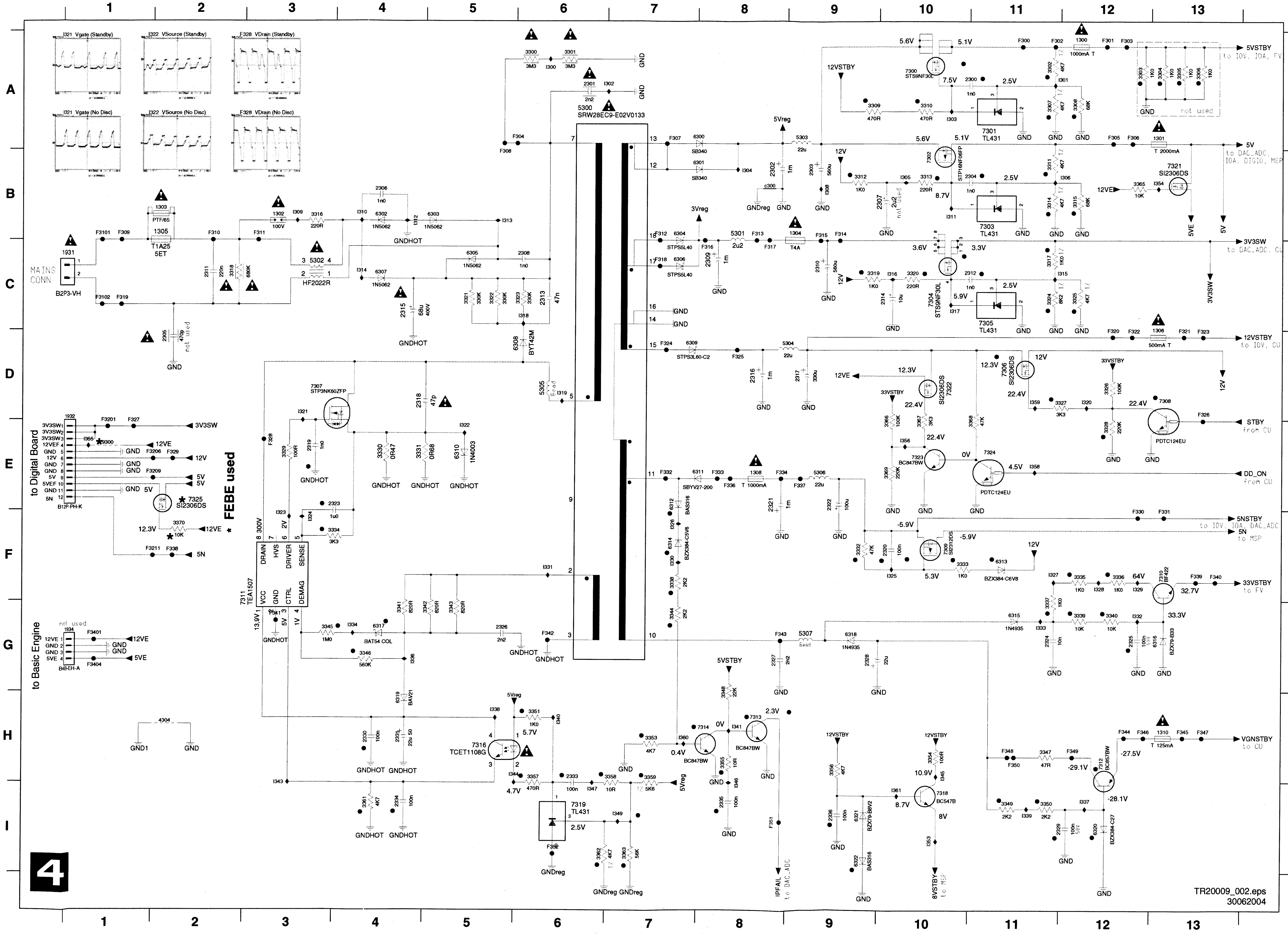
1940-1	A7
1940-2	A13
1940-3	A9
1942	F1
1947	C14
2401	B3
2402	B12
2403	B12
2404	B13
2405	B14
2406	B6
2407	B7
2408	B7
2409	B8
2410	B2
2411	C1
2412	D8
2413	D8
2414	D8
2415	D3
2416	D8
2417	D9
2418	D9
2419	E5
2420	E7
2421	E2
2422	E10
2423	E10
2424	E10
2425	F10
2426	F10
2427	F6
2428	F10
2429	F6
2430	F9
2431	F4
2432	F5
2433	F7
2434	G14
2435	G10
2436	G3
2437	G10
2438	G10
2439	H10
2440	H12
2441	H3
2442	H3
2443	H14
2444	H11
2445	H6
2446	H5
2447	I12
3401	A14
3402	A14
3403	A7
3404	A8
3405	B11
3406	B11
3407	B3
3408	B3
3409	B9
3410	B12
3411	B13
3412	B7
3413	B8
3414	B4
3415	B5
3416	B3
3417	B11
3418	B10
3419	B2
3420	C4
3421	C7
3422	C4
3423	C5
3424	C7
3425	C11
3426	C11
3427	C12
3428	C7
3429	C4
3430	C1
3431	C2
3432	C2
3433	C7
3434	D8
3435	D7
3436	D6
3437	D6
3438	D7
3439	D7
3440	D5
3441	D7
3442	E7
3443	E3
3444	E3
3445	E2
3446	E6
3447	F4
3448	F6
3449	G10
3450	G13
3451	G13
3452	G10
3453	G11
3454	H7
3455	H10
3456	H5
3457	H5
3458	H11
3459	H13
3460	H14
3461	H7
3462	H7
3463	H13
3464	H12
3465	I13
3466	G14
4401	A9
5401	C8
5402	D9
6401	B4
6402	B5
6403	B5
6404	B8
6405	B4
6406	B5
6407	B6
6408	B9
6409	B10
6410	B11
6411	B11
6412	B12
6413	B13
6414	B14
6415	B14
6416	B4
6417	B11
6418	B6
6419	B7
6420	B7
6421	B8
6422	C12
6423	C12
6424	C6
6425	C6
7401	B2
7402	C2
7403	C7
7404	C1
7405	C6
7406	D7
7407	D7
7408	D5
7409	D6
7410	E8
7411	G4
7412	G14
7413	H13
7414	H6
7415	H11
7416	I4
F4001	A6
F4002	A6
F4003	A6
F4006	A6
F4007	A6
F4008	A5
F4010	A5
F4011	A5
F4015	A4
F4016	A4
F4019	A4
F4020	A4
F4021	A4
F4101	A12
F4102	A12
F4103	A12
F4106	A12
F4107	A12
F4108	A11
F4110	A11
F4111	A11
F4115	A10
F4116	A10
F4119	A10
F4120	A10
F4201	G1
F4202	G1
F4203	G1
F4204	G2
F4205	G2
F4206	G2
F4207	G2
F4209	G2
F4210	F2
F4211	F2
F4213	F2
F4215	F1
F4701	C13
F4703	C13
F4705	D13
F4707	D13
F4709	D13
F4712	D13
F4714	D13
F4716	D13
F4718	E13
F4720	E13
F4721	E13
F4722	E13
I401	B3
I402	B2
I403	C2
I404	C2
I405	C1
I406	C5
I407	D6
I408	D8
I409	D9
I410	E1
I411	E7
I413	E7
I414	E9
I415	E7
I416	E9
I417	E7
I418	F7
I419	F9
I421	F7
I422	F9
I424	G7
I425	G7
I426	G4
I427	G7
I428	G4
I429	G4
I430	G7
I431	G13
I432	G7
I433	G7
I434	G7
I435	G13
I436	H7
I437	H14
I438	H7
I439	H13
I440	H4
I441	H13
I442	I3
I443	I3
I444	C7
I445	C7
I459	G9
I461	H7
I462	H5

MOBO: Audio In/Out (IOA)


from PS
5VSTBY
5NSTBY
7501
HEF4052B
7504
HEF4052B
MDX
VDD
VEE VSS
G4
7500-2
MC33078D
7500-1
MC33078D
7503-2
MC33078D
7503-1
MC33078D
false type
7505
BC817-25W
7507
BC817-25W
RSA2
RSA1
from MSP
AINFR
from IOV
AINFL
from IOV
AIN2L
from IOV
AIN2R
from IOV
AIN1L
from IOV
AIN1R
from IOV
IMUTE
from CU
ASC1
from IOA
AFER
from MSP
AFEL
from MSP
ALDAC
from DAC_ADC
ARDAC
from DAC_ADC
ARADC
to DAC_ADC
ALADC
to DAC_ADC
AOUT1L
to IOV
AOUT1R
to IOV
AKILL
from DAC_ADC
0V
I502 ARADC
I509 ALADC
I524 AOUT1R
I514 AOUT1L
3
TR20008_002.eps
30062004

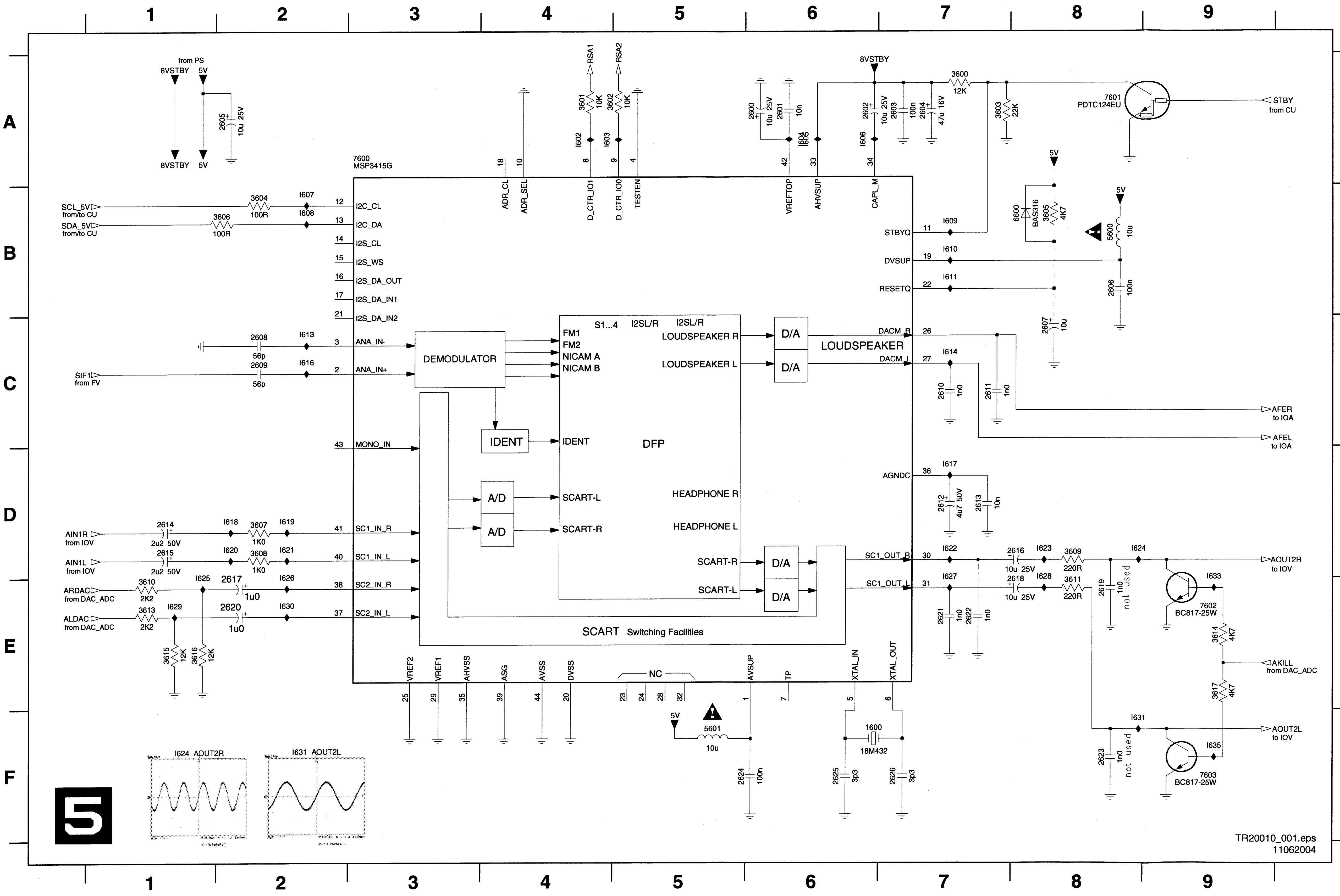
2500	A8
2501	A9
2502	A7
2503	B7
2504	B2
2505	B2
2506	B2
2507	C2
2508	C2
2509	C2
2510	C7
2511	D2
2512	D8
2513	D2
2514	D8
2515	D7
2516	D2
2517	D2
2518	E8
2519	E8
2520	B6
2521	C6
3500	B6
3501	C6
3502	C4
3503	C5
3504	C4
3505	C4
3506	D6
3507	D7
3508	D8
3509	D9
3510	E2
3511	E2
3512	E3
3513	E3
3514	E3
3515	E4
3516	E6
3517	E7
3518	E8
3519	E9
3521	D8
3522	E8
7500-1	B7
7500-2	B7
7501	A5
7503-1	E7
7503-2	D7
7504	C5
7505	D9
7507	E9
I500	A5
I501	B5
I502	B9
I504	B3
I505	B2
I507	B2
I509	C9
I510	C5
I511	D2
I512	D5
I514	D9
I519	D6
I521	D5
I524	E9
I525	E6
I534	D3
I541	D6
I542	D8

MOBO: Power Supply (PS)


I321 Vgate (Standby)
I322 VSource (Standby)
F328 VDrain (Standby)
I321 Vgate (No Disc)
I322 VSource (No Disc)
F328 VDrain (No Disc)
MAINS CONN
1931
B2P3-VH
1303 PTF/65
1305 T1A25 5ET
5302 HF2022R
5300 SRW28EC9-E02V0133
7307 STP3NK60ZFP
7311 TEA1507
DRAIN HVS DRIVER SENSE
VCC GND CTRL DEMAG
7316 TCET1108G
7319 TL431
7300 STS9NF30L
7301 TL431
7302 STP16NF06FP
7303 TL431
7304 STS9NF30L
7305 TL431
7321 SI2306DS
7322 SI2306DS
7306 SI2306DS
7323 BC847BW
7324 PDTC124EU
7308 PDTC124EU
7309 SI2301DS
7310 BF422
7312 BC857BW
7313 BC847BW
7314 BC847BW
7318 BC547B
7325 SI2306DS
5VSTBY
to IOV, IOA, FV
5V
to DAC_ADC, IOA, DIGIO, MSP
3V3SW
to DAC_ADC, CU
12VSTBY
to IOV, CU
STBY
from CU
DD_ON
from CU
5NSTBY
to IOV, IOA, DAC_ADC
5N
to MSP
33VSTBY
to FV
VGNSTBY
to CU
IPFAIL
to DAC_ADC
8VSTBY
to MSP
GND
GNDHOT
GNDreg
to Digital Board
1932
B12P-PH-K
FEBE used
to Basic Engine
1934
B4B-EH-A
not used
4304
GND1
TR20009_002.eps
30062004
4

1300	A12
1301	A13
1302	B3
1303	B2
1304	B9
1305	B2
1306	D13
1308	E8
1310	H13
1931	C1
1932	D1
1934	G1
2300	A11
2301	A6
2302	B8
2303	B9
2304	B11
2305	D2
2306	B4
2307	B10
2308	C6
2309	C8
2310	C9
2311	C2
2312	C11
2313	C6
2314	C10
2315	C4
2316	D8
2317	D9
2318	D4
2319	E3
2320	F10
2321	E8
2322	E9
2323	E4
2324	G11
2325	G12
2326	G5
2327	G8
2328	G9
2329	I12
2330	H4
2331	H4
2333	H6
2334	I4
2335	I8
2336	I9
3300	A6
3301	A6
3302	A11
3303	A12
3304	A13
3305	A13
3306	A13
3307	A11
3308	A12
3309	A9
3310	A10
3311	B11
3312	B9
3313	B10
3314	B11
3315	B12
3316	B3
3317	C11
3318	C2
3319	C9
3320	C10
3321	C5
3322	C5
3323	C6
3324	C11
3325	C12
3326	D12
3327	D12
3328	E12
3329	E3
3330	E4
3331	E4
3332	F9
3333	F10
3334	F4
3335	F12
3336	F12
3337	G11
3338	F7
3339	G12
3340	G12
3341	G4
3342	G5
3343	G5
3344	G7
3345	G3
3346	G4
3347	H11
3348	H8
3349	I11
3350	I11
3351	H6
3353	H7
3354	H10
3355	H8
3356	H9
3357	H6
3358	H7
3359	H7
3361	I4
3362	I6
3363	I7
3365	B12
3366	E10
3367	E10
3368	E11
3369	E10
3370	F2
4304	H2
5300	A6
5301	B8
5302	C3
5303	A9
5304	D9
5305	D6
5306	E9
5307	G9
6300	A7
6301	B7
6302	B4
6303	B5
6304	B7
6305	C5
6306	C7
6307	C4
6308	D6
6309	D7
6310	E5
6311	E8
6312	E7
6313	F11
6314	F7
6315	G11
6316	G13
6317	G4
6318	G9
6319	H4
6320	I12
6321	I9
6322	I9
7300	A10
7301	A11
7302	B10
7303	B11
7304	C10
7305	C11
7306	D11
7307	D3
7308	D13
7309	F10
7310	F13
7311	G3
7312	H12
7313	H8
7314	H8
7316	H5
7318	I10
7319	I6
7321	B13
7322	D10
7323	E10
7324	E11
7325	E2
9300	E1
F300	A11
F301	A12
F302	A11
F303	A12
F304	A6
F305	A12
F306	A12
F307	A7
F308	B5
F309	B1
F310	B2
F3101	B1
F3102	C1
F311	B3
F312	B7
F313	B8
F314	B9
F315	B9
F316	C8
F317	C8
F318	C7
F319	C1
F320	D12
F3201	E1
F3206	E2
F3209	E2
F321	D13
F3211	F2
F322	D12
F323	D13
F324	D7
F325	D8
F326	D13
F327	E1
F328	E3
F329	E2
F330	F12
F331	F13
F332	E7
F333	E8
F334	E8
F336	E8
F337	E9
F338	F2
F339	F13
F340	F13
F3401	G1
F3404	G1
F341	G3
F342	G6
F343	G8
F344	H12
F345	H13
F346	H12
F347	H13
F348	H11
F349	H12
F350	H11
F351	I8
F352	I6
I300	A6
I301	A12
I302	A7
I303	A10
I304	B8
I305	B10
I306	B12
I308	B9
I309	B3
I310	B4
I311	B10
I312	B4
I313	B5
I314	C4
I315	C12
I316	C10
I317	C10
I318	C6
I319	D6
I320	D12
I321	D3
I322	E5
I323	F3
I324	F3
I325	F10
I326	F7
I327	F11
I328	F12
I329	F12
I330	F7
I331	F6
I332	G12
I333	G11
I334	G4
I336	G4
I337	I12
I338	H5
I339	I11
I340	H6
I341	H8
I343	I3
I344	H6
I345	H10
I346	I8
I347	I6
I349	I7
I353	I10
I354	B13
I355	E1
I356	E10
I358	E11
I359	D11
I360	H7
I361	I10
c300	B8

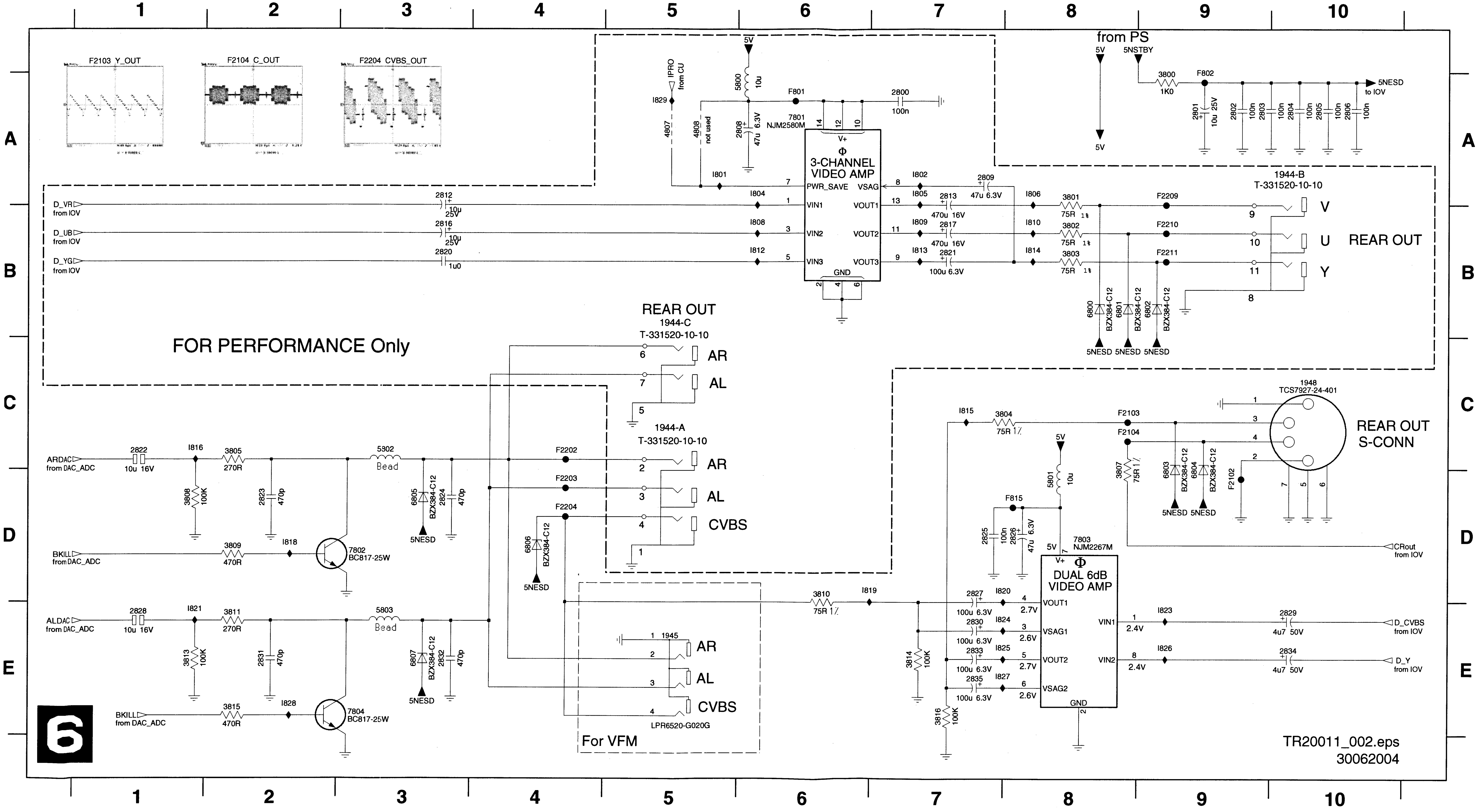
MOBO: Multi Sound Processing (MSP)


1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
from PS
8VSTBY
5V
2605
10u 25V
7600
MSP3415G
RSA1
RSA2
3601
10K
3602
10K
I602
I603
ADR_CL
ADR_SEL
D_CTR_IO1
D_CTR_IO0
TESTEN
2600
10u 25V
2601
10n
I604
I605
VREFTOP
AHVSUP
I606
CAPL_M
2602
10u 25V
2603
100n
2604
47u 16V
3600
12K
3603
22K
7601
PDTC124EU
STBY
from CU
SCL_5V
from/to CU
SDA_5V
from/to CU
3604
100R
3606
100R
I607
I608
I2C_CL
I2C_DA
I2S_CL
I2S_WS
I2S_DA_OUT
I2S_DA_IN1
I2S_DA_IN2
STBYQ
DVSUP
RESETQ
I609
I610
I611
6600
BAS316
3605
4K7
5600
10u
2606
100n
2607
10u
2608
56p
2609
56p
I613
I616
SIF1
from FV
ANA_IN-
ANA_IN+
DEMODULATOR
S1...4
I2SL/R
FM1
FM2
NICAM A
NICAM B
LOUDSPEAKER R
LOUDSPEAKER L
D/A
LOUDSPEAKER
DACM_R
DACM_L
I614
2610
1n0
2611
1n0
AFER
to IOA
AFEL
to IOA
MONO_IN
IDENT
DFP
AGNDC
I617
2612
4u7 50V
2613
10n
A/D
SCART-L
SCART-R
HEADPHONE R
HEADPHONE L
AIN1R
from IOV
AIN1L
from IOV
2614
2u2 50V
2615
2u2 50V
I618
3607
1K0
I619
I620
3608
1K0
I621
SC1_IN_R
SC1_IN_L
SC2_IN_R
SC2_IN_L
ARDAC
from DAC_ADC
ALDAC
from DAC_ADC
3610
2K2
3613
2K2
I625
2617
1u0
I626
I629
2620
1u0
I630
3615
12K
3616
12K
SCART Switching Facilities
SC1_OUT_R
SC1_OUT_L
I622
I627
2616
10u 25V
2618
10u 25V
I623
I628
3609
220R
3611
220R
I624
2619
1n0
not used
2621
1n0
2622
1n0
AOUT2R
to IOV
I633
7602
BC817-25W
3614
4K7
AKILL
from DAC_ADC
3617
4K7
I631
AOUT2L
to IOV
2623
1n0
not used
I635
7603
BC817-25W
VREF2
VREF1
AHVSS
ASG
AVSS
DVSS
NC
AVSUP
TP
XTAL_IN
XTAL_OUT
5601
10u
2624
100n
1600
18M432
2625
3p3
2626
3p3
I624 AOUT2R
I631 AOUT2L
5
TR20010_001.eps
11062004

1600	F6
2600	A6
2601	A6
2602	A6
2603	A7
2604	A7
2605	A2
2606	B8
2607	C8
2608	C2
2609	C2
2610	C7
2611	C7
2612	D7
2613	D7
2614	D1
2615	D1
2616	D8
2617	E2
2618	E8
2619	E8
2620	E2
2621	E7
2622	E7
2623	F8
2624	F5
2625	F6
2626	F7
3600	A7
3601	A4
3602	A4
3603	A7
3604	B2
3605	B8
3606	B2
3607	D2
3608	D2
3609	D8
3610	E1
3611	E8
3613	E1
3614	E9
3615	E1
3616	E1
3617	E9
5600	B8
5601	F5
6600	B8
7600	A3
7601	A8
7602	E9
7603	F9
I602	A4
I603	A4
I604	A6
I605	A6
I606	A6
I607	B2
I608	B2
I609	B7
I610	B7
I611	B7
I613	C2
I614	C7
I616	C2
I617	D7
I618	D2
I619	D2
I620	D2
I621	D2
I622	D7
I623	D8
I624	D8
I625	D1
I626	D2
I627	D7
I628	D8
I629	E1
I630	E2
I631	F8
I633	D9
I635	F9

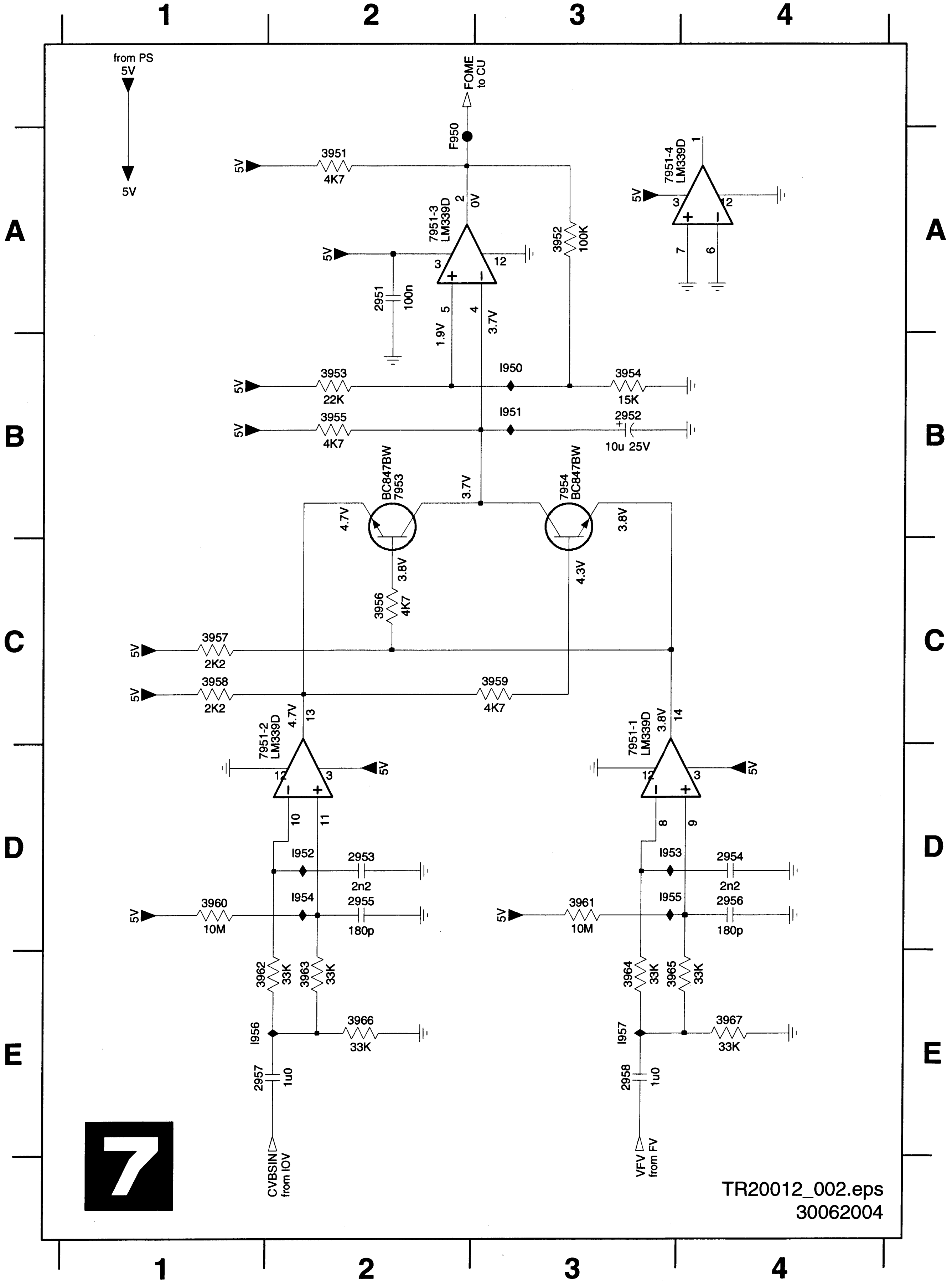
MOBO: Cinch Out (CINCH)

1944-A C5
1944-B A10
1944-C B5
1945 E5
1948 C10
2800 A7
2801 A9
2802 A9
2803 A9
2804 A10
2805 A10
2806 A10
2808 A6
2809 A7
2812 A3
2813 A7
2816 B3
2817 B7
2820 B3
2821 B7
2822 C1
2823 D2
2824 D3
2825 D7
2826 D8
2827 D7
2828 E1
2829 E10
2830 E7
2831 E2
2832 E3
2833 E7
2834 E10
2835 E7
3800 A9
3801 A8
3802 B8
3803 B8
3804 C7
3805 C2
3807 C8
3808 D1
3809 D2
3810 D6
3811 E2
3813 E1
3814 E7
3815 E2
3816 E7
4807 A5
4808 A5
5800 A6
5801 D8
5802 C3
5803 E3
6800 B8
6801 B8
6802 B9
6803 C9
6804 C9
6805 D3
6806 D4
6807 E3
7801 A6
7802 D3
7803 D8
7804 E3
F2102 D9
F2103 C8
F2104 C8
F2202 C4
F2203 D4
F2204 D4
F2209 A9
F2210 B9
F2211 B9
F801 A6
F802 A9
F815 D8
I801 A5
I802 A7
I804 A6
I805 A7
I806 A8
I808 B6
I809 B7
I810 B8
I812 B6
I813 B7
I814 B8
I815 C7
I816 C1
I818 D2
I819 D6
I820 D7
I821 E1
I823 E9
I824 E7
I825 E7
I826 E9
I827 E7
I828 E2
I829 A5


1
2
3
4
5
6
7
8
9
10
A
B
C
D
E
F2103 Y_OUT
F2104 C_OUT
F2204 CVBS_OUT
IPRO from CU
I829
4807
4808 not used
5V
5800 10u
2808 47u 6.3V
F801
7801 NJM2580M
3-CHANNEL VIDEO AMP
V+
PWR_SAVE
VSAG
VIN1
VIN2
VIN3
VOUT1
VOUT2
VOUT3
GND
2800 100n
from PS
5V
5NSTBY
3800 1K0
F802
5NESD to IOV
2801 10u 25V
2802 100n
2803 100n
2804 100n
2805 100n
2806 100n
I801
I802
2809 47u 6.3V
I804
I805
2813 470u 16V
I806
3801 75R 1%
F2209
1944-B T-331520-10-10
V
U
Y
REAR OUT
D_VR from IOV
2812 10μ 25V
D_UB from IOV
2816 10μ 25V
D_YG from IOV
2820 1u0
I808
I809
2817 470u 16V
I810
3802 75R 1%
F2210
I812
I813
2821 100u 6.3V
I814
3803 75R 1%
F2211
6800 BZX384-C12
6801 BZX384-C12
6802 BZX384-C12
5NESD
FOR PERFORMANCE Only
REAR OUT
1944-C T-331520-10-10
AR
AL
1944-A T-331520-10-10
AR
AL
CVBS
ARDAC from DAC_ADC
2822 10u 16V
I816
3805 270R
5302 Bead
F2202
F2203
F2204
3808 100K
2823 470p
6805 BZX384-C12
2824 470p
6806 BZX384-C12
BKILL from DAC_ADC
3809 470R
I818
7802 BC817-25W
ALDAC from DAC_ADC
2828 10u 16V
I821
3811 270R
5803 Bead
3813 100K
2831 470p
6807 BZX384-C12
2832 470p
BKILL from DAC_ADC
3815 470R
I828
7804 BC817-25W
1945
AR
AL
CVBS
LPR6520-G020G
For VFM
3810 75R 1%
I819
I815
3804 75R 1%
F2103
F2104
1948 TCS7927-24-401
REAR OUT S-CONN
3807 75R 1%
6803 BZX384-C12
6804 BZX384-C12
F2102
5801 10u
F815
2825 100n
2826 47u 6.3V
7803 NJM2267M
DUAL 6dB VIDEO AMP
VOUT1
VSAG1
VOUT2
VSAG2
VIN1
VIN2
GND
2827 100u 6.3V
I820
2.7V
2830 100u 6.3V
I824
2.6V
2833 100u 6.3V
I825
2.7V
2835 100u 6.3V
I827
2.6V
3814 100K
3816 100K
I823
2829 4u7 50V
D_CVBS from IOV
2.4V
I826
2834 4u7 50V
D_Y from IOV
2.4V
CRout from IOV
6
TR20011_002.eps
30062004

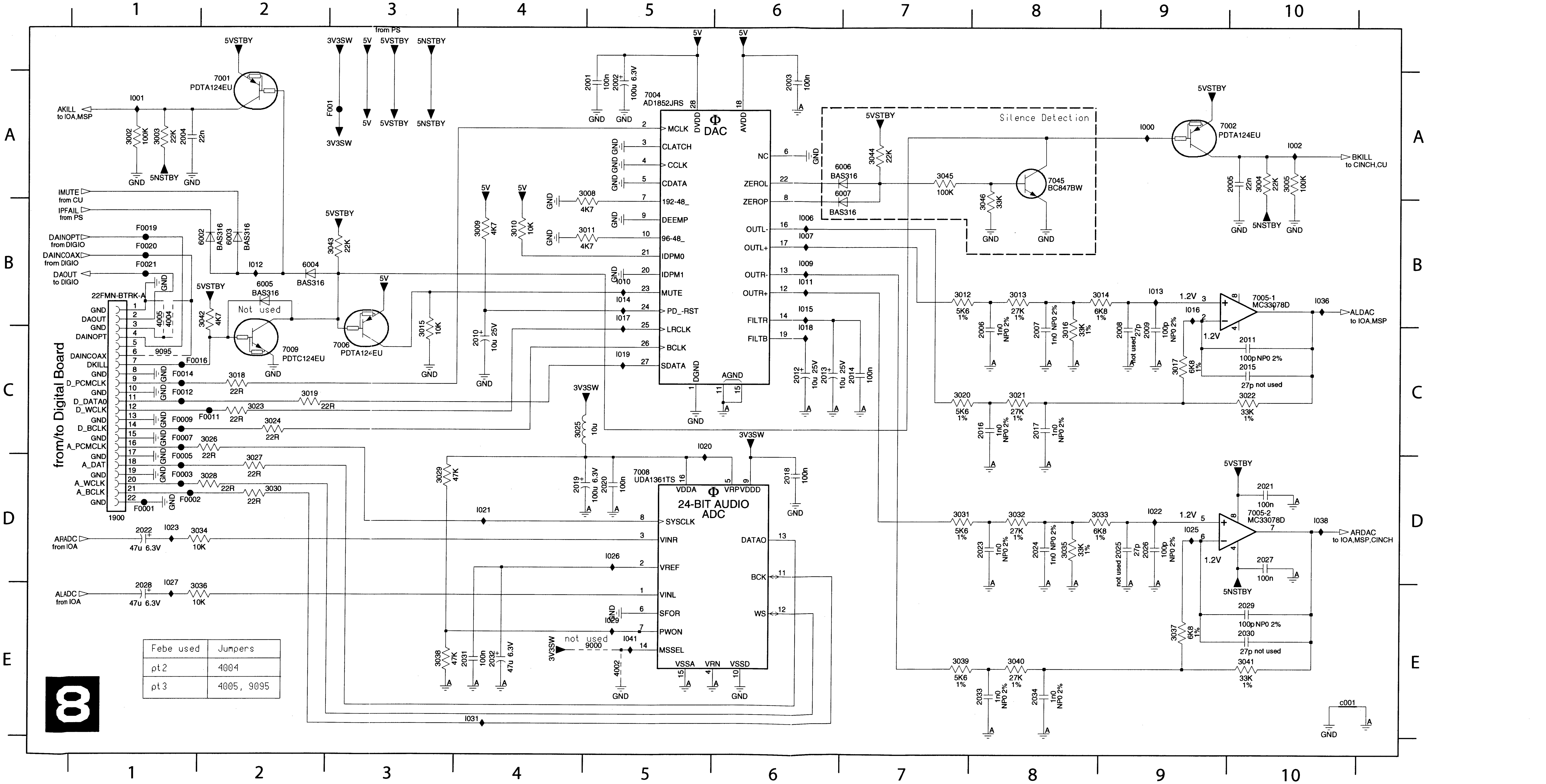
MOBO Board: Follow Me (FOME)

2951 A2	2956 D4	3953 B2	3958 C1	3963 E2	7951-1 D3	7954 B3	I953 D3
2952 B3	2957 E1	3954 B3	3959 C3	3964 E3	7951-2 D1	F950 A2	I954 D2
2953 D2	2958 E3	3955 B2	3960 D1	3965 E3	7951-3 A2	I950 B3	I955 D3
2954 D4	3951 A2	3956 C2	3961 D3	3966 E2	7951-4 A3	I951 B3	I956 E1
2955 D2	3952 A3	3957 C1	3962 E1	3967 E4	7953 B2	I952 D2	I957 E3

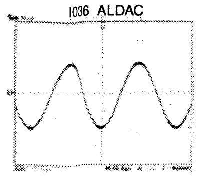

1
2
3
4
A
B
C
D
E
from PS
5V
FOME
to CU
F950
3951
4K7
7951-3
LM339D
0V
3952
100K
7951-4
LM339D
2951
100n
1.9V
3.7V
3953
22K
I950
3954
15K
3955
4K7
I951
2952
10u 25V
BC847BW
7953
7954
BC847BW
4.7V
3.7V
3.8V
3.8V
4.3V
3956
4K7
3957
2K2
3958
2K2
3959
4K7
7951-2
LM339D
7951-1
LM339D
I952
2953
2n2
I953
2954
2n2
3960
10M
I954
2955
180p
3961
10M
I955
2956
180p
3962
33K
3963
33K
3964
33K
3965
33K
I956
3966
33K
I957
3967
33K
2957
1u0
2958
1u0
CVBSIN
from IOV
VFV
from FV
7
TR20012_002.eps
30062004

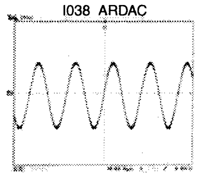
MOBO Board: Audio Converter (DAC_ADC)

1900 D1
2001 A5
2002 A5
2003 A6
2004 A1
2005 A10
2006 C8
2007 C8
2008 C9
2009 C9
2010 C4
2011 C10
2012 C6
2013 C6
2014 C7
2015 C10
2016 C8
2017 C8
2018 D6
2019 D4
2020 D5
2021 D10
2022 D1
2023 D8
2024 D8
2025 D9
2026 D9
2027 D10
2028 E1
2029 E10
2030 E10
2031 E4
2032 E4
2033 E8
2034 E8
3002 A1
3003 A1
3004 A10
3005 A10
3008 A5
3009 B4
3010 B4
3011 B5
3012 B7
3013 B8
3014 B9
3015 C3
3016 C8
3017 C9
3018 C2
3019 C2
3020 C7
3021 C8
3022 C10
3023 C2
3024 C2
3025 C4
3026 C2
3027 D2
3028 D2
3029 D3
3030 D2
3031 D7
3032 D8
3033 D9
3034 D2
3035 D8
3036 E2
3037 E9
3038 E3
3039 E7
3040 E8
3041 E10
3042 B2
3043 B3
3044 A7
3045 A7
3046 B8
4002 E5
4004 B1
4005 B1
6002 B2
6003 B2
6004 B2
6005 B2
6006 A7
6007 A7
7001 A2
7002 A9
7004 A5
7005-1 B10
7005-2 D10
7006 C3
7008 D5
7009 C2
7045 A8
9000 E5
9095 C1
F0001 D1
F0002 D1
F0003 D1
F0005 D1
F0007 C1
F0009 C1
F001 A3
F0011 C2
F0012 C1
F0014 C1
F0016 C1
F0019 B1
F0020 B1
F0021 B1
I000 A9
I001 A1
I002 A10
I006 B6
I007 B6
I009 B6
I010 B5
I011 B6
I012 B2
I013 B9
I014 B5
I015 B6
I016 B9
I017 B5
I018 C6
I019 C5
I020 C5
I021 D4
I022 D9
I023 D1
I025 D9
I026 D5
I027 E1
I029 E5
I031 E4
I036 B10
I038 D10
I041 E5
c001 E10


1
2
3
4
5
6
7
8
9
10
A
B
C
D
E
from PS
5VSTBY
3V3SW
5V
5NSTBY
F001
7001
PDTA124EU
AKILL
to IOA,MSP
I001
3002 100K
3003 22K
2004 22n
GND
5NSTBY
IMUTE
from CU
IPFAIL
from PS
DAINOPT
from DIGIO
DAINCOAX
from DIGIO
DAOUT
to DIGIO
F0019
F0020
F0021
6002 BAS316
6003 BAS316
I012
6004 BAS316
6005 BAS316
3043 22K
22FMN-BTRK-A
3042 4K7
Not used
7009
PDTC124EU
7006
PDTA124EU
3015 10K
4005
4004
9095
F0016
from/to Digital Board
GND
DAOUT
DAINOPT
DAINCOAX
DKILL
D_PCMCLK
D_DATA0
D_WCLK
D_BCLK
A_PCMCLK
A_DAT
A_WCLK
A_BCLK
1900
F0014
F0012
F0011
F0009
F0007
F0005
F0003
F0002
F0001
3018 22R
3019 22R
3023 22R
3024 22R
3026 22R
3027 22R
3028 22R
3030 22R
2001 100n
2002 100u 6.3V
7004
AD1852JRS
DAC
DVDD
AVDD
MCLK
CLATCH
CCLK
CDATA
192-48_
DEEMP
96-48_
IDPM0
IDPM1
MUTE
PD_-RST
LRCLK
BCLK
SDATA
DGND
AGND
NC
ZEROL
ZEROP
OUTL-
OUTL+
OUTR-
OUTR+
FILTR
FILTB
2003 100n
3008 4K7
3011 4K7
3009 4K7
3010 10K
2010 10u 25V
I010
I014
I017
I019
I006
I007
I009
I011
I015
I018
2012 10u 25V
2013 10u 25V
2014 100n
Silence Detection
3044 22K
6006 BAS316
6007 BAS316
3045 100K
3046 33K
7045
BC847BW
I000
7002
PDTA124EU
I002
BKILL
to CINCH,CU
2005 22n
3004 22K
3005 100K
3012 5K6 1%
3013 27K 1%
3014 6K8 1%
I013
1.2V
7005-1
MC33078D
I036
ALDAC
to IOA,MSP
I016
2006 1n0 NP0 2%
2007 1n0 NP0 2%
3016 33K 1%
2008 not used 27p
2009 100p NP0 2%
2011 100p NP0 2%
2015 27p not used
3017 6K8 1%
3020 5K6 1%
3021 27K 1%
3022 33K 1%
2016 1n0 NP0 2%
2017 1n0 NP0 2%
3V3SW
3025 10u
I020
2019 100u 6.3V
2020 100n
7008
UDA1361TS
24-BIT AUDIO ADC
VDDA
VRPVDDD
SYSCLK
VINR
VREF
VINL
SFOR
PWON
MSSEL
DATAO
BCK
WS
VSSA
VRN
VSSD
2018 100n
3029 47K
I021
ARADC
from IOA
2022 47u 6.3V
I023
3034 10K
I026
ALADC
from IOA
2028 47u 6.3V
I027
3036 10K
I029
not used 9000
I041
4002
3038 47K
2031 100n
2032 47u 6.3V
I031
3031 5K6 1%
3032 27K 1%
3033 6K8 1%
I022
I025
7005-2
MC33078D
I038
ARDAC
to IOA,MSP,CINCH
2021 100n
2027 100n
2023 1n0 NP0 2%
2024 1n0 NP0 2%
3035 33K 1%
2025 not used 27p
2026 100p NP0 2%
2029 100p NP0 2%
2030 27p not used
3037 6K8 1%
3039 5K6 1%
3040 27K 1%
3041 33K 1%
2033 1n0 NP0 2%
2034 1n0 NP0 2%
c001
8

Febe used	Jumpers
pt2	4004
pt3	4005, 9095





TR20013_002.eps
30062004

MOBO Board: Control Unit (CU)

0005 I14
0007 I15
1100 B14
1101 B7
1102 E6
1911 A15
1913 C1
1915 G1
1917 B3
2100 A7
2101 A9
2102 A10
2103 A10
2104 A11
2105 A12
2106 A5
2107 A13
2108 B9
2109 B9
2110 B6
2111 B10
2112 B12
2113 B13
2114 B10
2115 C5
2116 C1
2117 C11
2118 C11
2119 D11
2120 D11
2121 D11
2122 D11
2123 E2
2124 E3
2126 E11
2127 E6
2128 E2
2129 E6
2130 F2
2131 G1
2132 G5
2133 G11
2134 G5
2135 H11
2136 I5
2137 I3
2138 I3
2139 B9
2140 B12
2141 A2
2188 H4
2189 C8
3094 B14
3095 B14
3096 B14
3097 H14
3098 H14
3099 I14
3101 A5
3102 A6
3103 A9
3104 A11
3105 A2
3106 A7
3108 A11
3109 A8
3110 A11
3111 B13
3112 B10
3113 B12
3114 B5
3115 B6
3116 B13
3117 B10
3118 B2
3119 B7
3120 B5
3121 B6
3122 C3
3123 C2
3124 C6
3125 C7
3126 C3
3127 C3
3128 C12
3130 C12
3131 D2
3132 D12
3133 D1
3134 D12
3135 D1
3136 D7
3137 D12
3138 D3
3139 D3
3140 E3
3141 E2
3142 E12
3143 E8
3144 E12
3145 E1
3146 E2
3147 E1
3148 E8
3149 E8
3150 E3
3151 F5
3152 F5
3153 F1
3154 F2
3155 F5
3156 F2
3157 F5
3158 F1
3159 F7
3160 G5
3161 G11
3162 G12
3163 G5
3164 G6
3165 G6
3166 G6
3167 G6
3168 G7
3169 G7
3170 G7
3171 G8
3172 H2
3173 H3
3174 H3
3175 H11
3176 H12
3177 H8
3178 H1
3179 I8
3180 I4
3181 I8
3182 I3
3183 G3
3184 H9
3185 I9
3186 I9
3187 G6
3188 H4
3189 F4
3190 F4
3196 B5
3197 C5
3198 C5
3199 D5
5100 A9
5101 B12
6100 A10
6101 B7
6102 B13
6103 B5
6104 F12
6105 G12
6106 G10
6107 G10
6108 H10
6109 H10
6110 H10
6111 H10
6112 I10
6113 H10
6114 I10
6188 G4
7100 A6
7101 A7
7102 A11
7103 B11
7104 B11
7105 B6
7106 C1
7107 B9
7108 C2
7109 E2
7110 F11
7111 G4
7112 G11
7113 G8
7114 H2
7115 H2
7116 H8
7117 H5
7118 I8
7121 H9
7122 I9
7123 C6
7124 D6
9104 B12
F100 A10
F108 A9
F1101 A14
F1102 A14
F1103 A14
F1107 D8
F111 C1
F1301 B1
F1302 C1
F1601 G1
F1602 G1
F1603 G1
F1604 G1
F1605 G1
F1606 G1
F1608 G1
F1609 H1
I101 A1
I102 A1
I104 A9
I105 A1
I106 A11
I107 A7
I108 A1
I109 A7
I110 A11
I1107 D2
I111 A11
I112 B12
I1120 E2
I1122 H8
I113 B13
I114 B10
I115 B11
I116 B14
I117 B8
I118 B8
I119 C8
I120 C8
I121 C10
I122 C10
I123 C10
I124 C10
I125 C10
I126 C8
I127 C8
I128 C10
I129 C10
I130 D8
I131 D10
I132 D10
I134 D10
I135 D10
I136 D8
I137 D10
I138 D10
I139 D10
I140 D8
I141 D8
I142 D10
I143 D10
I144 D10
I145 D8
I146 D10
I147 E10
I148 E10
I149 E8
I150 E10
I151 E8
I152 E10
I153 E8
I154 E10
I155 E10
I156 E8
I157 E10
I158 E10
I159 E8
I160 E10
I161 E10
I162 E10
I163 F8
I164 F10
I165 F10
I166 F8
I167 F10
I168 F10
I169 F8
I170 F8
I171 F10
I172 F10
I173 F8
I174 F10
I175 F10
I176 F11
I177 F8
I178 G8
I179 G8
I180 H11
I181 H9
I182 H14
I183 I7
I184 F8
I185 B6
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I1910 C2
I1911 C3
I1912 E1
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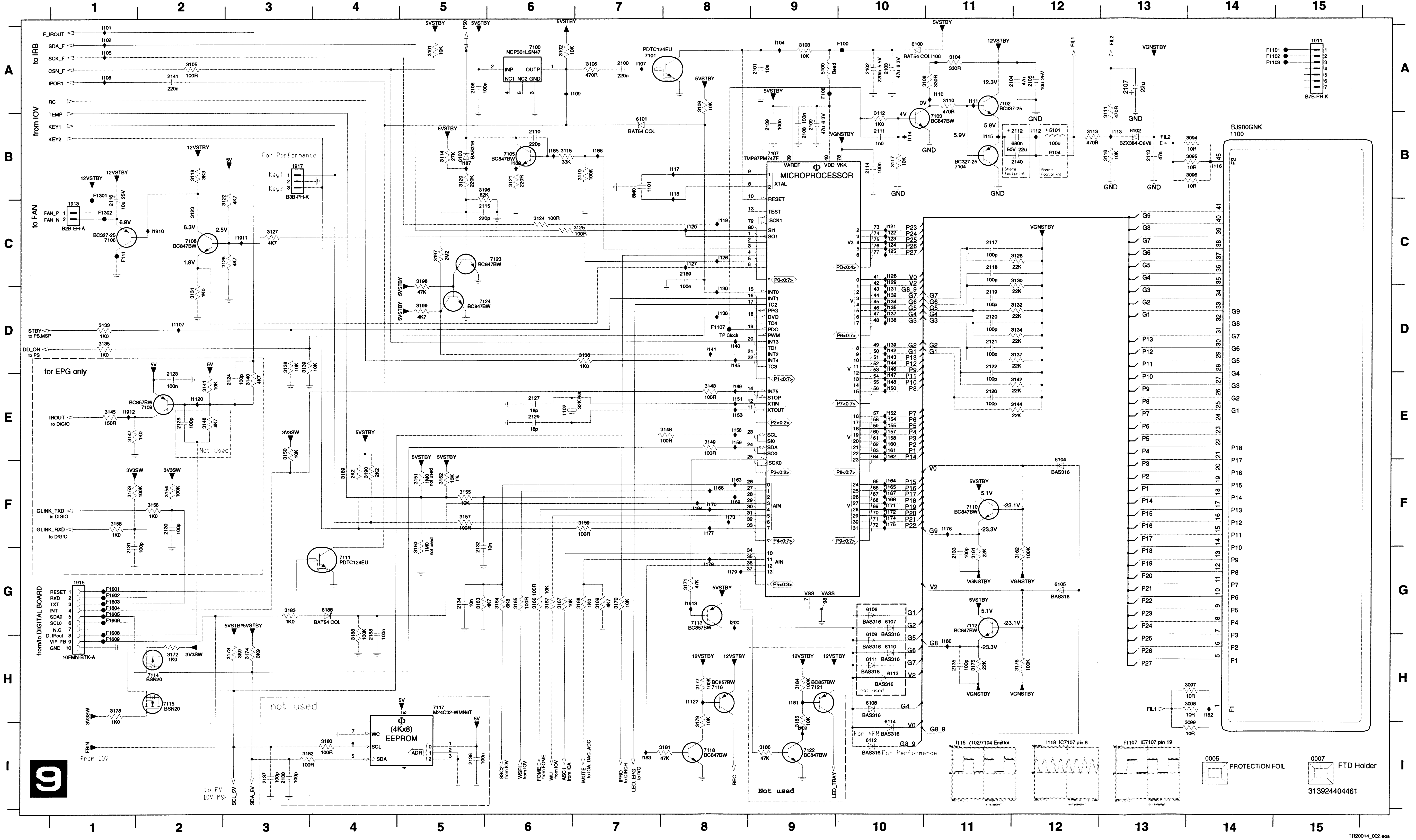
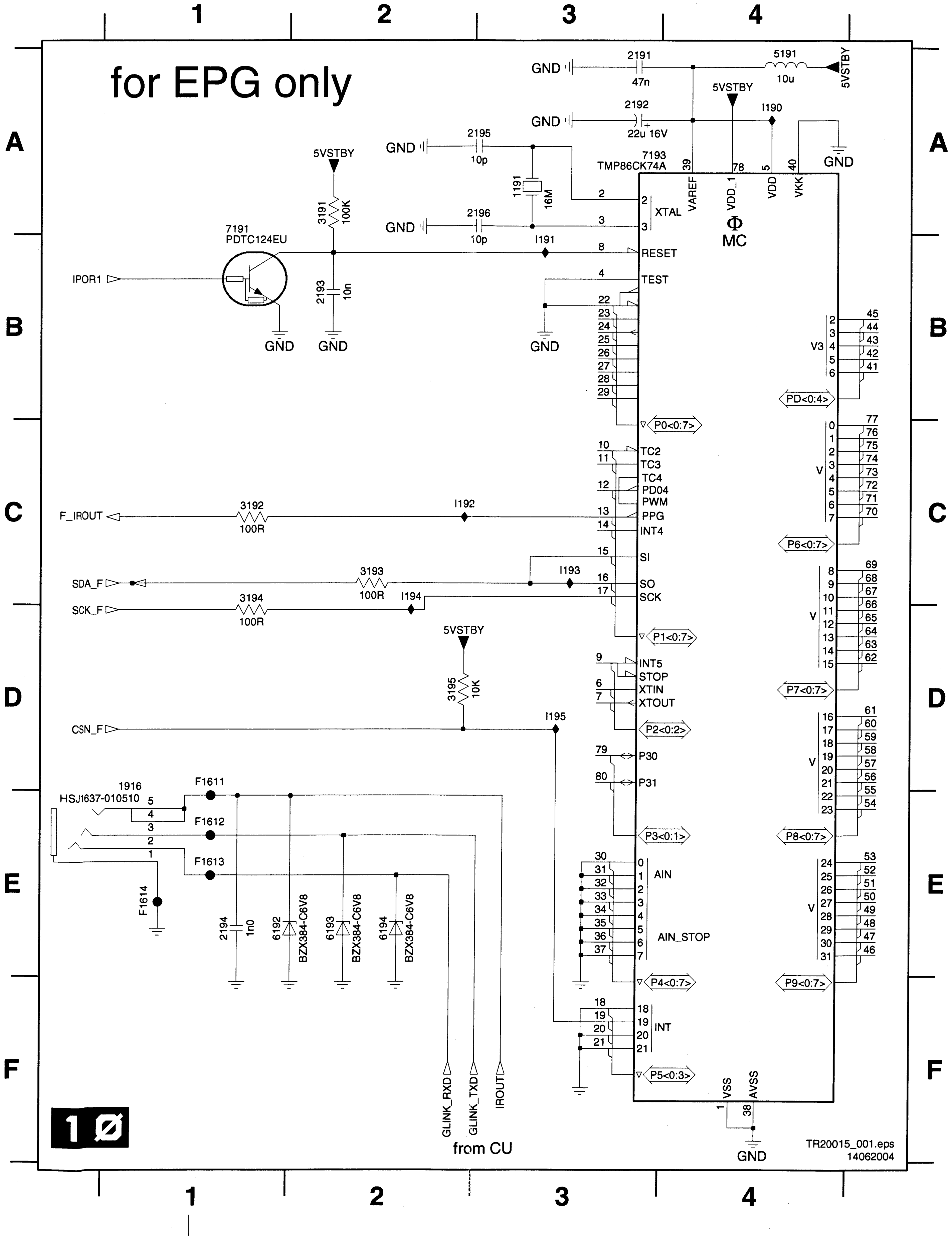
I202 I9


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
A
B
C
D
E
F
G
H
I
to IRB
F_IROUT
SDA_F
SCK_F
CSN_F
IPOR1
from IOV
RC
TEMP
KEY1
KEY2
to FAN
FAN_P
FAN_N
B2B-EH-A
For Performance
Key1
Key2
B3B-PH-K
NCP301LSN47
INP
OUTP
NC1
NC2
GND
PDTC124EU
TMP87PM74ZF
MICROPROCESSOR
VAREF
VDD
VKK
XTAL
RESET
TEST
SCK1
SI1
SO1
INT0
INT1
TC2
PPG
DVO
TC4
PDO
PWM
INT3
TC1
INT2
INT4
TC3
INT5
STOP
XTIN
XTOUT
SCL
SI0
SDA
SO0
SCK0
AIN
VSS
VASS
STBY
to PS,MSP
DD_ON
to PS
for EPG only
IROUT
to DIGIO
Not Used
GLINK_TXD
to DIGIO
GLINK_RXD
to DIGIO
from/to DIGITAL BOARD
RESET
RXD
TXT
INT
SDA0
SCL0
N.C.
D_IRout
VIP_FB
GND
10FMN-BTK-A
BAT54 COL
BSN20
not used
(4Kx8)
EEPROM
M24C32-WMN6T
WC
SCL
SDA
ADR
from IOV
to FV
IOV MSP
SCL_5V
SDA_5V
BSC2
from IOV
WSFI
from IOV
FOME
from FOME
WG
from IOV
ASC1
from IOA
MUTE
to IOA
DAC_ADC
IPRO
to CINCH
LED_EPG
to IVO
REC
LED_TRAY
Not used
For Performance
For VFM
BAS316
BJ900GNK
1100
VGNSTBY
5VSTBY
12VSTBY
3V3SW
FIL1
FIL2
B7B-PH-K
BZX384-C6V8
BC847BW
BC857BW
BC327-25
BC337-25
PDTC124EU
I115 7102/7104 Emitter
I118 IC7107 pin 8
F1107 IC7107 pin 19
0005
PROTECTION FOIL
0007
FTD Holder
313924404461

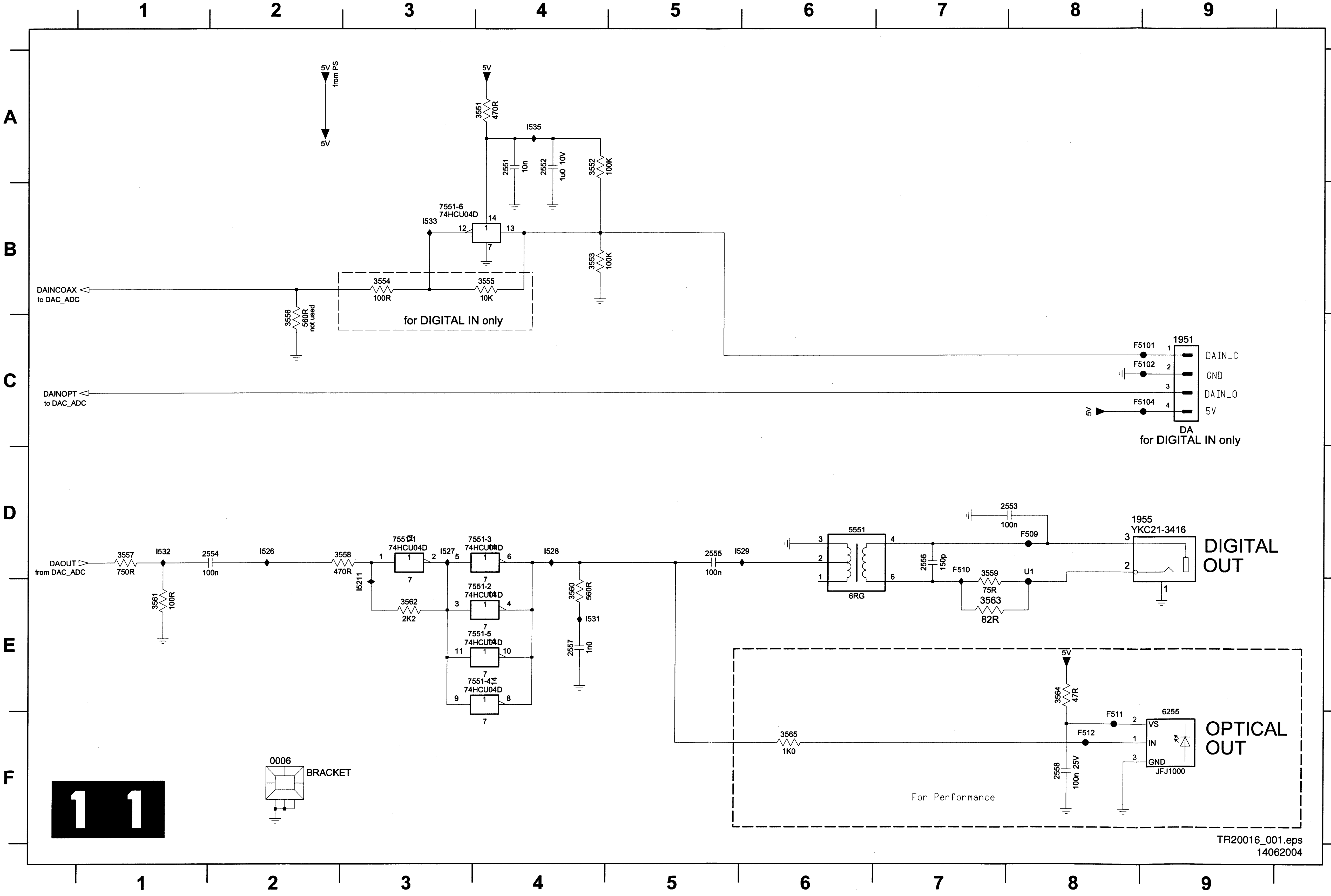
MOBO Board: IR Blaster (IRB)

1191 A3
1916 D1
2191 A3
2192 A3
2193 B2
2194 E1
2195 A3
2196 A3
3191 A2
3192 C1
3193 C2
3194 C1
3195 D2
5191 A4
6192 E1
6193 E2
6194 E2
7191 A1
7193 A4
F1611 D1
F1612 E1
F1613 E1
F1614 E1
I190 A4
I191 B3
I192 C2
I193 C3
I194 C2
I195 D3



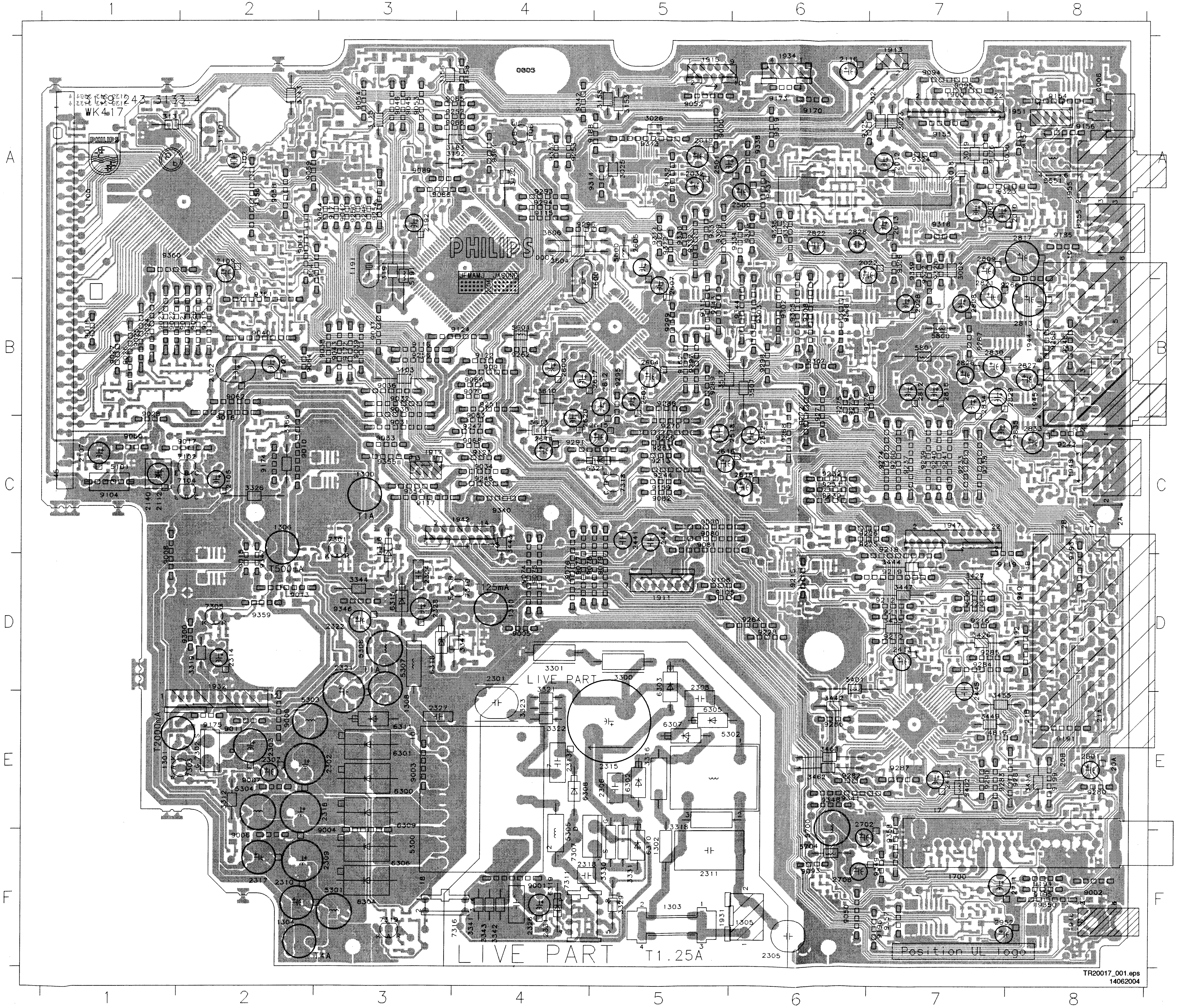
for EPG only
1
2
3
4
A
B
C
D
E
F
GND
2191
47n
5191
10u
5VSTBY
2192
22u 16V
I190
2195
10p
1191
16M
2196
10p
I191
7193
TMP86CK74A
VAREF
VDD_1
VDD
VKK
Φ
MC
XTAL
RESET
TEST
3191
100K
7191
PDTC124EU
IPOR1
2193
10n
V3
PD<0:4>
P0<0:7>
TC2
TC3
TC4
PD04
PWM
PPG
INT4
SI
SO
SCK
F_IROUT
3192
100R
I192
SDA_F
3193
100R
I193
SCK_F
3194
100R
I194
V
P6<0:7>
P1<0:7>
5VSTBY
3195
10K
INT5
STOP
XTIN
XTOUT
P7<0:7>
CSN_F
I195
P2<0:2>
P30
P31
P3<0:1>
P8<0:7>
1916
HSJ1637-010510
F1611
F1612
F1613
F1614
AIN
AIN_STOP
2194
1n0
6192
BZX384-C6V8
6193
BZX384-C6V8
6194
BZX384-C6V8
P4<0:7>
P9<0:7>
INT
P5<0:3>
VSS
AVSS
GLINK_RXD
GLINK_TXD
IROUT
from CU
1 Ø
TR20015_001.eps
14062004

MOBO Board: Digital In/Out 1 (DIGIO 1)


5V from PS
5V
3551 470R
I535
2551 10n
2552 1u0 10V
3552 100K
7551-6 74HCU04D
I533
3553 100K
DAINCOAX to DAC_ADC
3554 100R
3555 10K
for DIGITAL IN only
3556 560R not used
1951
F5101
F5102
F5104
DAIN_C
GND
DAIN_O
5V
DA
for DIGITAL IN only
DAINOPT to DAC_ADC
DAOUT from DAC_ADC
3557 750R
I532
3561 100R
2554 100n
I526
3558 470R
I5211
7551-1 74HCU04D
I527
3562 2K2
7551-3 74HCU04D
7551-2 74HCU04D
7551-5 74HCU04D
7551-4 74HCU04D
I528
3560 560R
I531
2557 1n0
2555 100n
I529
5551
6RG
2553 100n
2556 150p
F509
F510
3559 75R
3563 82R
U1
1955 YKC21-3416
DIGITAL OUT
5V
3564 47R
F511
F512
3565 1K0
2558 100n 25V
6255
VS
IN
GND
JFJ1000
OPTICAL OUT
For Performance
0006
BRACKET
1 1
TR20016_001.eps
14062004

U1	D8
0006	F2
1951	C9
1955	D8
2551	A4
2552	A4
2553	D8
2554	D2
2555	D5
2556	D7
2557	E4
2558	F8
3551	A4
3552	A4
3553	B4
3554	B3
3555	B4
3556	C2
3557	D1
3558	D3
3559	D7
3560	E4
3561	E1
3562	E3
3563	E7
3564	E8
3565	F6
5551	D6
6255	F9
7551-1	D3
7551-2	E4
7551-3	D4
7551-4	E4
7551-5	E4
7551-6	B3
F509	D8
F510	D7
F5101	C9
F5102	C9
F5104	C9
F511	F8
F512	F8
I5211	E3
I526	D2
I527	D3
I528	D4
I529	D6
I531	E4
I532	D1
I533	B3
I535	A4

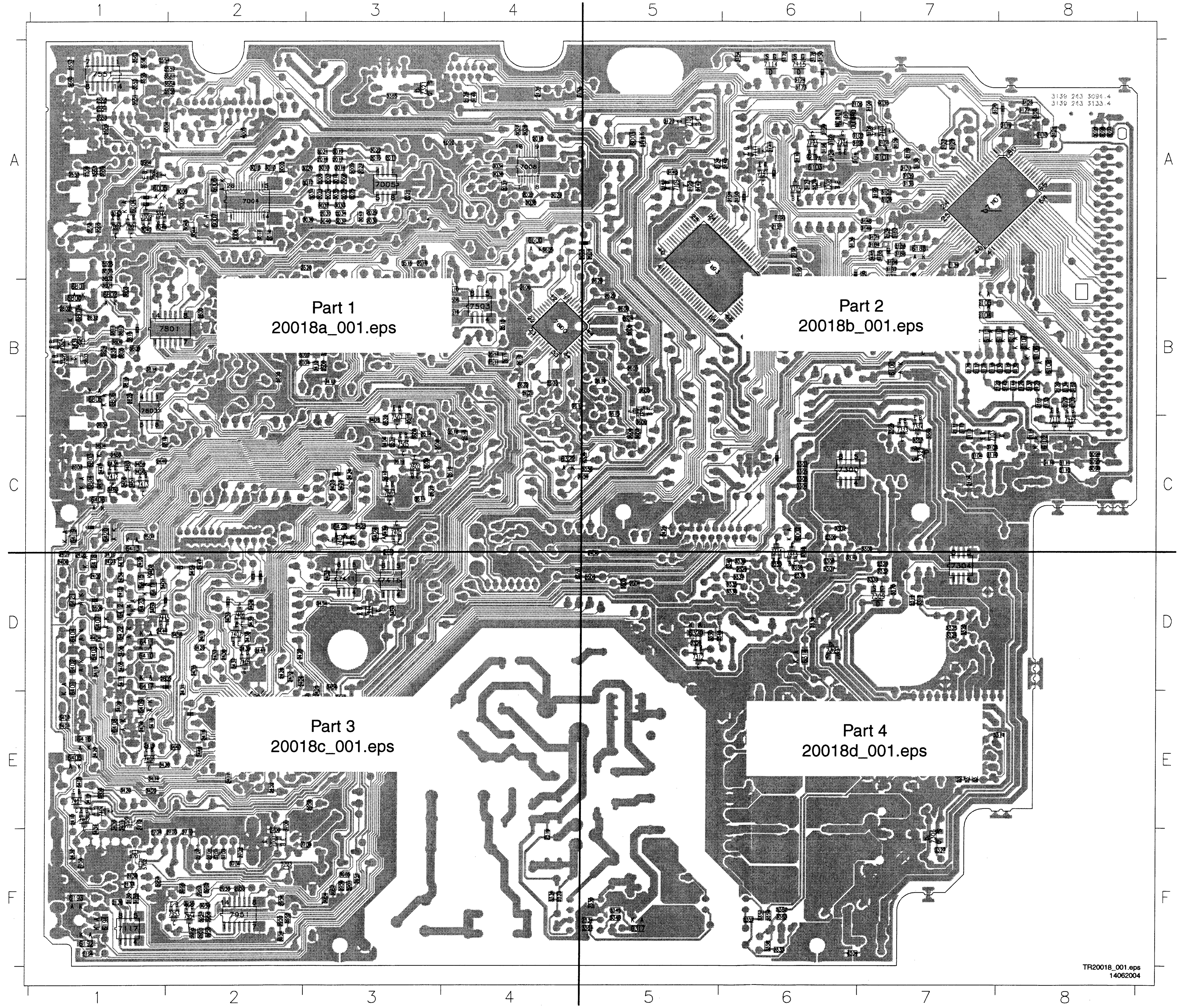
Layout: MOBO - Main Part (Top View)



TR20017_001.eps
14062004

0005	A4	3122	A4	9034	C4	9280	E8
0006	A8	3131	A1	9036	B3	9281	E8
0007	A4	3143	A2	9037	B3	9282	E6
0803	A4	3153	A5	9038	B3	9283	E7
1100	A1	3156	A3	9039	B3	9284	D7
1101	A2	3158	A5	9040	B2	9285	D7
1102	A2	3183	A3	9041	A2	9286	E6
1191	A3	3191	A3	9042	A3	9287	E7
1300	C3	3192	A3	9043	B3	9288	B5
1301	E1	3300	D5	9044	A3	9289	B5
1302	F5	3301	D4	9045	A3	9290	E7
1303	F5	3312	E2	9046	A3	9291	C4
1304	F2	3316	E5	9050	F6	9293	A4
1305	F6	3318	E5	9052	A5	9294	A4
1306	C2	3319	D2	9053	A3	9295	B5
1308	E3	3321	D4	9054	A3	9296	A4
1310	D4	3322	E4	9058	A2	9297	B5
1600	B5	3323	E4	9059	A2	9298	B6
1700	F7	3326	C2	9060	C1	9299	B5
1900	A7	3329	F5	9061	A2	9300	D2
1911	D5	3330	F5	9062	B2	9302	B6
1913	A7	3331	F5	9064	B2	9303	B6
1915	A5	3341	F4	9065	A3	9305	B6
1916	F8	3342	F4	9066	A3	9306	B6
1917	C3	3343	F4	9068	C4	9307	B6
1931	F5	3344	D3	9069	B4	9308	B6
1932	D2	3347	D4	9070	B4	9309	A5
1934	A6	3366	C2	9074	D4	9311	A5
1940	D8	3416	E8	9075	D4	9312	A5
1942	C4	3426	D7	9076	D4	9313	A5
1944	B8	3427	D7	9077	D4	9314	A4
1945	B8	3435	D7	9078	D4	9315	B5
1947	C7	3442	E6	9079	D5	9318	A7
1948	C8	3443	C4	9080	C5	9319	A6
1951	A8	3444	D7	9081	C5	9320	A7
1955	A8	3447	D7	9082	C5	9322	A7
2002	A7	3449	E7	9083	B4	9323	A7
2010	A8	3455	E7	9086	A3	9324	A7
2012	A7	3461	E6	9089	A3	9325	A6
2013	A7	3462	E6	9090	C5	9326	A7
2019	A5	3507	B6	9091	B4	9327	A6
2022	A6	3517	B5	9093	F6	9330	A5
2028	B7	3604	A4	9094	A7	9331	A5
2032	A5	3606	A4	9095	A7	9332	A5
2102	B2	3610	B4	9104	C1	9333	A4
2103	B2	3613	C4	9105	D5	9334	A6
2105	C2	4816	E7	9106	D5	9335	A6
2107	C1	5101	C1	9115	A4	9336	A6
2109	A2	5191	A3	9116	B3	9337	A6
2112	C1	5300	F3	9117	C3	9338	A6
2116	A6	5301	F3	9119	D8	9339	A7
2140	C1	5302	E6	9122	B4	9340	C4
2192	A3	5303	E2	9123	C4	9341	E6
2301	D4	5304	E2	9124	B4	9342	A4
2302	E3	5305	F4	9154	A8	9343	B5
2303	E2	5306	D3	9155	A7	9344	B6
2305	F6	5307	D3	9156	A8	9346	D3
2306	E5	5401	D6	9157	A8	9347	D2
2307	E2	5402	E7	9158	A4	9348	E6
2308	D5	5551	A8	9159	C5	9349	F7
2309	F3	5600	A5	9162	B5	9350	F8
2310	F2	5601	B4	9170	A6	9351	B2
2311	F5	5700	E6	9171	A3	9354	C3
2313	E4	5704	F6	9172	B3	9355	C3
2314	D2	5800	B7	9173	A6	9356	A2
2315	E5	5801	B7	9174	C2	9357	F7
2316	E3	6255	A8	9175	E2	9358	F7
2317	F2	6300	E3	9176	A7	9359	D2
2318	F4	6301	E3	9182	A5	9360	A1
2321	D3	6302	E5	9185	A8	9361	A4
2322	D3	6303	D5	9188	A4		
2324	D3	6304	F3	9191	E8		
2326	F4	6305	E5	9192	D8		
2327	E3	6306	F3	9193	C8		
2328	D3	6307	E5	9194	F8		
2331	F4	6308	E4	9195	F8		
2413	D7	6309	E3	9196	F7		
2418	E7	6310	F5	9199	E8		
2441	C5	6311	E3	9210	D7		
2442	C5	6315	D3	9211	D7		
2445	D7	6316	C3	9212	D7		
2500	A6	6318	D3	9213	C5		
2501	A5	6319	F4	9215	D6		
2512	C6	6321	C5	9216	D7		
2518	C6	7102	C2	9217	D7		
2600	B4	7104	C2	9218	C7		
2602	B5	7106	A4	9219	D7		
2604	B5	7301	C3	9220	D7		
2605	A5	7302	E2	9225	C7		
2607	B5	7303	E2	9226	C7		
2612	B5	7305	D2	9228	D6		
2614	C4	7307	F4	9230	C6		
2615	C5	7310	D4	9231	C6		
2616	C5	7311	F4	9232	C6		
2617	B5	7316	F4	9233	C7		
2618	C6	7318	C5	9237	C7		
2620	C4	7319	F3	9238	C7		
2702	E6	9000	A5	9239	C7		
2706	F6	9001	F4	9240	C7		
2711	F8	9002	F8	9241	C7		
2801	E8	9003	E3	9242	C8		
2808	B7	9004	F3	9244	C5		
2809	A7	9005	D4	9245	C4		
2812	B7	9006	F2	9246	A3		
2813	B8	9007	E2	9247	C4		
2816	B7	9008	D1	9248	B8		
2817	A8	9009	E2	9250	A3		
2821	B7	9010	C2	9251	B4		
2822	A6	9011	E2	9252	A3		
2826	B7	9013	D2	9253	A4		
2827	B8	9015	D2	9254	A3		
2828	A6	9016	C2	9256	B3		
2829	B8	9017	C2	9260	C7		
2830	B7	9018	B1	9262	B4		
2833	C8	9019	B2	9263	C5		
2834	B7	9020	B2	9264	D6		
2835	C8	9021	B2	9265	B8		
2952	F7	9022	B1	9266	B8		
3004	A7	9023	B1	9267	B7		
3018	A7	9024	B1	9268	C6		
3019	A7	9025	B1	9269	C5		
3023	A7	9026	B1	9270	C5		
3024	A7	9027	B1	9271	B6		
3025	A5	9028	B1	9272	C6		
3026	A5	9030	B3	9273	B6		
3030	A7	9031	C3	9274	C7		
3103	B3	9032	B3	9275	B6		
3115	A3	9033	C3	9276	B6		

Layout: MOBO - Main Part (Bottom View)



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2003	A2	2510	B4	3133	A7	3421	C3	4408	D1	7312	D5
2004	B2	2511	B4	3134	B8	3422	E1	4409	D2	7313	D6
2005	A1	2513	B3	3135	A7	3423	C3	4410	D2	7314	C6
2006	A3	2514	C3	3136	A6	3424	C3	4411	D2	7321	A3
2007	A3	2515	B4	3137	B8	3425	D2	4412	D2	7322	C7
2008	A3	2516	A3	3138	A7	3428	D2	4413	B7	7323	C7
2009	A3	2517	B3	3139	A7	3429	E1	4414	A8	7324	C7
2011	A3	2519	C4	3140	A6	3430	E1	4415	B1	7325	D6
2014	A2	2520	A3	3141	A5	3431	F1	4416	A6	7401	E1
2015	A3	2521	B3	3142	B8	3432	F1	4418	B3	7402	E1
2016	A3	2551	A1	3144	B8	3433	D2	4422	B3	7403	C3
2017	A3	2552	A1	3145	A5	3434	D2	4807	B2	7404	E1
2018	A4	2553	A1	3146	A4	3436	E1	4808	B2	7405	C3
2020	A4	2554	A1	3147	A5	3437	D2	4809	A5	7406	D2
2021	A3	2555	A1	3148	A7	3438	D2	4810	C6	7407	D2
2023	A3	2556	A1	3149	A7	3439	D2	4811	A7	7408	E1
2024	A3	2557	A1	3150	A6	3440	E2	4812	A6	7409	D2
2025	A3	2558	A1	3151	B7	3441	D2	4813	A6	7410	E2
2026	A3	2601	B5	3152	B7	3445	A7	4814	A6	7411	D3
2027	A3	2603	B4	3154	A6	3446	E2	4815	A1	7412	C1
2029	A3	2606	B4	3155	B7	3448	E3	5100	B7	7413	C1
2030	A3	2608	B5	3157	A7	3450	C1	5701	F1	7414	D3
2031	A4	2609	B5	3159	A7	3451	C1	5702	F1	7415	D1
2033	A3	2610	B4	3160	B7	3452	E2	5703	F2	7416	D3
2034	A3	2611	B4	3161	B8	3453	D1	5706	E1	7500	B2
2100	A7	2613	B4	3162	B8	3454	D3	5802	B1	7501	B3
2101	A7	2619	C4	3163	A7	3456	D3	5803	B1	7503	B4
2104	C7	2621	B4	3164	A7	3457	D3	6002	C6	7504	B3
2106	A6	2622	B4	3165	A7	3458	D2	6003	A5	7505	C3
2108	B7	2623	C3	3166	A7	3459	C1	6004	A1	7507	C3
2110	A6	2624	B5	3167	B7	3460	C1	6005	A1	7551	A1
2111	C7	2625	B5	3168	B7	3463	C1	6006	A2	7600	B4
2113	A8	2626	B5	3169	B7	3464	D2	6007	A2	7601	B5
2114	C8	2700	F2	3170	A7	3465	C1	6100	B7	7602	C3
2115	A6	2701	F2	3171	A7	3466	C1	6101	A7	7603	C3
2117	B7	2703	F2	3172	A6	3500	B3	6102	C8	7801	B2
2118	B7	2704	F1	3173	A6	3501	B3	6103	A6	7802	B1
2119	B8	2705	F1	3174	A6	3502	D4	6104	B7	7803	B1
2120	B8	2707	F2	3175	B8	3503	D5	6105	B7	7804	B1
2121	B8	2709	F3	3176	B7	3504	B3	6106	B8	7951	F2
2122	B7	2710	F2	3177	B7	3505	B3	6107	B8	7953	F2
2123	A5	2712	E1	3178	A6	3506	B4	6108	B8	7954	F2
2124	A5	2800	B2	3179	B7	3508	C3	6109	B8	9035	A7
2126	B8	2802	C1	3180	F1	3509	C3	6110	B8	9234	C3
2127	A7	2803	B1	3181	B7	3510	B3	6111	B7	9235	D1
2128	A4	2804	C1	3182	F1	3511	B3	6112	B7	9236	D1
2129	A7	2805	D1	3184	B7	3512	B3	6113	B7		
2130	A4	2806	D1	3185	B7	3513	B3	6114	B7		
2131	A4	2820	B2	3186	B7	3514	B4	6188	A7		
2132	B7	2823	B1	3187	A7	3515	A3	6192	F1		
2133	B8	2824	B1	3188	A7	3516	B4	6193	F1		
2134	A7	2825	B1	3189	B7	3518	C4	6194	F1		
2135	B8	2831	B1	3190	A7	3519	C3	6312	E6		
2136	F1	2832	B1	3193	A6	3521	C3	6313	E7		
2137	F1	2951	F2	3194	A6	3522	C3	6314	D6		
2138	F1	2953	F2	3195	A7	3551	A1	6317	F5		
2139	A7	2954	F2	3196	A6	3552	A1	6320	D5		
2141	A6	2955	F2	3197	A6	3553	A1	6322	C4		
2188	A7	2956	F3	3198	A6	3554	A2	6401	D1		
2189	A7	2957	F1	3199	A6	3555	A1	6402	D1		
2191	A6	2958	E3	3302	C6	3556	A2	6403	D1		
2193	A6	3002	B2	3303	C6	3557	A2	6404	D1		
2194	F1	3003	B2	3304	C6	3558	A1	6405	E1		
2195	A6	3005	A1	3305	C6	3559	A1	6406	C1		
2196	A6	3008	A2	3306	C6	3560	A1	6407	D1		
2300	C6	3009	A2	3307	D6	3561	A2	6408	E1		
2304	E7	3010	A2	3308	D6	3562	A1	6409	E1		
2312	D7	3011	A2	3309	C7	3563	A1	6410	D1		
2319	F4	3012	A3	3310	D6	3564	A1	6411	D1		
2320	D7	3013	A3	3311	E8	3565	A1	6412	D1		
2323	F4	3014	A3	3313	E7	3600	C5	6413	C1		
2325	D6	3015	A2	3314	E7	3601	A5	6414	D1		
2329	D5	3016	A3	3315	E7	3602	A4	6415	D1		
2330	F5	3017	A3	3317	D7	3603	B5	6416	E1		
2333	F6	3020	A3	3320	D7	3605	A4	6417	D1		
2334	F5	3021	A3	3324	D7	3607	C5	6418	D1		
2335	D6	3022	A3	3325	D7	3608	C5	6419	C1		
2336	C5	3027	A4	3327	F7	3609	C3	6420	C1		
2401	E1	3028	A4	3328	A6	3611	C3	6421	D1		
2402	D1	3029	A4	3332	D7	3614	C3	6422	D1		
2403	D1	3031	A3	3333	D7	3615	B5	6423	D1		
2404	D1	3032	A3	3334	F4	3616	B5	6424	C3		
2405	D1	3033	A3	3335	D6	3617	C3	6425	C3		
2406	D1	3034	A4	3336	D6	3700	E2	6600	A4		
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2415	D2	3042	A1	3349	D5	3803	B1	6807	B1		
2416	E2	3043	A1	3350	D5	3804	C1	7000	F2		
2417	E2	3044	A2	3351	F6	3805	B1	7001	A1		
2419	E1	3045	A2	3353	D6	3807	C1	7002	A1		
2420	D2	3046	A1	3354	C5	3808	B1	7004	A2		
2421	C5	3094	C8	3355	D6	3809	B1	7005	A3		
2422	C3	3095	C8	3356	C5	3810	B1	7006	A1		
2423	C3	3096	C8	3357	F6	3811	B1	7008	A4		
2424	C3	3097	A8	3358	F6	3813	B1	7009	A1		
2425	E3	3098	A8	3359	F6	3814	B1	7045	A1		
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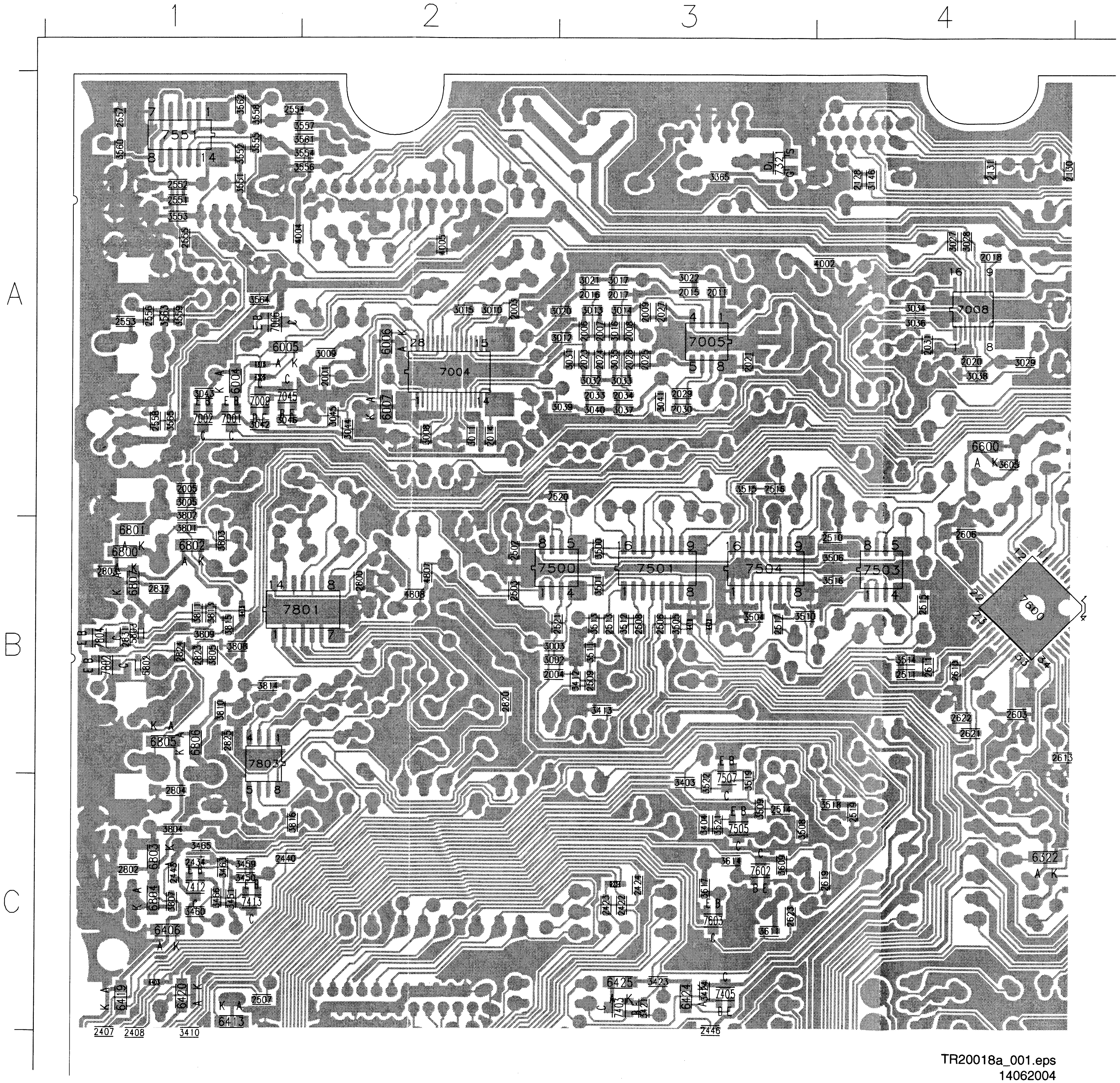
2427	E3	3101	A7	3362	F6	3816	C1	7101	A7		
2428	D2	3102	A6	3363	F6	3951	F3	7103	C7		
2429	E3	3104	C7	3365	A3	3952	F2	7105	A6		
2430	E3	3105	A7	3367	C7	3953	F2	7107	A7		
2431	D2	3106	A7	3368	C7	3954	F2	7108	A5		
2432	D3	3108	C7	3369	C7	3955	F2	7109	A5		
2433	E3	3109	A7	3370	D7	3956	F2	7110	C8		
2434	C1	3110	C7	3401	D1	3957	F2	7111	A6		
2435	D2	3111	C8	3402	D1	3958	F2	7112	C8		
2436	D5	3112	C7	3403	C3	3959	F2	7113	B7		
2437	D2	3113	C8	3404	C3	3960	F2	7114	A6		
2438	D2	3114	A6	3405	D1	3961	F3	7115	A6		
2439	E1	3116	C8	3406	D1	3962	F2	7116	B7		
2440	C1	3117	C7	3407	E1	3963	F2	7117	F1		
2443	C1	3118	A5	3408	E1	3964	F3	7118	B7		
2444	D1	3119	A8	3409	E1	3965	F3	7121	B7		
2446	C3	3120	A6	3410	D1	3966	F2	7122	B7		
2447	D2	3121	A6	3411	D1	3967	F3	7123	A6		
2502	B2	3123	A5	3412	B3	4002	A4	7124	A6		
2503	B2	3124	A8	3413	B3	4004	A1	7191	A6		
2504	D5	3125	A8	3414	E1	4005	A2	7193	A5		
2505	D5	3126	A8	3415	D1	4304	F6	7300	C6		
2506	B3	3127	A8	3417	D1	4305	A1	7304	D7		
2507	C1	3128	B7	3418	E1	4401	D1	7306	F7		
2508	B3	3130	B8	3419	E1	4403	C1	7308	A6		

Layout: MOBO - Main Part (Bottom View) Part 1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A
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C
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7500
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7801
7803
7321
7507
7505
7602
7603
7412
7413
7403
7405
6600
6322
6801
6800
6802
6805
6806
6005
6004
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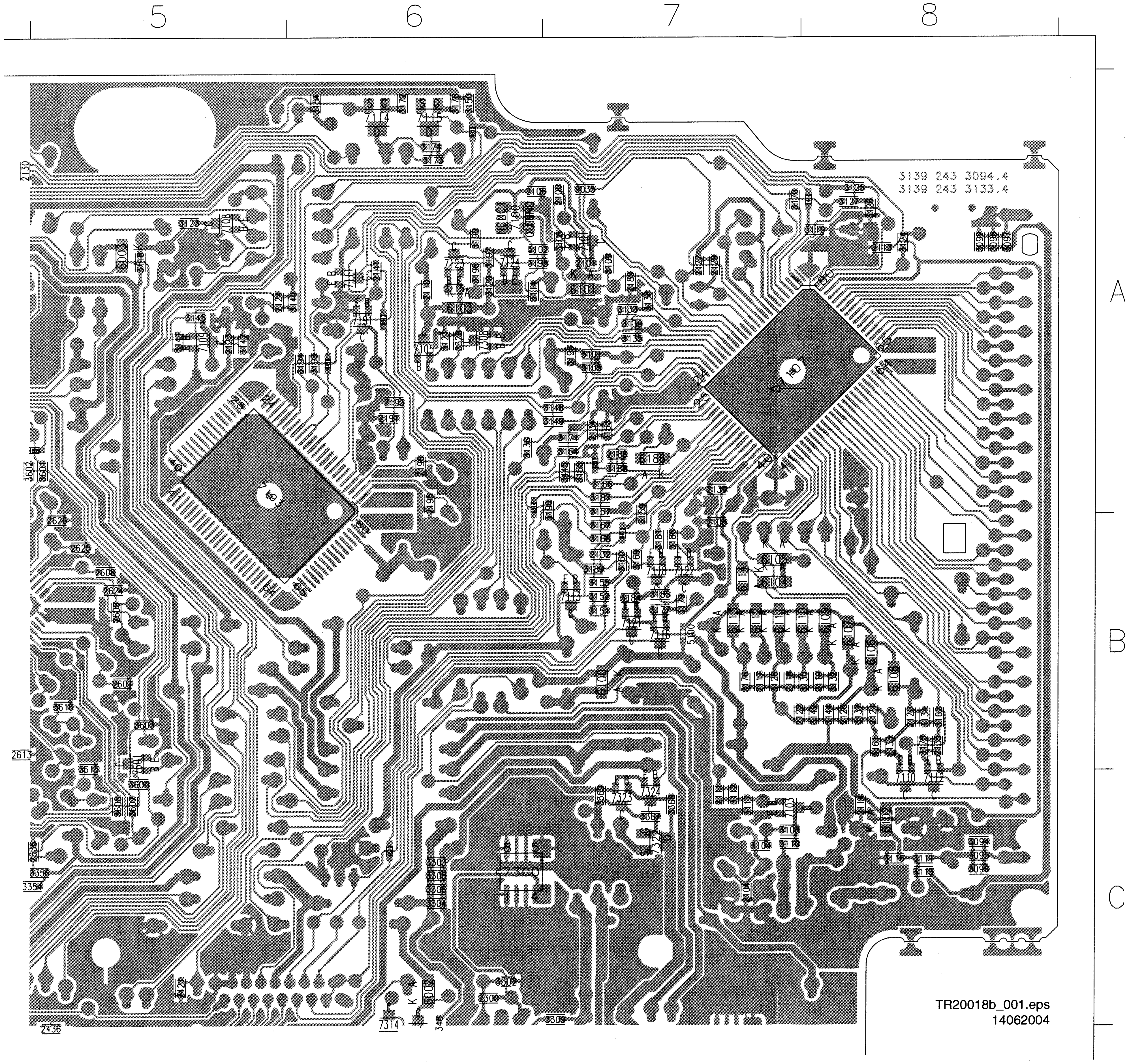
6425
6424

TR20018a_001.eps
14062004

Layout: MOBO - Main Part (Bottom View) Part 2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C
3139 243 3094.4
3139 243 3133.4
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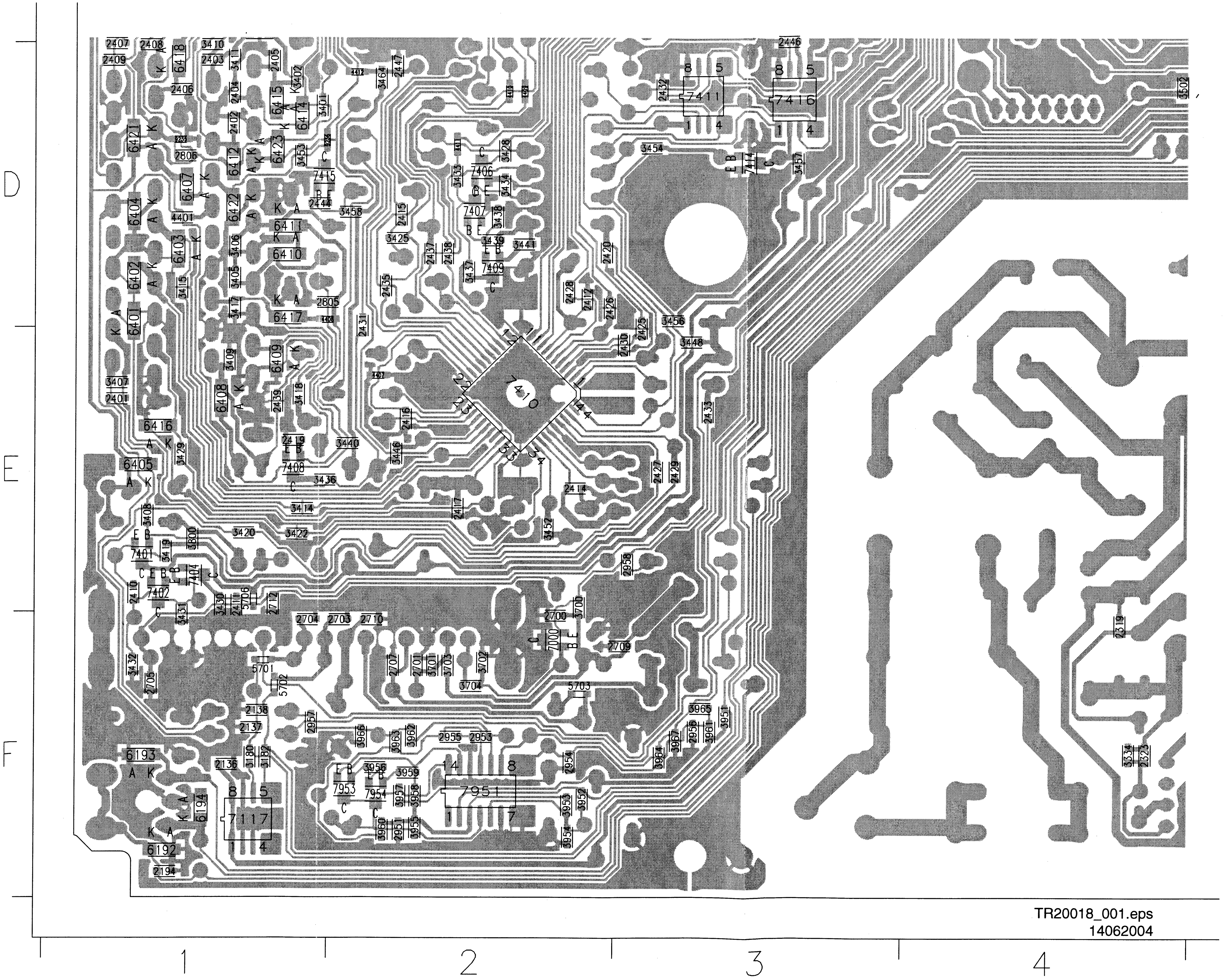
7115
7108
7109
7111
7191
7123
7124
7100
7101
7105
7120
6003
6101
6103
6104
6105
6106
6107
6108
6109
6100
6102
6002
6188
7110
7112
7113
7116
7118
7122
7300
7314
7323
7324
7601
2130
2436
2613
3354
3602
3601
2626
2625
2608
2624
2609
2601
3616
3603
3615
3600
9035

TR20018b_001.eps
14062004

Layout: MOBO - Main Part (Bottom View) Part 3


D
E
F
1
2
3
4
2407
2408
2409
3410
2403
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2406
3411
2405
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3464
2447
7411
7416
2446
3502
6421
2808
6412
6422
6407
6404
4401
6403
6402
6401
6415
6414
6423
3401
3453
7415
2444
3458
6411
6410
6417
2805
6409
6408
3409
3418
2439
7410
3406
3405
3415
3417
3425
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2437
2438
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3437
7406
7407
7409
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3439
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2420
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2412
2426
2425
2430
3456
3448
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3457
7414
2433
3407
2401
6416
3429
6405
3440
2419
7408
3436
3446
2416
2417
3414
2414
2427
2429
3452
3408
7401
3419
3800
3420
3422
7402
7404
2410
3431
3430
2411
5706
2712
2704
2703
2710
2700
3700
7000
2709
2958
3432
2705
5701
5702
2707
2701
3701
3703
3702
3704
5703
3965
3951
2138
2137
2957
3966
3963
3962
2955
2953
3964
3967
2956
3961
6193
2136
3180
3182
7953
3956
7954
3959
7951
2954
3957
3958
7117
6194
6192
2194
3960
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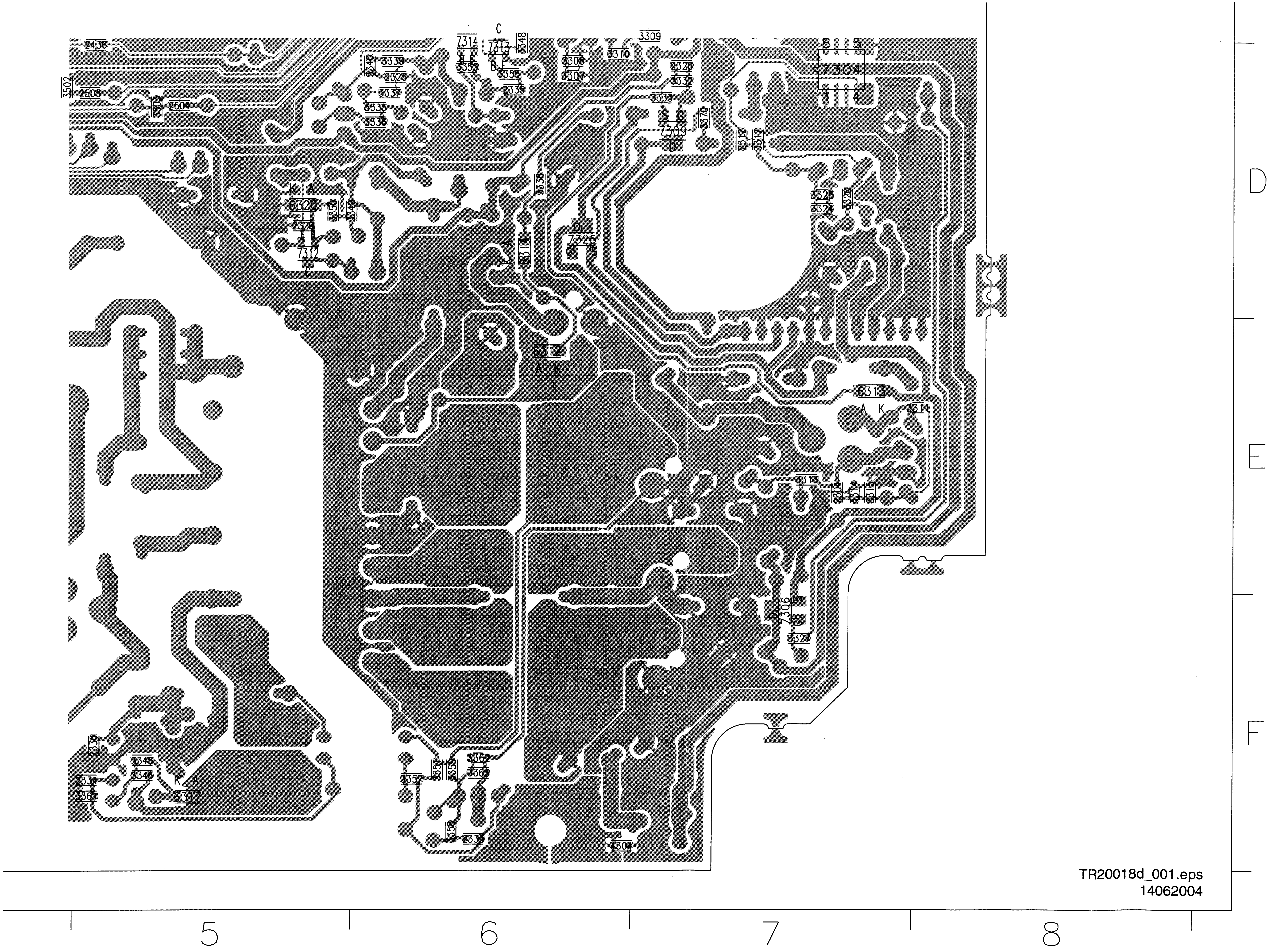
3334
2323

TR20018_001.eps
14062004

Layout: MOBO - Main Part (Bottom View) Part 4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3502
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3503
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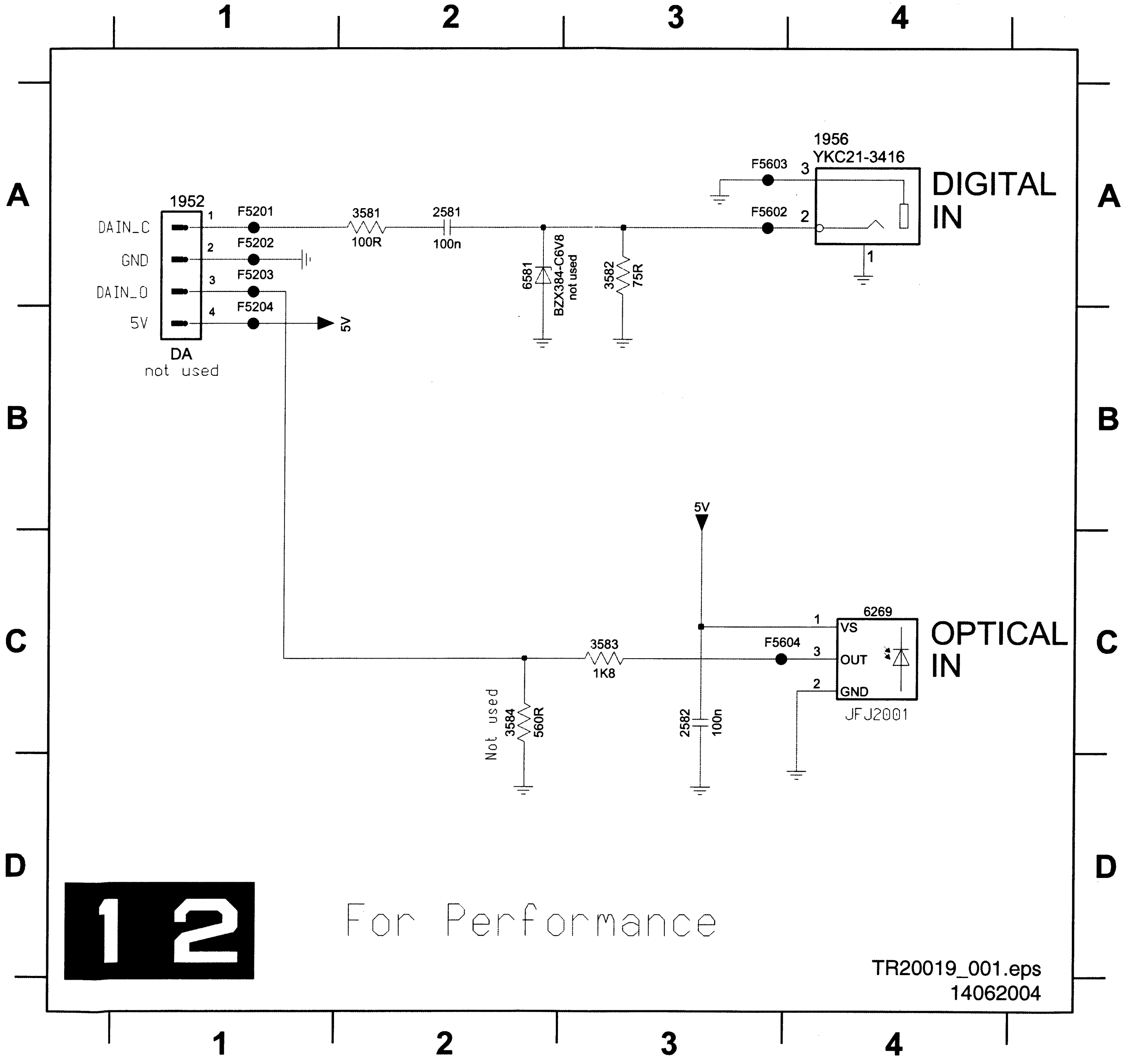
2325
3337
3335
3336
7314
C
7313
3348
B E
3353
B E
3355
2335
3309
3308
3307
3310
2320
3332
3333
S G
7309
D
3370
8 5
7304
1 4
2312
3317
3338
K A
6320
3350
3349
2329
7312
C
K A
6314
D
7325
G S
3325
3324
3320
6312
A K
6313
A K
3311
3313
2304
6314
3315
D
7306
S
G
3327
2330
3345
3346
2334
3361
K A
6317
3357
3351
3359
3362
3363
3358
2333
4304
D
E
F
5
6
7
8

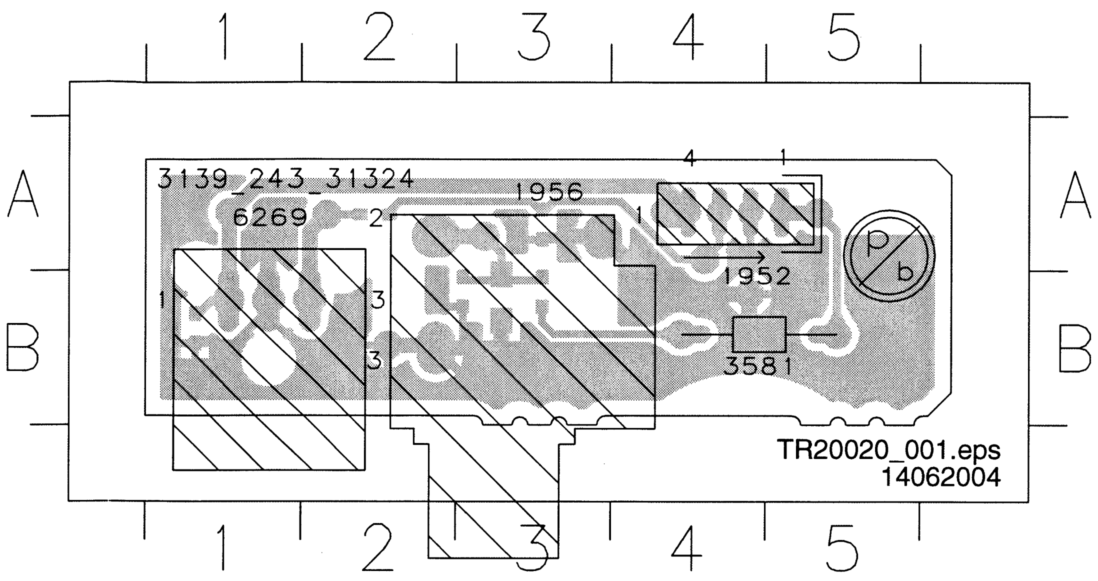
TR20018d_001.eps
14062004

MOBO : Digital In/Out 2 (DIGIO 2)

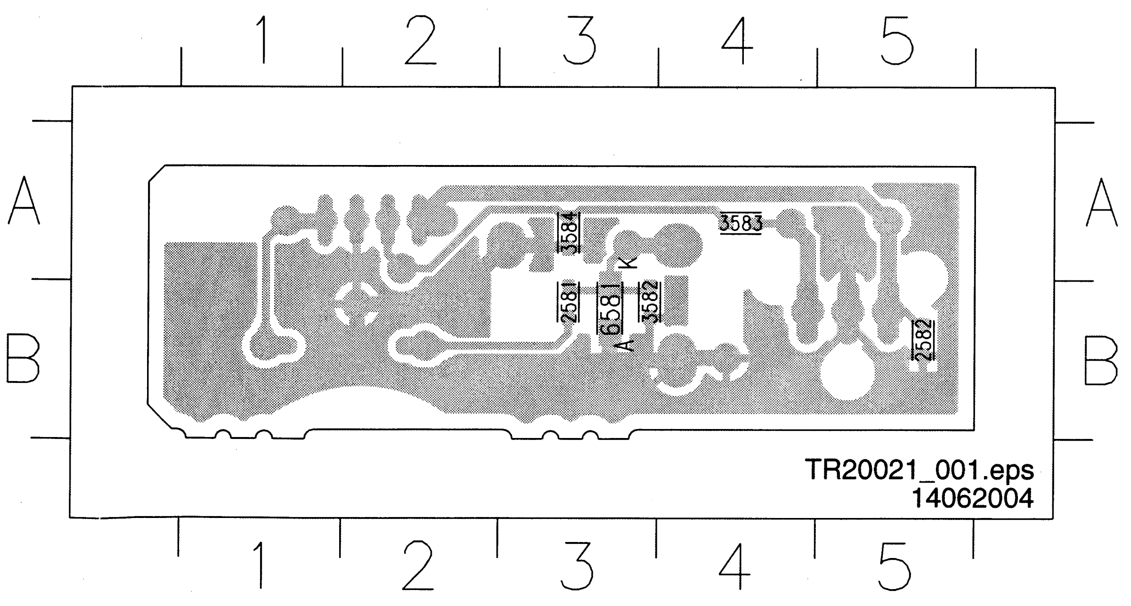
1952 A1	2581 A2	3581 A2	3583 C3	6269 C4	F5201 A1	F5203 A1	F5602 A3	F5604 C3
1956 A4	2582 C3	3582 A3	3584 C2	6581 A2	F5202 A1	F5204 B1	F5603 A3	


1
2
3
4
A
B
C
D
1952
DAIN_C
GND
DAIN_O
5V
DA
not used
F5201
F5202
F5203
F5204
3581
100R
2581
100n
6581
BZX384-C6V8
not used
3582
75R
5V
1956
YKC21-3416
F5603
F5602
DIGITAL
IN
5V
6269
VS
OUT
GND
JFJ2001
OPTICAL
IN
F5604
3583
1K8
Not used
3584
560R
2582
100n
12
For Performance
TR20019_001.eps
14062004

Layout: MOBO - Digital In/Out 2 Part

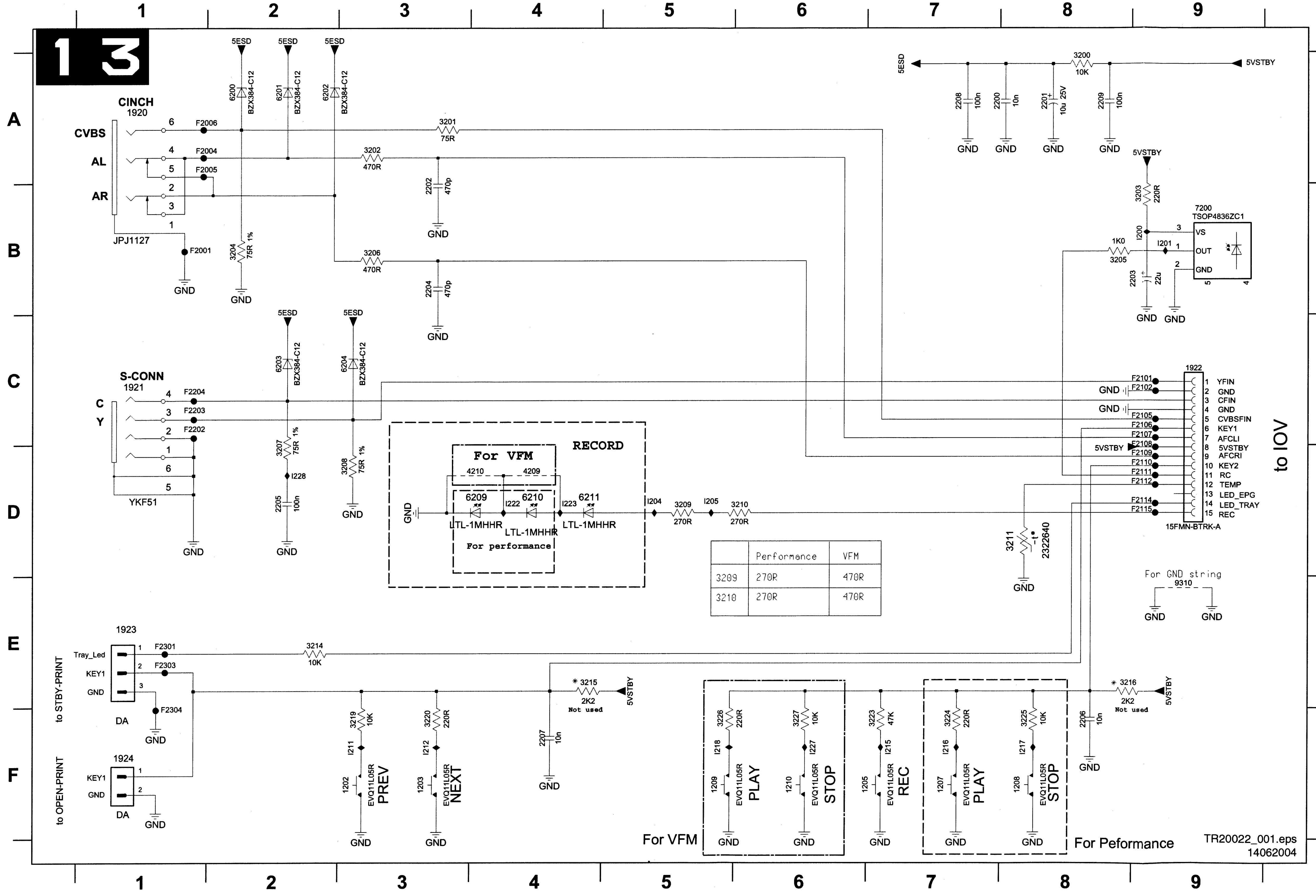

1
2
3
4
5
A
B
3139_243_31324
6269
1956
1952
3581
TR20020_001.eps
14062004

1952	B4
1956	A3
3581	B4
6269	A1


1
2
3
4
5
A
B
3584
3583
2581
6581
3582
K
A
2582
TR20021_001.eps
14062004

2581	B3
2582	B5
3582	B3
3583	A4
3584	A3
6581	B3

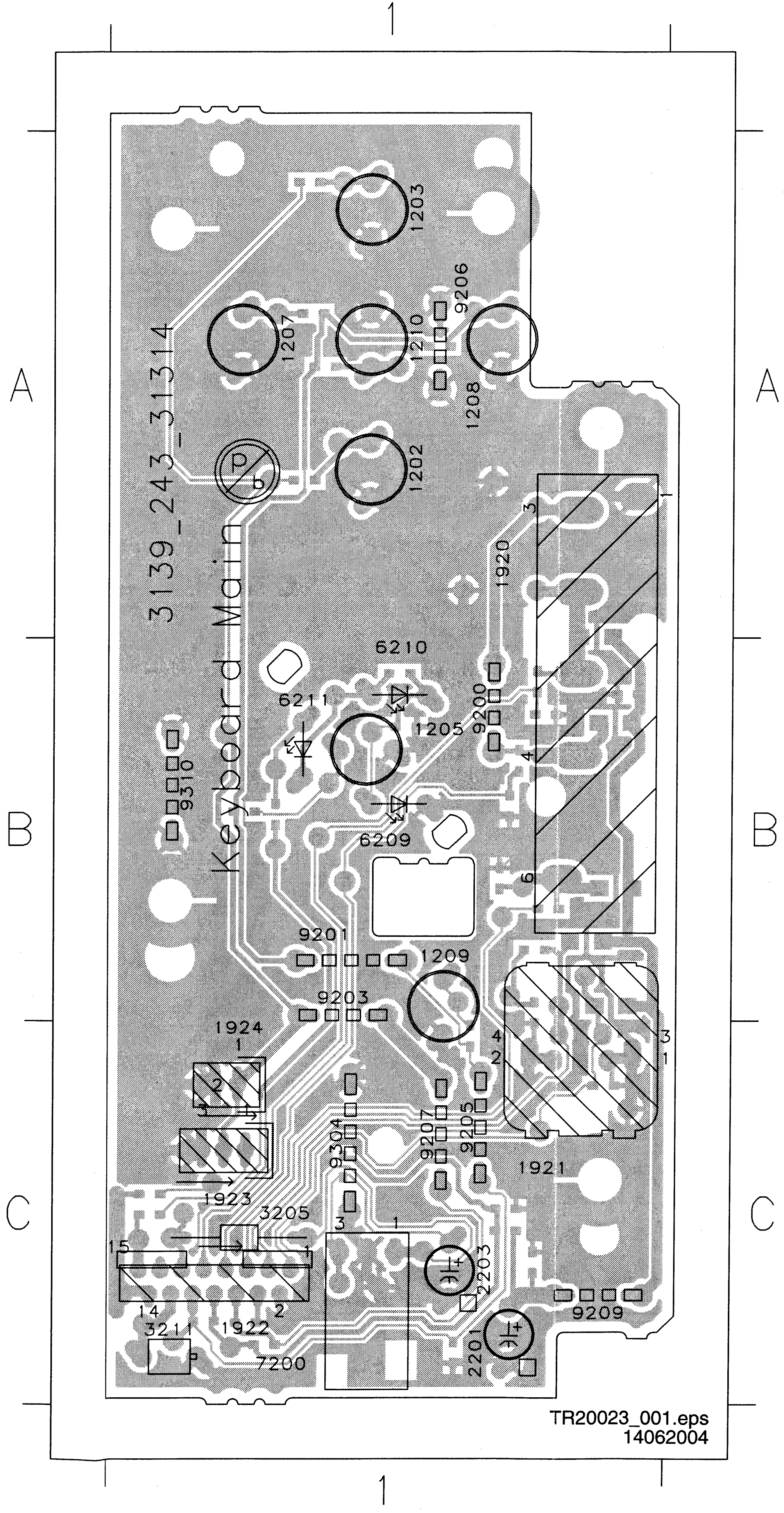
MOBO Keyboard (KEY)


13
CINCH
1920
CVBS
AL
AR
JPJ1127
F2001
F2004
F2005
F2006
5ESD
6200
6201
6202
BZX384-C12
3201
75R
3202
470R
3204
75R 1%
2202
470p
3206
470R
2204
470p
GND
S-CONN
1921
C
Y
F2204
F2203
F2202
YKF51
6203
6204
3207
75R 1%
I228
3208
75R 1%
2205
100n
RECORD
For VFM
4210
4209
6209
6210
6211
I222
I223
LTL-1MHHR
For performance
I204
I205
3209
270R
3210
270R
5ESD
3200
10K
5VSTBY
2208
100n
2200
10n
2201
10u 25V
2209
100n
3203
220R
7200
TSOP4836ZC1
VS
OUT
GND
I200
I201
1K0
3205
2203
22u
1922
YFIN
GND
CFIN
GND
CVBSFIN
KEY1
AFCLI
5VSTBY
AFCRI
KEY2
RC
TEMP
LED_EPG
LED_TRAY
REC
F2101
F2102
F2105
F2106
F2107
F2108
F2109
F2110
F2111
F2112
F2114
F2115
15FMN-BTRK-A
to IOV
3211
2322640
For GND string
9310
1923
Tray_Led
KEY1
GND
F2301
F2303
F2304
DA
to STBY-PRINT
1924
KEY1
GND
DA
to OPEN-PRINT
3214
10K
* 3215
2K2
Not used
* 3216
2K2
Not used
3219
10K
3220
220R
I211
I212
1202
1203
EVQ11L05R
PREV
NEXT
2207
10n
3226
220R
3227
10K
I218
I227
1209
1210
PLAY
STOP
3223
47K
I215
1205
REC
3224
220R
3225
10K
I216
I217
1207
1208
PLAY
STOP
2206
10n
For VFM
For Peformance
TR20022_001.eps
14062004

	Performance	VFM
3209	270R	470R
3210	270R	470R

1202	F3
1203	F3
1205	F7
1207	F7
1208	F8
1209	F5
1210	F6
1920	A1
1921	C1
1922	C9
1923	E1
1924	F1
2200	A7
2201	A8
2202	B3
2203	B9
2204	B3
2205	D2
2206	F8
2207	F4
2208	A7
2209	A8
3200	A8
3201	A3
3202	A3
3203	B9
3204	B2
3205	B8
3206	B3
3207	D2
3208	D3
3209	D5
3210	D6
3211	D8
3214	E2
3215	E4
3216	E8
3219	F3
3220	F3
3223	F7
3224	F7
3225	F8
3226	F5
3227	F6
4209	D4
4210	D4
6200	A2
6201	A2
6202	A2
6203	C2
6204	C3
6209	D4
6210	D4
6211	D4
7200	B9
9310	E9
F2001	B1
F2004	A1
F2005	A1
F2006	A1
F2101	C9
F2102	C9
F2105	C9
F2106	C9
F2107	C9
F2108	D9
F2109	D9
F2110	D9
F2111	D9
F2112	D9
F2114	D9
F2115	D9
F2202	C1
F2203	C1
F2204	C1
F2301	E1
F2303	E1
F2304	F1
I200	B9
I201	B9
I204	D5
I205	D5
I211	F3
I212	F3
I215	F7
I216	F7
I217	F8
I218	F5
I222	D4
I223	D4
I227	F6
I228	D2

Layout MOBO Keyboard (KEY)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1208
1202
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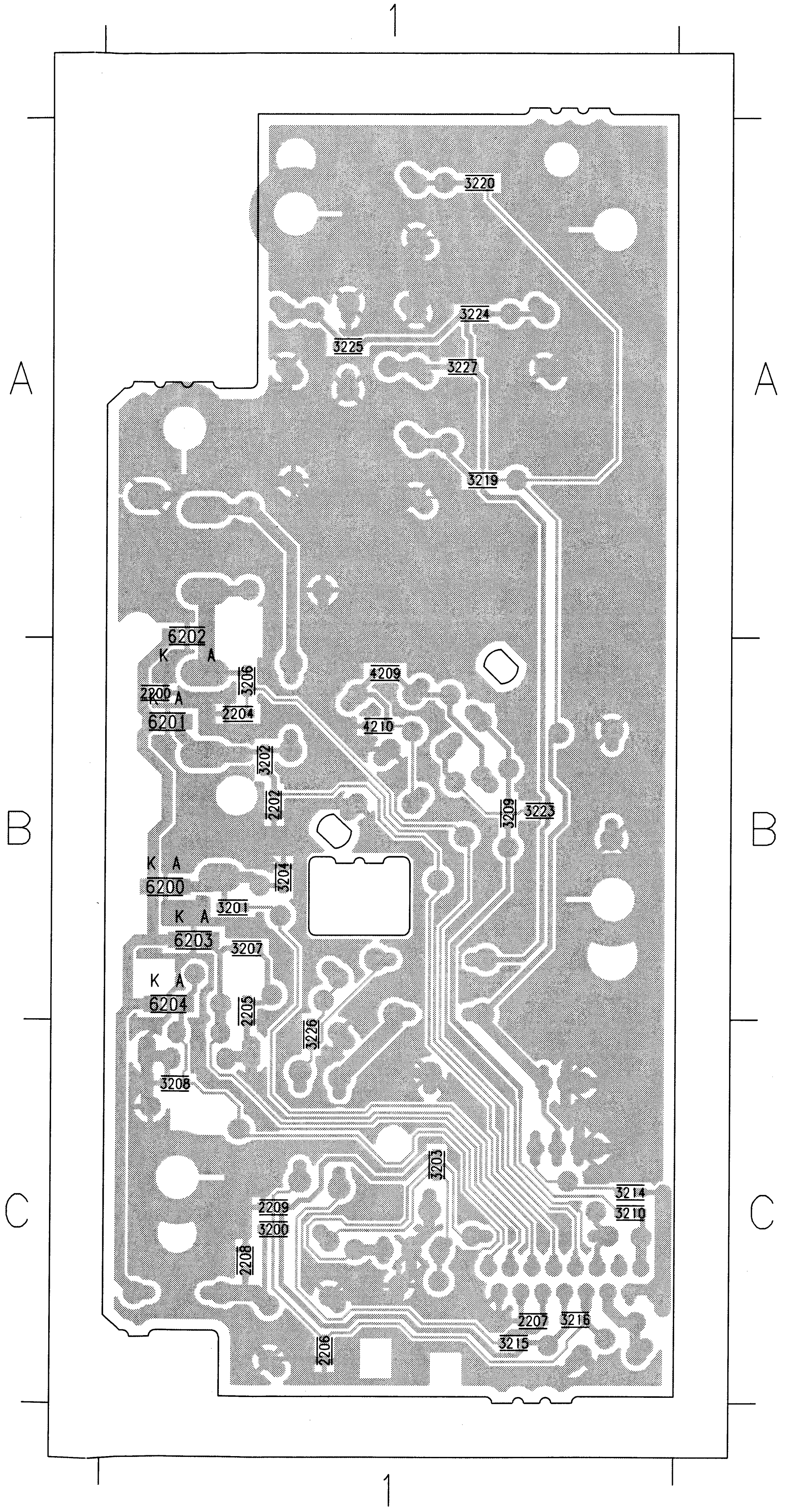
1920
6210
6211
1205
9200
9310
6209
9201
1209
9203
1924
1923
3205
9304
9207
9205
1921
2203
9209
2201
3211
1922
7200
15
14
2
3
4
6

TR20023_001.eps
14062004

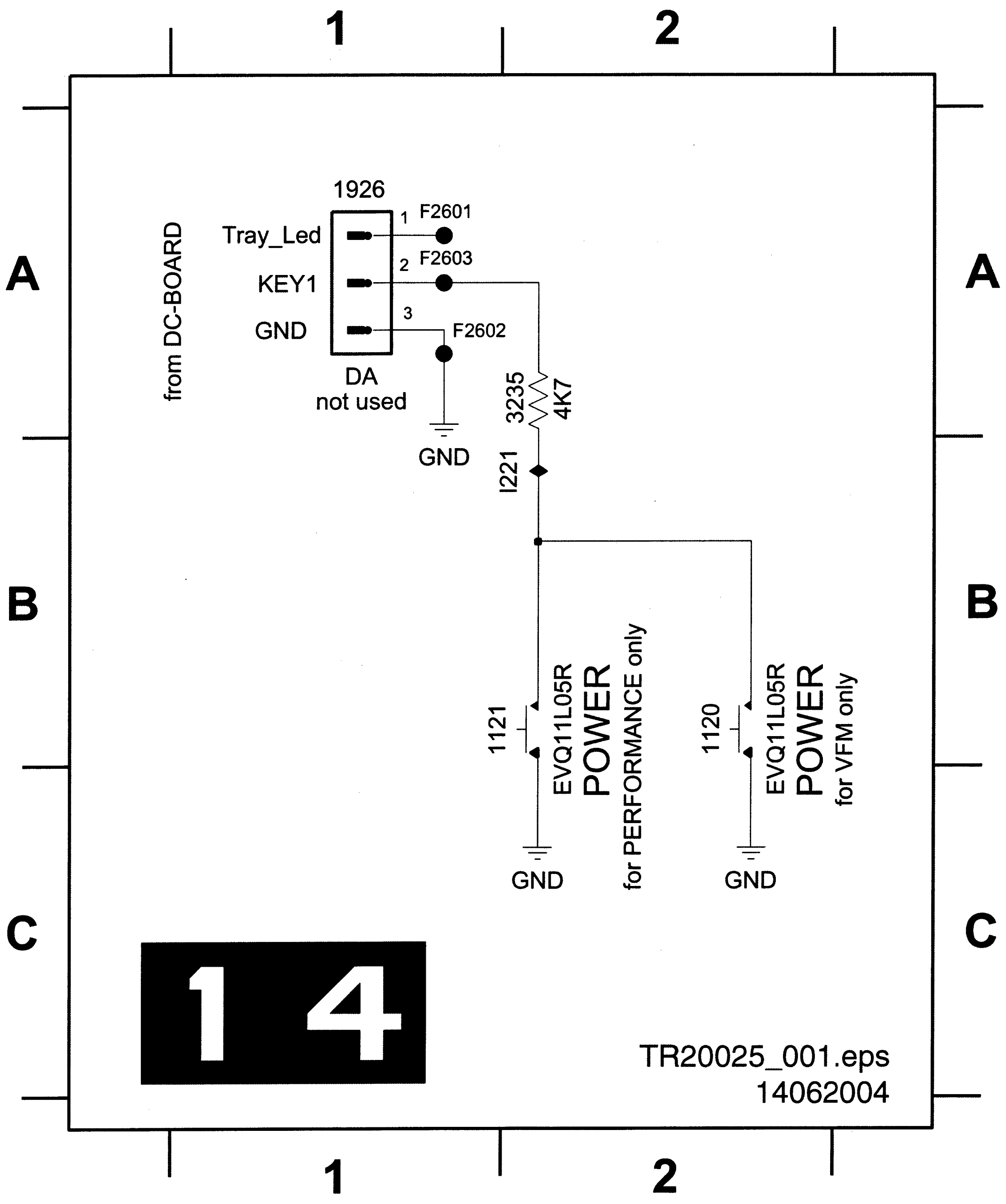
1202	A1
1203	A1
1205	B1
1207	A1
1208	A1
1209	B1
1210	A1
1920	A1
1921	C1
1922	C1
1923	C1
1924	C1
2201	C1
2203	C1
3205	C1
3211	C1
6209	B1
6210	B1
6211	B1
7200	C1
9200	B1
9201	B1
9203	B1
9205	C1
9206	A1
9207	C1
9209	C1
9304	C1
9310	B1


1
A
B
C
3220
3224
3225
3227
3219
6202
K
A
3206
2200
6201
2204
4209
4210
3202
2202
3209
3223
6200
3204
3201
6203
3207
6204
2205
3226
3208
3203
2209
3200
2208
3214
3210
2207
3216
3215
2206

TR20024_001.eps
14062004

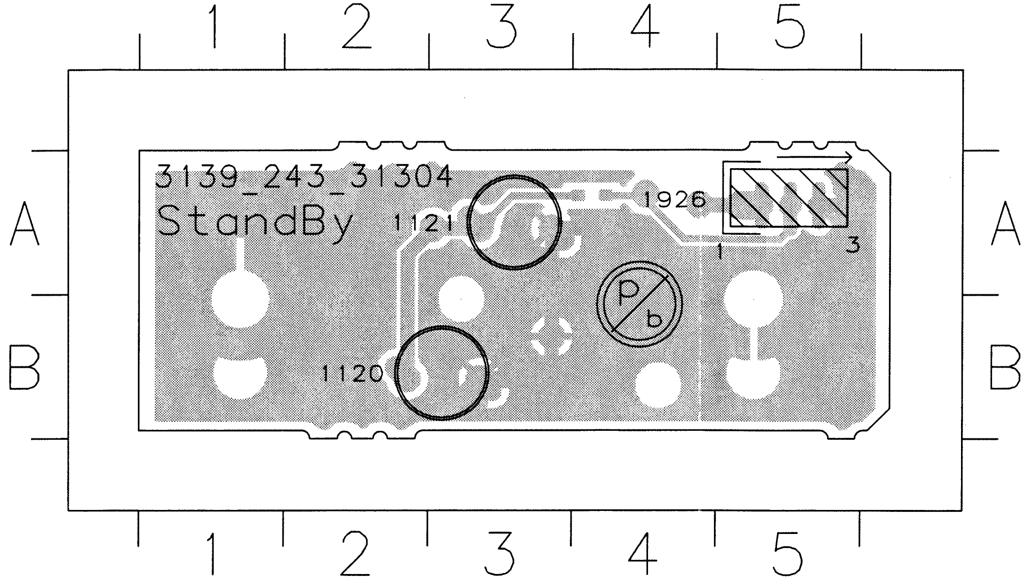
2200	B1
2202	B1
2204	B1
2205	B1
2206	C1
2207	C1
2208	C1
2209	C1
3200	C1
3201	B1
3202	B1
3203	C1
3204	B1
3206	B1
3207	B1
3208	C1
3209	B1
3210	C1
3214	C1
3215	C1
3216	C1
3219	A1
3220	A1
3223	B1
3224	A1
3225	A1
3226	C1
3227	A1
4209	B1
4210	B1
6200	B1
6201	B1
6202	A1
6203	B1
6204	B1

MOBO: Stand-by(STBY)

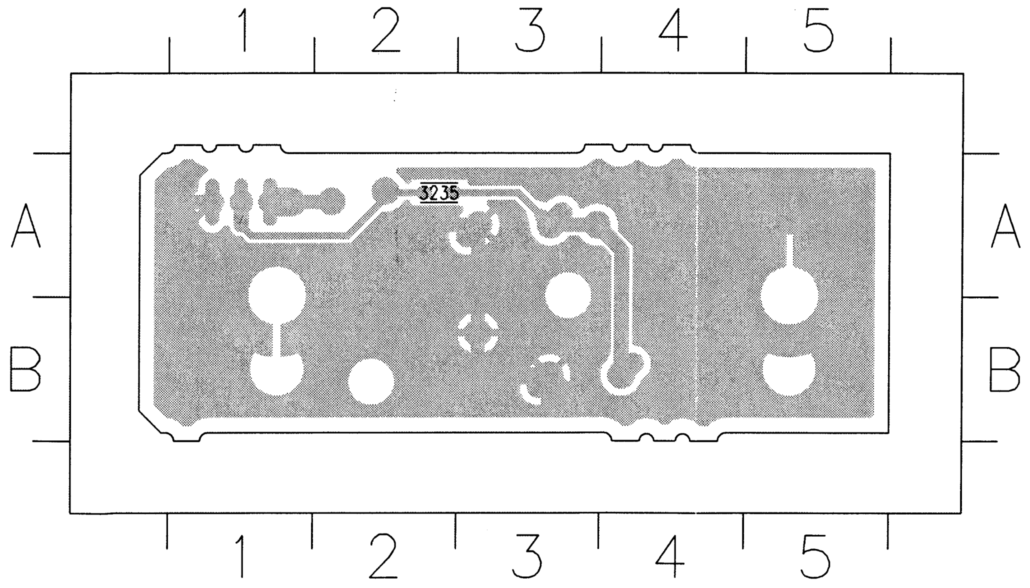

1
2
A
B
C
1926
Tray_Led
KEY1
GND
1
2
3
F2601
F2603
F2602
DA
not used
from DC-BOARD
GND
3235
4K7
I221
1121
EVQ11L05R
POWER
for PERFORMANCE only
1120
EVQ11L05R
POWER
for VFM only
GND
GND
14
TR20025_001.eps
14062004

1120	B2
1121	B2
1926	A1
3235	A2
F2601	A1
F2602	A1
F2603	A1
I221	B2

Layout: MOBO - Standby Part


1
2
3
4
5
A
B
3139_243_31304
StandBy
1121
1926
1
3
1120
P
b

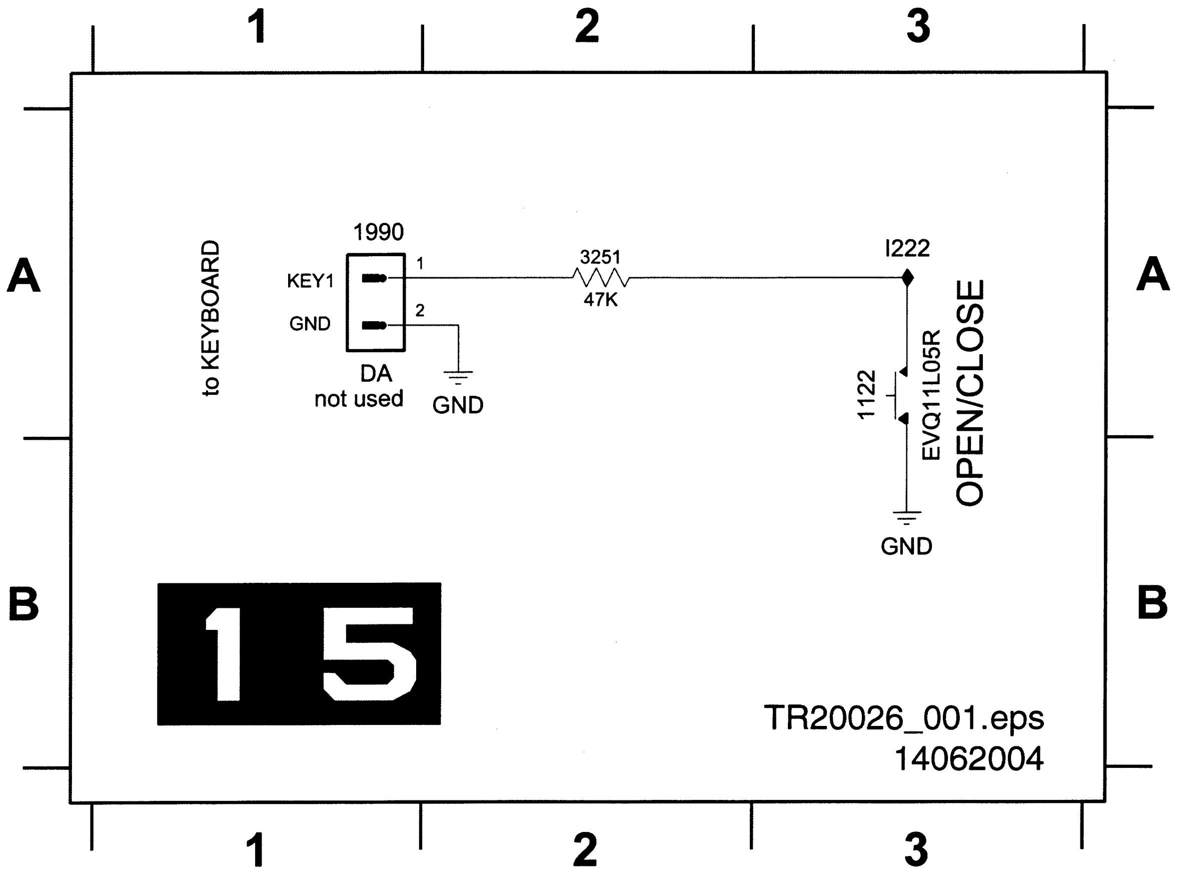
1120	B2
1121	A2
1926	A4


1
2
3
4
5
A
B
3235

3235	A2

TR20053_001.eps
30062004

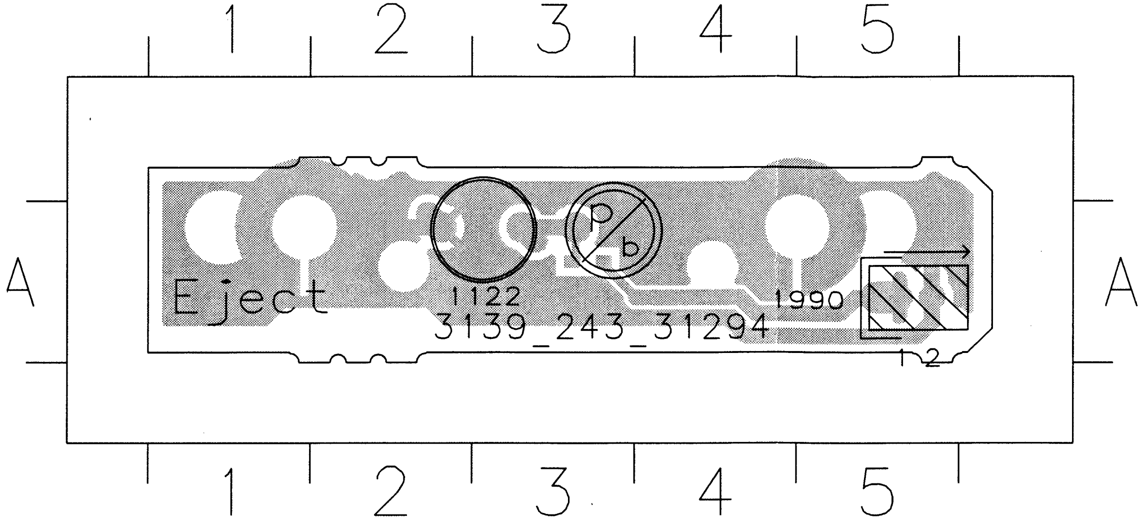
MOBO: Open/Close (OPCL)


1
2
3
A
B
to KEYBOARD
1990
KEY1
GND
1
2
DA
not used
GND
3251
47K
I222
1122
EVQ11L05R
OPEN/CLOSE
GND
15

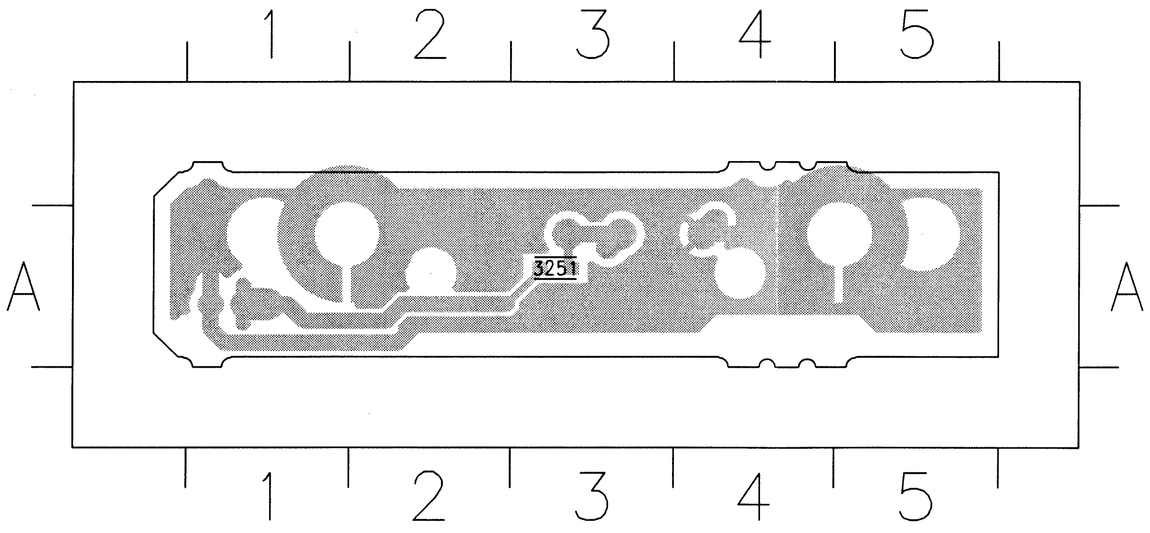
TR20026_001.eps
14062004

1122 A
1990 A
3251 A
I222 A

Layout: MOBO - Open/Close (OPCL)


1
2
3
4
5
A
Eject
1122
3139_243_31294
1990

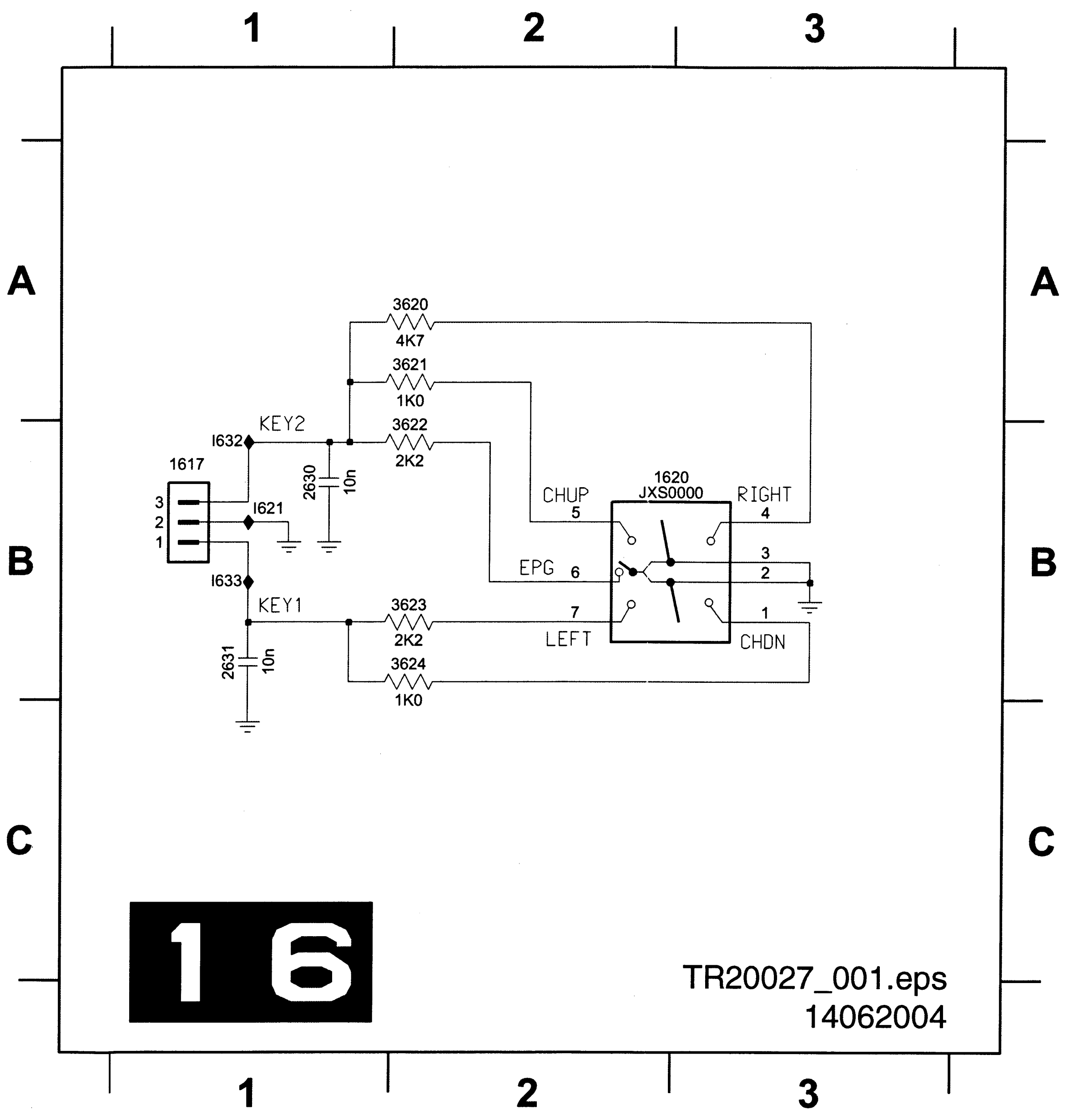
1122 A3
1990 A5


1
2
3
4
5
A
3251

3251 A3

TR20054_001.eps
30062004

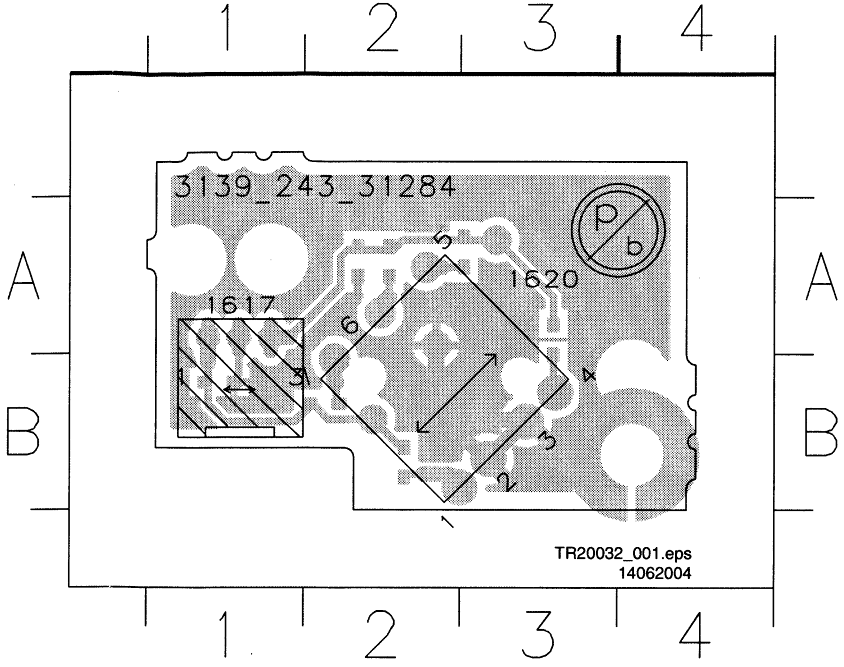
MOBO: 5-Way Switch (5WSW)


1
2
3
A
B
C
3620
4K7
3621
1K0
3622
2K2
KEY2
I632
1617
2630
10n
I621
3
2
1
1620
JXS0000
CHUP
5
RIGHT
4
EPG
6
3
2
7
LEFT
1
CHDN
I633
KEY1
3623
2K2
3624
1K0
2631
10n
16

TR20027_001.eps
14062004

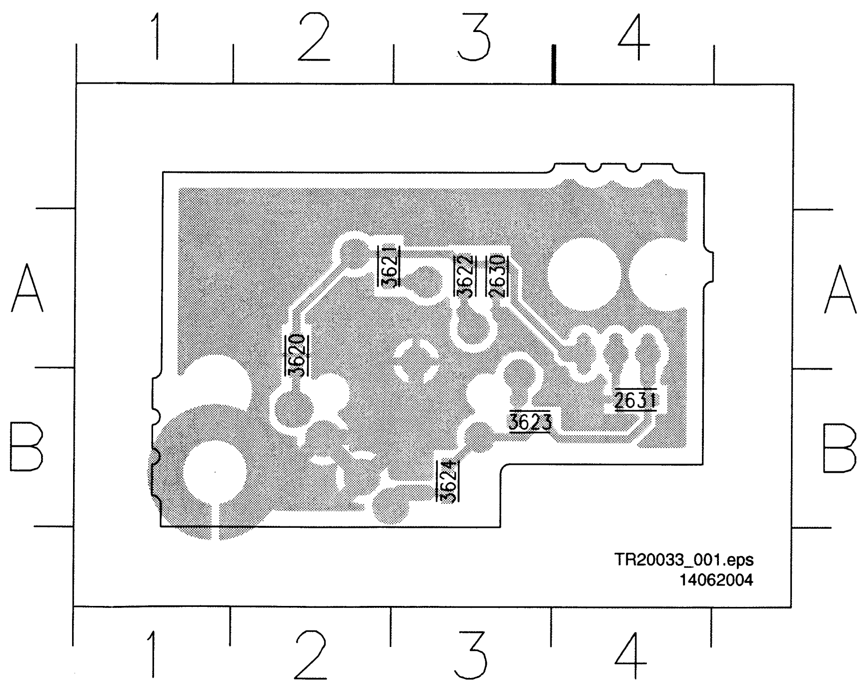
1617	B1
1620	B2
2630	B1
2631	B1
3620	A2
3621	A2
3622	B2
3623	B2
3624	B2
I621	B1
I632	B1
I633	B1

Layout MOBO: 5-Way Switch (5WSW)


1
2
3
4
A
B
3139_243_31284
1620
1617
5
6
4
3
2
1
P
b

TR20032_001.eps
14062004

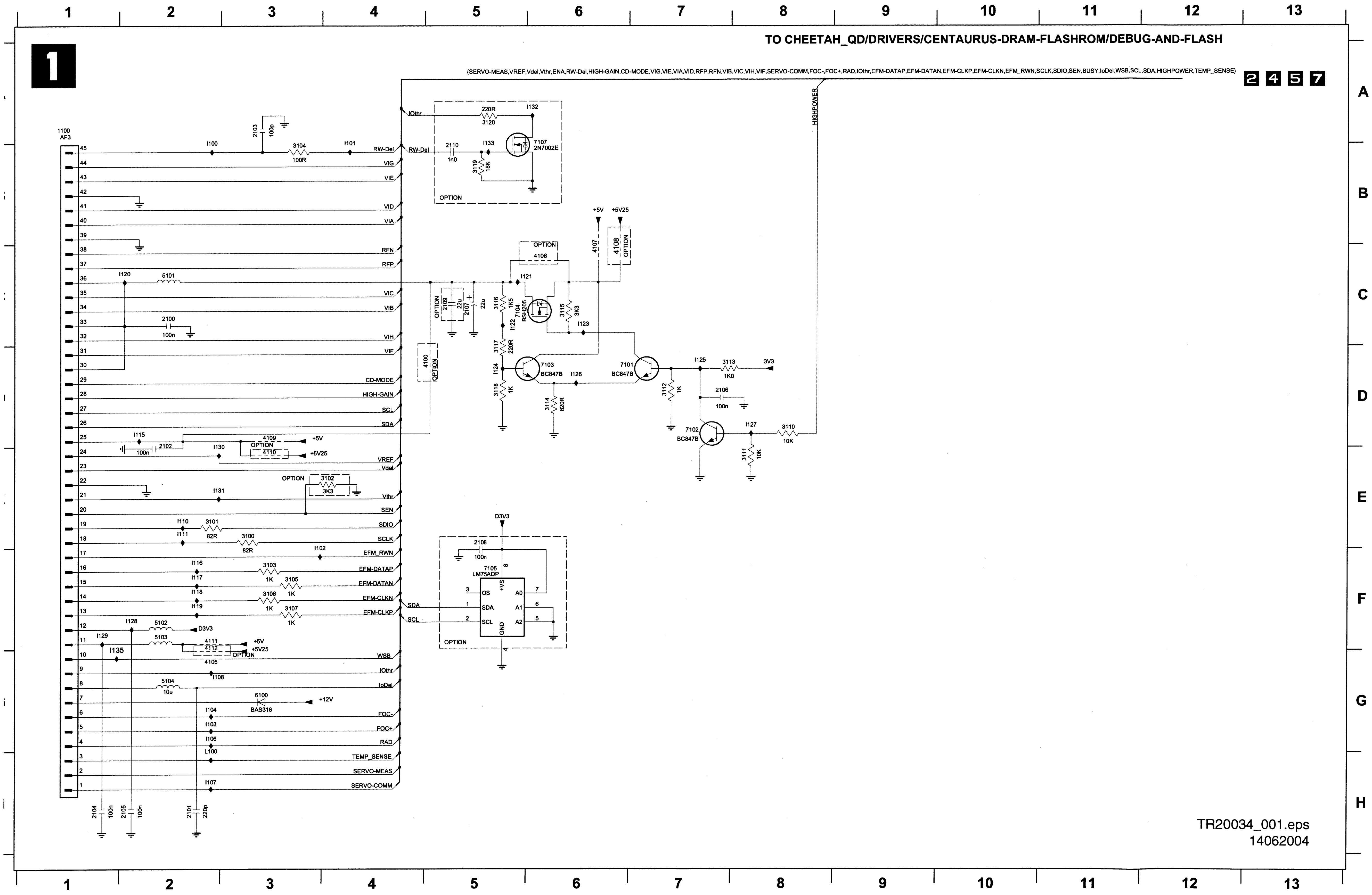
1617	A1
1620	A3


1
2
3
4
A
B
3621
3622
2630
3620
2631
3623
3624

TR20033_001.eps
14062004

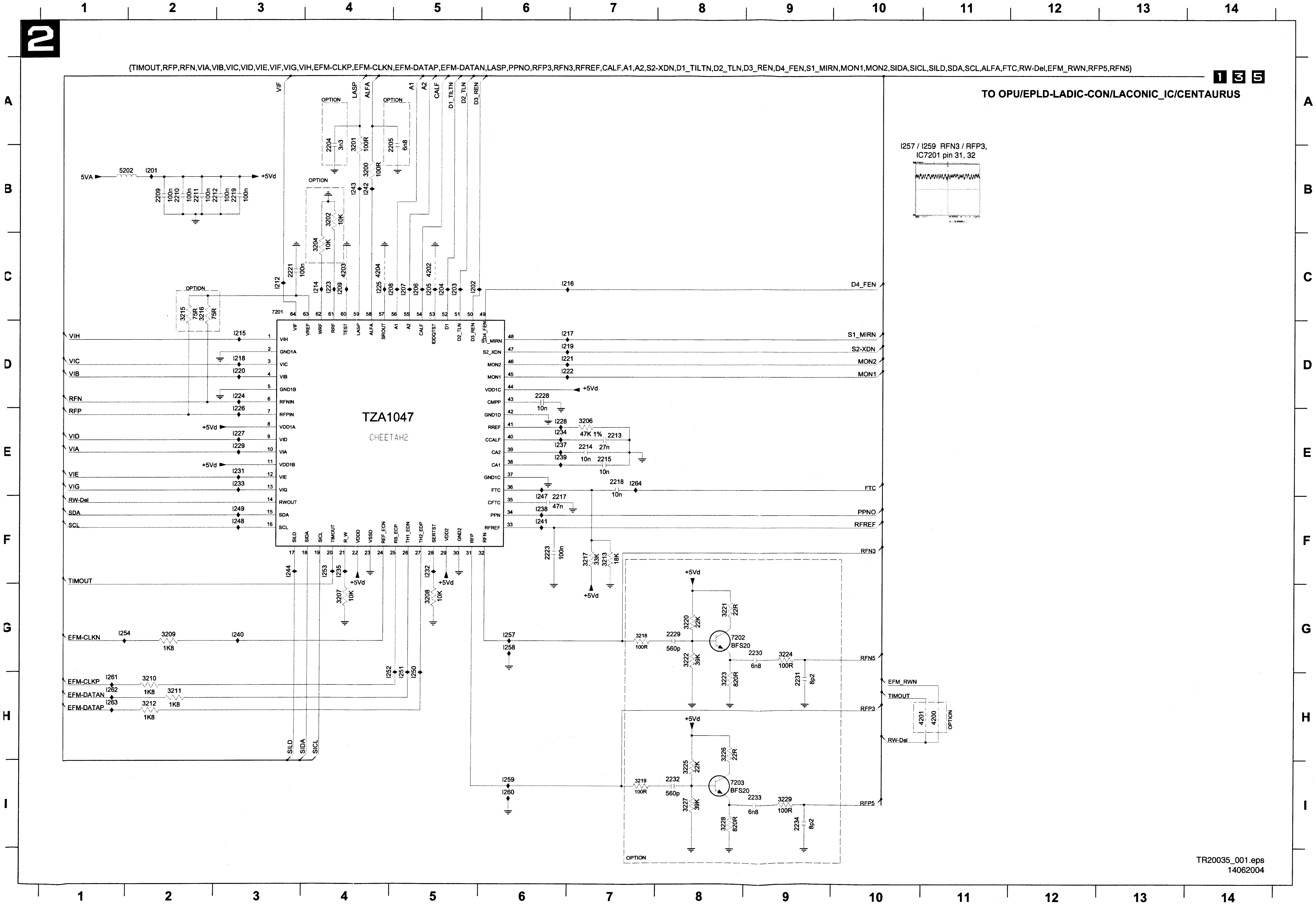
2630	A3
2631	B4
3620	A2
3622	A3
3623	B3
3624	B3

FEBE: FE OPU Interface


1
TO CHEETAH_QD/DRIVERS/CENTAURUS-DRAM-FLASHROM/DEBUG-AND-FLASH
{SERVO-MEAS,VREF,Vdel,Vthr,ENA,RW-Del,HIGH-GAIN,CD-MODE,VIG,VIE,VIA,VID,RFP,RFN,VIB,VIC,VIH,VIF,SERVO-COMM,FOC-,FOC+,RAD,IOthr,EFM-DATAP,EFM-DATAN,EFM-CLKP,EFM-CLKN,EFM_RWN,SCLK,SDIO,SEN,BUSY,IoDel,WSB,SCL,SDA,HIGHPOWER,TEMP_SENSE}
2 4 5 7
HIGHPOWER
1100
AF3
RW-Del
VIG
VIE
VID
VIA
RFN
RFP
VIC
VIB
VIH
VIF
CD-MODE
HIGH-GAIN
SCL
SDA
VREF
Vdel
Vthr
SEN
SDIO
SCLK
EFM_RWN
EFM-DATAP
EFM-DATAN
EFM-CLKN
EFM-CLKP
WSB
IOthr
IoDel
FOC-
FOC+
RAD
TEMP_SENSE
SERVO-MEAS
SERVO-COMM
3104 100R
2103 100p
3120 220R
2110 1n0
3119 18K
7107 2N7002E
OPTION
+5V
+5V25
4106
4107
4108
5101
2100 100n
2109 22u
2107 22u
4100
3116 1K5
7104 BSH205
3115 3K3
3117 220R
3118 1K
7103 BC847B
3114 820R
7101 BC847B
3112 1K
3113 1K0
3V3
2106 100n
7102 BC847B
3110 10K
3111 10K
2102 100n
4109
4110
3102 3K3
3101 82R
3100 82R
3103 1K
3105 1K
3106 1K
3107 1K
D3V3
2108 100n
7105 LM75ADP
OS
SDA
SCL
+VS
GND
A0
A1
A2
5102
5103
4111
4112
4105
5104 10u
6100 BAS316
+12V
2104 100n
2105 100n
2101 220p
TR20034_001.eps
14062004

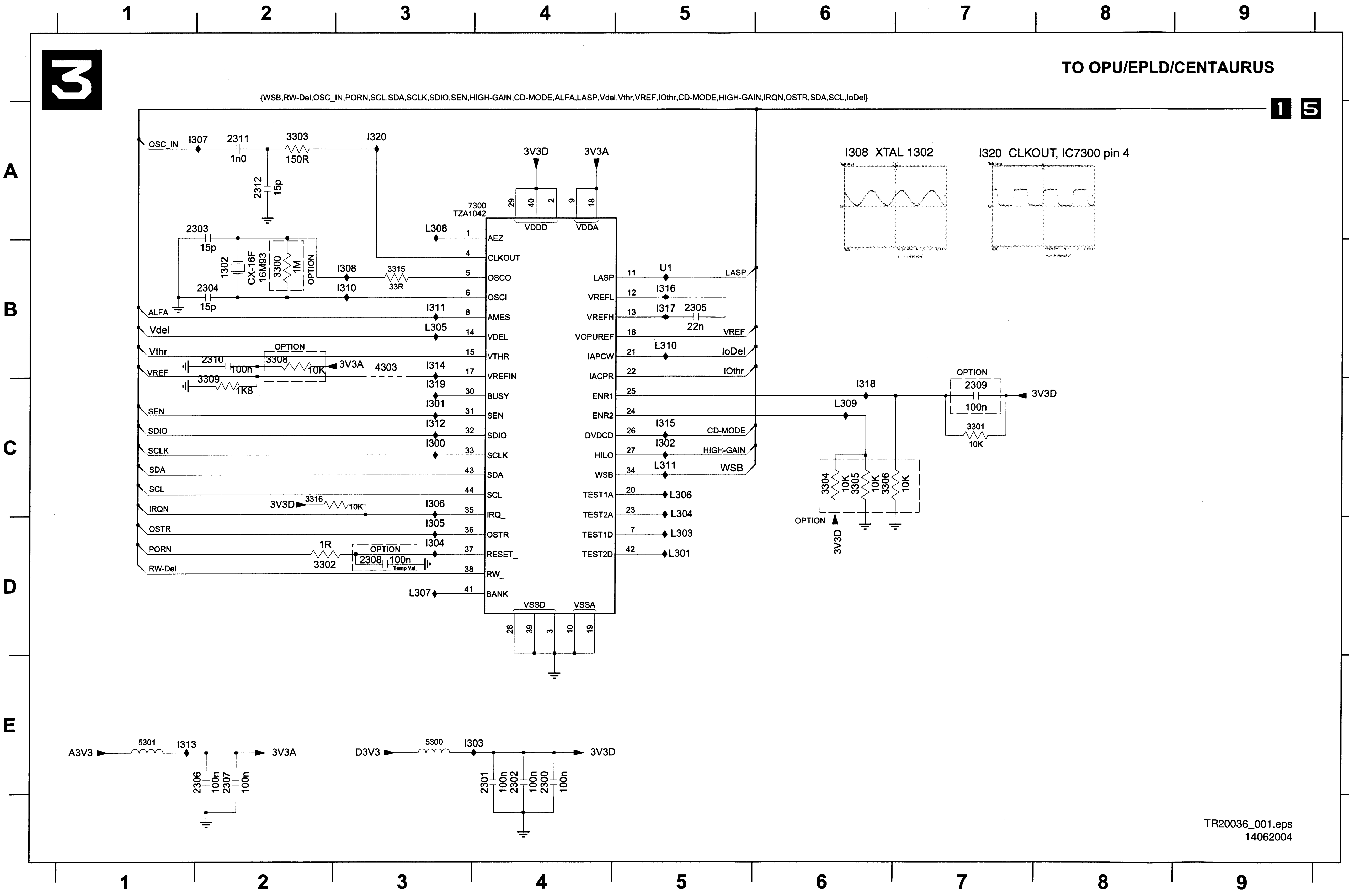
1100	A1
2100	C2
2101	H2
2102	E2
2103	A3
2104	H1
2105	H2
2106	D7
2107	C5
2108	E5
2109	C5
2110	B5
3100	E3
3101	E2
3102	E4
3103	F3
3104	B3
3105	F3
3106	F3
3107	F3
3110	D8
3111	E8
3112	D7
3113	D7
3114	D6
3115	C6
3116	C5
3117	D5
3118	D5
3119	B5
3120	A5
4100	D5
4105	G2
4106	C6
4107	C6
4108	C6
4109	D3
4110	E3
4111	F2
4112	F2
5101	C2
5102	F2
5103	F2
5104	G2
6100	G3
7101	D7
7102	D7
7103	D6
7104	C5
7105	F5
7107	B6
I100	A2
I101	A4
I102	E3
I103	G2
I104	G2
I106	G2
I107	H2
I108	G2
I110	E2
I111	E2
I115	D2
I116	F2
I117	F2
I118	F2
I119	F2
I120	C2
I121	C5
I122	C5
I123	C6
I124	D5
I125	D7
I126	D6
I127	D8
I128	F2
I129	F1
I130	D2
I131	E2
I132	A6
I133	A5
I135	F1
L100	G2

FEBE: FE Cheetah 2 Pre-processing


2
{TIMOUT,RFP,RFN,VIA,VIB,VIC,VID,VIE,VIF,VIG,VIH,EFM-CLKP,EFM-CLKN,EFM-DATAP,EFM-DATAN,LASP,PPNO,RFP3,RFN3,RFREF,CALF,A1,A2,S2-XDN,D1_TILTN,D2_TLN,D3_REN,D4_FEN,S1_MIRN,MON1,MON2,SIDA,SICL,SILD,SDA,SCL,ALFA,FTC,RW-Del,EFM_RWN,RFP5,RFN5}
1 3 5
TO OPU/EPLD-LADIC-CON/LACONIC_IC/CENTAURUS
I257 / I259 RFN3 / RFP3,
IC7201 pin 31, 32
TZA1047
CHEETAH2
7201
5VA
5202
I201
+5Vd
OPTION
7202
BFS20
7203
BFS20
D4_FEN
S1_MIRN
S2-XDN
MON2
MON1
FTC
PPNO
RFREF
RFN3
RFN5
RFP3
RFP5
EFM_RWN
TIMOUT
RW-Del
VIH
VIC
VIB
RFN
RFP
VID
VIA
VIE
VIG
SDA
SCL
EFM-CLKN
EFM-CLKP
EFM-DATAN
EFM-DATAP
SILD
SIDA
SICL
TR20035_001.eps
14062004

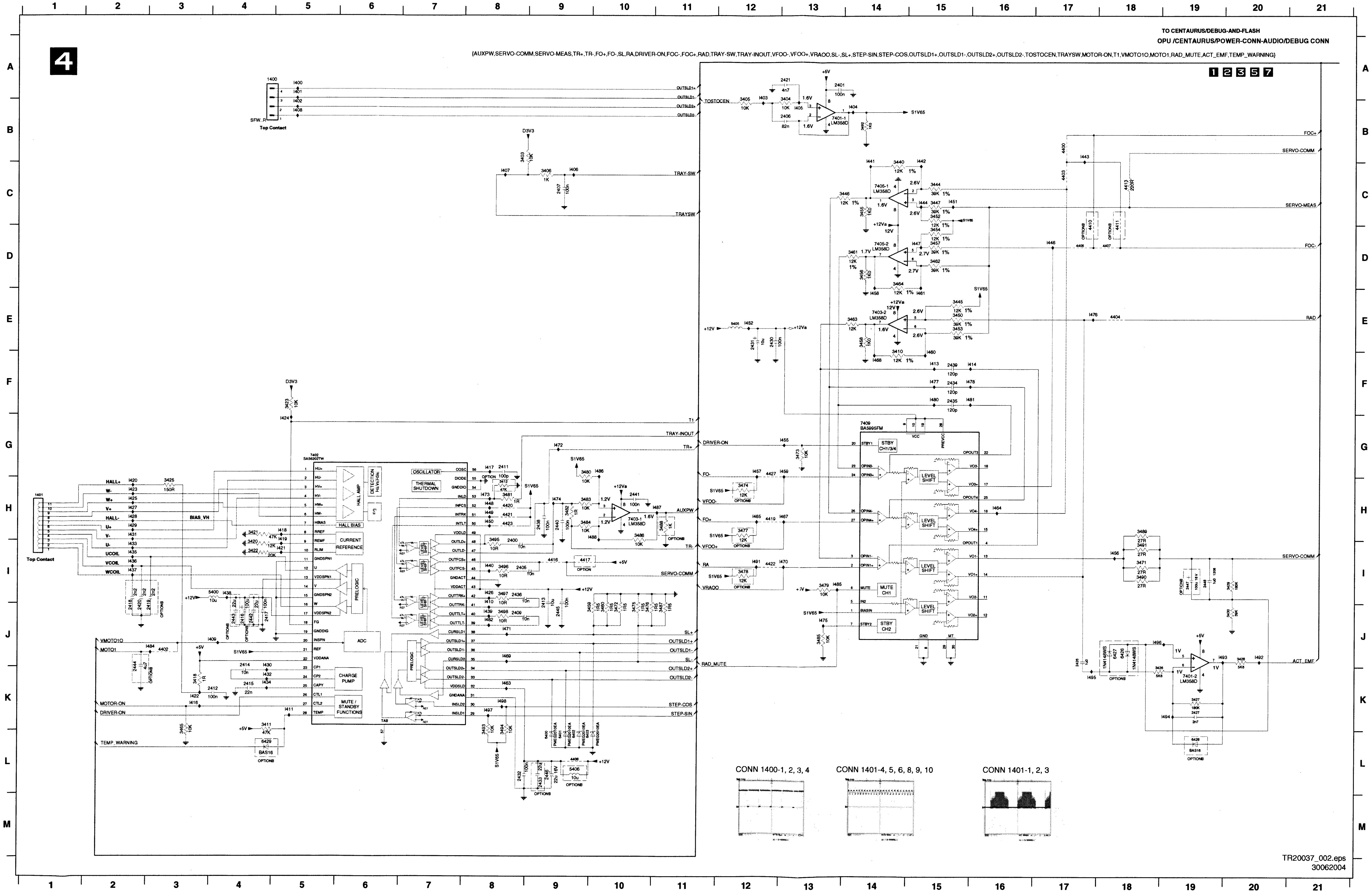
2204	B4
2205	B4
2209	B2
2210	B2
2211	B2
2212	B3
2213	E7
2214	E7
2215	E7
2217	E6
2218	E7
2219	B3
2221	C3
2223	F6
2228	D6
2229	G8
2230	G9
2231	H9
2232	I8
2233	I9
2234	I9
3200	B4
3201	B4
3202	B4
3204	C4
3206	E7
3207	G4
3208	G5
3209	G2
3210	H2
3211	H2
3212	H2
3213	F7
3215	C2
3216	C2
3217	F7
3218	G7
3219	I7
3220	G8
3221	G8
3222	G8
3223	H8
3224	G9
3225	I8
3226	H8
3227	I8
3228	I8
3229	I9
4200	H11
4201	H11
4202	C5
4203	C4
4204	C4
5202	B1
7201	C3
7202	G8
7203	I8
I201	B2
I202	C5
I203	C5
I204	C5
I205	C5
I206	C5
I207	C5
I208	C4
I209	C4
I212	C3
I214	C4
I215	D3
I216	C6
I217	D6
I218	D3
I219	D6
I220	D3
I221	D6
I222	D6
I223	C4
I224	D3
I225	C4
I226	E3
I227	E3
I228	E6
I229	E3
I231	E3
I232	F5
I233	E3
I234	E6
I235	F4
I237	E6
I238	F6
I239	E6
I240	G3
I241	F6
I242	B4
I243	B4
I244	F3
I247	F6
I248	F3
I249	F3
I250	H5
I251	H5
I252	H4
I253	F4
I254	G1
I257	G6
I258	G6
I259	I6
I260	I6
I261	H1
I262	H1
I263	H1
I264	E7

FEBE: FE Laconic Pre-processing


3
TO OPU/EPLD/CENTAURUS
{WSB,RW-Del,OSC_IN,PORN,SCL,SDA,SCLK,SDIO,SEN,HIGH-GAIN,CD-MODE,ALFA,LASP,Vdel,Vthr,VREF,IOthr,CD-MODE,HIGH-GAIN,IRQN,OSTR,SDA,SCL,IoDel}
1 5
I308 XTAL 1302
I320 CLKOUT, IC7300 pin 4
OSC_IN
I307
2311 1n0
3303 150R
I320
2312 15p
3V3D
3V3A
7300 TZA1042
VDDD
VDDA
2303 15p
1302
CX-16F 16M93
3300 1M
OPTION
I308
3315 33R
2304 15p
I310
ALFA
I311
Vdel
L305
Vthr
OPTION
3308 10K
3V3A
VREF
2310 100n
3309 1K8
4303
I314
I319
I301
SEN
SDIO
I312
SCLK
I300
SDA
SCL
IRQN
3V3D 3316 10K
I306
OSTR
I305
PORN
1R 3302
OPTION 2308 100n
I304
RW-Del
L307
L308
AEZ
CLKOUT
OSCO
OSCI
AMES
VDEL
VTHR
VREFIN
BUSY
SEN
SDIO
SCLK
SDA
SCL
IRQ_
OSTR
RESET_
RW_
BANK
VSSD
VSSA
LASP
VREFL
VREFH
VOPUREF
IAPCW
IACPR
ENR1
ENR2
DVDCD
HILO
WSB
TEST1A
TEST2A
TEST1D
TEST2D
U1
I316
I317 2305 22n
L310
IoDel
IOthr
I315
CD-MODE
I302
HIGH-GAIN
L311
L306
L304
L303
L301
I318
L309
OPTION 2309 100n
3V3D
3301 10K
3304 10K
3305 10K
3306 10K
OPTION
3V3D
A3V3
5301
I313
3V3A
2306 100n
2307 100n
D3V3
5300
I303
3V3D
2301 100n
2302 100n
2300 100n
TR20036_001.eps
14062004
A B C D E
1 2 3 4 5 6 7 8 9

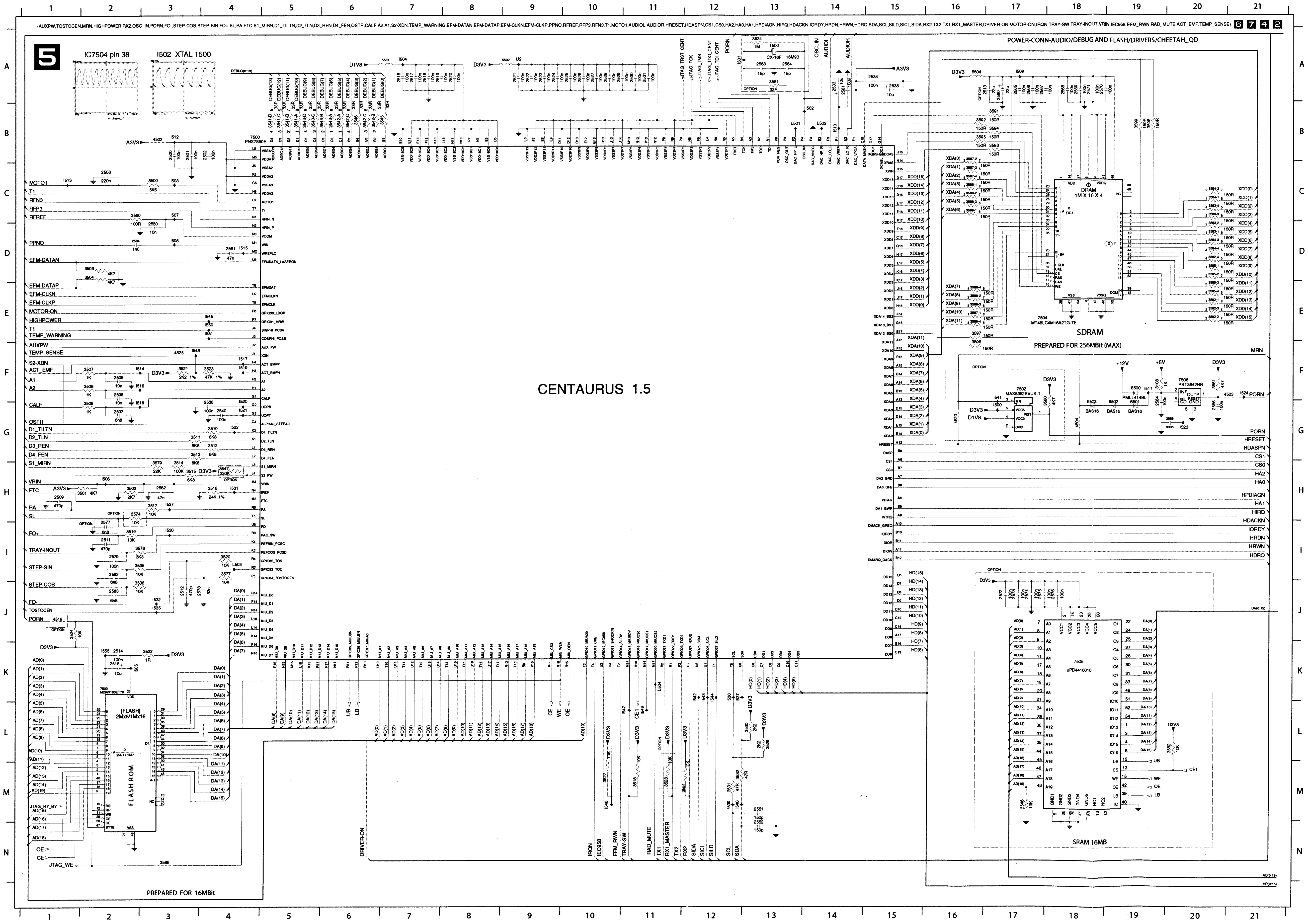
U1	B5
1302	B2
2300	E4
2301	E4
2302	E4
2303	A2
2304	B2
2305	B5
2306	E2
2307	E2
2308	D3
2309	C7
2310	B2
2311	A2
2312	A2
3300	B2
3301	C7
3302	D2
3303	A2
3304	C6
3305	C6
3306	C6
3308	B2
3309	B2
3315	B3
3316	C2
4303	B3
5300	E3
5301	E1
7300	A4
I300	C3
I301	C3
I302	C5
I303	E4
I304	D3
I305	D3
I306	C3
I307	A2
I308	B3
I310	B3
I311	B3
I312	C3
I313	E1
I314	B3
I315	C5
I316	B5
I317	B5
I318	C6
I319	C3
I320	A3
L301	D5
L303	D5
L304	C5
L305	B3
L306	C5
L307	D3
L308	A3
L309	C6
L310	B5
L311	C5

FEBE: FE Drivers


4
TO CENTAURUS/DEBUG-AND-FLASH
OPU /CENTAURUS/POWER-CONN-AUDIO/DEBUG CONN
{AUXPW,SERVO-COMM,SERVO-MEAS,TR+,TR-,FO+,FO-,SL,RA,DRIVER-ON,FOC-,FOC+,RAD,TRAY-SW,TRAY-INOUT,VFOO-,VFOO+,VRAOO,SL-,SL+,STEP-SIN,STEP-COS,OUTSLD1+,OUTSLD1-,OUTSLD2+,OUTSLD2-,TOSTOCEN,TRAYSW,MOTOR-ON,T1,VMOTO1O,MOTO1,RAD_MUTE,ACT_EMF,TEMP_WARNING}
1 2 3 5 7
1400
SFW_R
Top Contact
1401
Top Contact
7402
SA56202TW
OSCILLATOR
THERMAL SHUTDOWN
HALL AMP
DETECTION HL/VH/RH
HALL BIAS
CURRENT REFERENCE
PRELOGIC
ADC
CHARGE PUMP
MUTE / STANDBY FUNCTIONS
LEVEL SHIFT
7409
BA5995FM
STBY CH1/3/4
MUTE CH1
STBY CH2
7401-1 LM358D
7401-2 LM358D
7403-1 LM358D
7403-2 LM358D
7405-1 LM358D
7405-2 LM358D
HALL+
W-
W+
V+
HALL-
U+
V-
U-
UCOIL
VCOIL
WCOIL
BIAS_VH
VMOTO1O
MOTO1
MOTOR-ON
DRIVER-ON
TEMP_WARNING
TOSTOCEN
S1V65
TRAY-SW
TRAYSW
T1
TRAY-INOUT
TR+
TR-
AUXPW
SERVO-COMM
SL+
OUTSLD1+
OUTSLD1-
SL-
OUTSLD2+
OUTSLD2-
STEP-COS
STEP-SIN
FO-
VFOO-
FO+
VFOO+
RA
VRAOO
RAD_MUTE
FOC+
SERVO-COMM
SERVO-MEAS
FOC-
RAD
SERVO-COMM
ACT_EMF
OPTIONS
CONN 1400-1, 2, 3, 4
CONN 1401-4, 5, 6, 8, 9, 10
CONN 1401-1, 2, 3
TR20037_002.eps
30062004

1400	A5
1401	H1
2400	H8
2401	A13
2405	I8
2406	B13
2407	C9
2409	J8
2411	G8
2412	K4
2413	I9
2414	J4
2415	K4
2416	J4
2417	J4
2418	J2
2419	J3
2420	J2
2421	A13
2426	J17
2427	K19
2430	E12
2431	E12
2432	L8
2433	L9
2434	F15
2435	F15
2436	I8
2438	H9
2439	F15
2440	H9
2441	H10
2442	J4
2443	J4
2444	K2
2445	J9
2446	L9
2447	I19
2448	I19
3403	B8
3404	B13
3405	B12
3406	C9
3410	F14
3411	K4
3412	H8
3418	K3
3420	I4
3421	H4
3422	I4
3423	F5
3425	H3
3426	K18
3427	K19
3428	J20
3429	I20
3430	J20
3440	C14
3444	C15
3445	E15
3446	C13
3447	C15
3450	E15
3452	C15
3453	E15
3454	D15
3455	C14
3456	D14
3457	D15
3458	E14
3459	J10
3460	J10
3461	D14
3462	D15
3463	E14
3464	D14
3465	K3
3471	I18
3472	J10
3473	G13
3474	H12
3475	J10
3476	J10
3477	H12
3478	I12
3479	I13
3480	G9
3481	H8
3482	H9
3483	H9
3484	H9
3485	J13
3486	H10
3487	J11
3488	H11
3489	H18
3490	I18
3491	I18
3492	B14
3493	K8
3494	K8
3495	I8
3496	I8
3497	I8
3498	J8
4400	B17
4402	J3
4403	C17
4404	E18
4406	D17
4407	D18
4408	L9
4410	C17
4411	C18
4413	C18
4416	I9
4417	I9
4419	H12
4420	H8
4421	H8
4422	I12
4423	H8
4427	G12
5400	I4
5405	E12
5406	L9
6400	L9
6401	L9
6402	L9
6403	L9
6426	J18
6427	J18
6428	L19
6429	L4
7401-1	B13
7401-2	K19
7402	G5
7403-1	H10
7403-2	E14
7405-1	C14
7405-2	D14
7409	G14
I400	A5
I401	A5
I402	B5
I403	A12
I404	B14
I405	B13
I406	C9
I407	C8
I408	B5
I409	J4
I410	I8
I411	K5
I413	F15
I414	F16
I416	K3
I417	G8
I418	H5
I419	H5
I420	H2
I421	I5
I422	K3
I423	H2
I424	G5
I425	H2
I426	I8
I427	H2
I428	H2
I429	H2
I430	J4
I431	H2
I432	K4
I433	I2
I434	K4
I435	I2
I436	I2
I437	I2
I438	I4
I439	J8
I440	I8
I441	B14
I442	B15
I443	B17
I444	C15
I446	D17
I447	D15
I448	H8
I449	H8
I450	H8
I451	C15
I452	E12
I455	G13
I456	I18
I457	G12
I458	E14
I459	G13
I460	F15
I461	E15
I463	K8
I464	H16
I465	H12
I467	H13
I468	F14
I469	J8
I470	I13
I471	J8
I472	G9
I473	H8
I474	H9
I475	J13
I476	E17
I477	F15
I478	F15
I480	F15
I481	F15
I482	J8
I484	J3
I485	I13
I486	G10
I487	H11
I488	H10
I491	I12
I492	J20
I493	J19
I494	K19
I495	K17
I496	J18
I497	K8
I498	K8

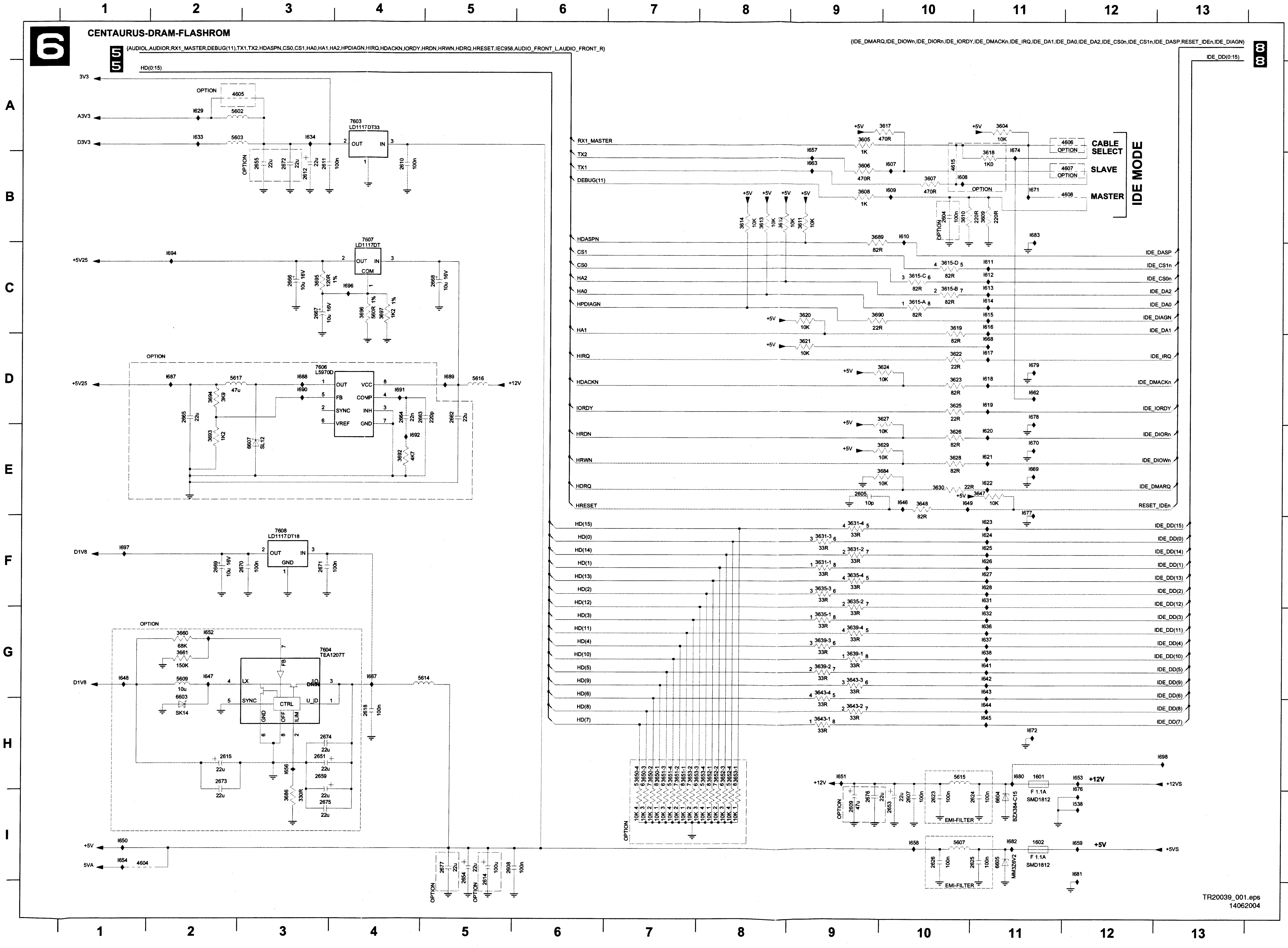
FEBE: FE Centaurus 1.5 Processor


5
IC7504 pin 38
I502 XTAL 1500
CENTAURUS 1.5
POWER-CONN-AUDIO/DEBUG AND FLASH/DRIVERS/CHEETAH_QD
7504
DRAM
1M X 16 X 4
MT48LC4M16A2TG-7E
SDRAM
PREPARED FOR 256MBit (MAX)
7502
MAX6326SVUK-T
7506
PST3642NR
PORN
MRN
7505
uPD4416016
SRAM 16MB
7503
M29W160ET70
[FLASH]
2Mx8/1Mx16
FLASH ROM
PREPARED FOR 16MBit
7500
PNX7850E
OPTION
D3V3
D1V8
A3V3
+12V
+5V
MOTO1
T1
RFN3
RFP3
RFREF
PPNO
EFM-DATAN
EFM-DATAP
EFM-CLKN
EFM-CLKP
MOTOR-ON
HIGHPOWER
TEMP_WARNING
AUXPW
TEMP_SENSE
S2-XDN
ACT_EMF
A1
A2
CALF
OSTR
D1_TILTN
D2_TLN
D3_REN
D4_FEN
S1_MIRN
VRIN
FTC
RA
SL
FO+
TRAY-INOUT
STEP-SIN
STEP-COS
FO-
TOSTOCEN
JTAG_RY_BY
JTAG_WE
OE
CE
WE
UB
LB
CE1
DRIVER-ON
IRQN
IEC958
EFM_RWN
TRAY-SW
RAD_MUTE
TX1
RX1_MASTER
TX2
RX2
SIDA
SICL
SILD
SCL
SDA
HRESET
HDASPN
CS1
CS0
HA2
HA0
HA1
HPDIAGN
HIRQ
HDACKN
IORDY
HRDN
HRWN
HDRQ
JTAG_TRST_CENT
JTAG_TCK
JTAG_TMS
JTAG_TDO_CENT
JTAG_TDI_CENT
PORN
OSC_IN
AUDIOL
AUDIOR
DEBUG(0:15)
AD(0:19)
HD(0:15)
DA(0:15)
6 7 4 2
(AUXPW,TOSTOCEN,MRN,HIGHPOWER,RX2,OSC_IN,PORN,FO-,STEP-COS,STEP-SIN,FO+,SL,RA,FTC,S1_MIRN,D1_TILTN,D2_TLN,D3_REN,D4_FEN,OSTR,CALF,A2,A1,S2-XDN,TEMP_WARNING,EFM-DATAN,EFM-DATAP,EFM-CLKN,EFM-CLKP,PPNO,RFREF,RFP3,RFN3,T1,MOTO1,AUDIOL,AUDIOR,HRESET,HDASPN,CS1,CS0,HA2,HA0,HA1,HPDIAGN,HIRQ,HDACKN,IORDY,HRDN,HRWN,HDRQ,SDA,SCL,SILD,SICL,SIDA,RX2,TX2,TX1,RX1_MASTER,DRIVER-ON,MOTOR-ON,IRQN,TRAY-SW,TRAY-INOUT,VRIN,IEC958,EFM_RWN,RAD_MUTE,ACT_EMF,TEMP_SENSE)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
A B C D E F G H I J K L M N

TR20038_001.eps
14062004

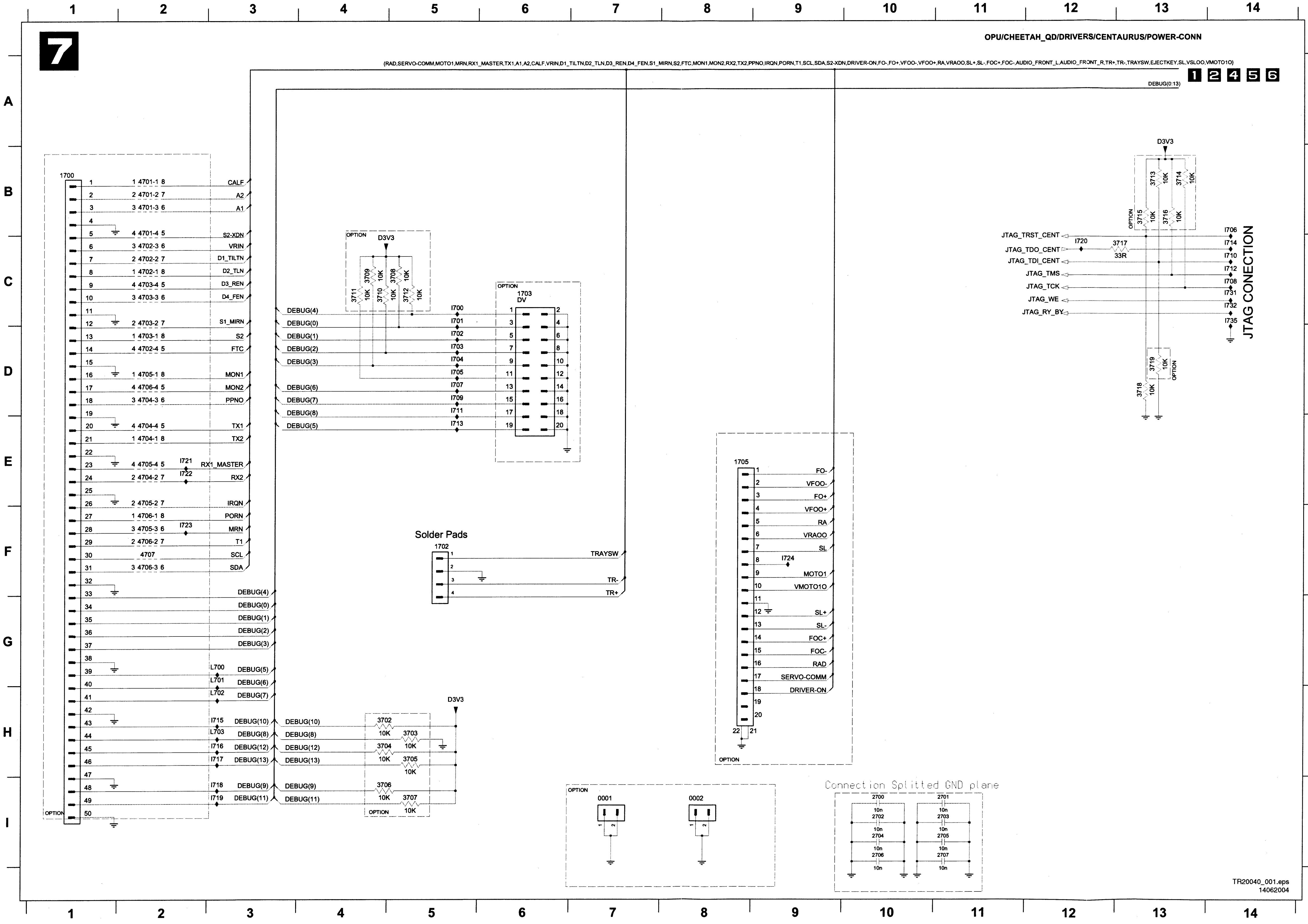
U2 A9	
1500 A13	
2500 B3	
2501 B3	
2502 B4	
2503 C2	
2504 D2	
2505 F2	
2506 F2	
2507 G2	
2509 H1	
2511 I2	
2512 J3	
2513 A17	
2514 K2	
2515 K2	
2516 A7	
2517 A7	
2518 A7	
2519 A7	
2520 A8	
2521 A9	
2522 A9	
2523 A9	
2524 A9	
2525 A10	
2526 A10	
2527 A10	
2528 A10	
2529 A10	
2530 A11	
2531 A11	
2533 A14	
2534 A15	
2536 G4	
2538 A15	
2540 G4	
2550 D3	
2551 M13	
2552 N13	
2561 D4	
2562 H3	
2563 A13	
2564 A13	
2565 A17	
2566 A17	
2567 A17	
2568 A18	
2569 A18	
2570 A18	
2571 A18	
2572 J17	
2573 J17	
2574 J17	
2575 J17	
2576 J18	
2577 I2	
2578 J4	
2579 I2	
2580 A17	
2581 A14	
2582 I2	
2583 J2	
2584 G19	
2585 G20	
2586 G20	
3108 F19	
3500 C3	
3501 H2	
3502 H2	
3503 D2	
3504 D2	
3507 F2	
3508 F2	
3509 G2	
3510 G4	
3511 G3	
3512 G4	
3513 G3	
3514 H3	
3515 H3	
3516 H4	
3517 H3	
3518 M11	
3519 I2	
3520 I4	
3521 F3	
3522 K3	
3523 F4	
3524 J1	
3527 M10	
3528 M11	
3529 L13	
3530 L13	
3531 M12	
3532 M12	
3534 A13	
3535 I2	
3536 J2	
3541-A B5	
3541-B B5	
3541-C B5	
3541-D B5	
3542-A B6	
3542-B B6	
3542-C B6	
3542-D B6	
3543-A B6	
3543-B B6	
3543-C B5	
3543-D B5	
3545 B7	
3546 B6	
3547 H4	
3548 M17	
3551 M12	
3560 C2	
3561 F20	
3562-1 E20	
3562-2 E20	
3562-3 E20	
3562-4 D20	
3574 H2	
3577 I4	
3578 I2	
3579 H3	
3580 G18	
3581 A13	
3582 L20	
3583-1 D20	
3583-2 D20	
3583-3 C20	
3583-4 C20	
3584-1 C20	
3584-2 C20	
3584-3 D20	
3584-4 D20	
3585-1 D20	
3585-2 D20	
3585-3 E20	
3585-4 E20	
3586 N3	
3587-1 E16	
3587-2 B16	
3587-3 C16	
3587-4 C16	
3588-1 C16	
3588-2 C16	
3588-3 C16	
3588-4 E16	
3589-1 C16	
3589-2 E16	
3589-3 E16	
3589-4 E16	
3591 B17	
3592 B16	
3593 B17	
3594 B17	
3595 B16	
3596 F16	
3597 E16	
3598 B19	
3599 B19	
4502 B3	
4503 F21	
4504 G18	
4519 J1	
4520 G16	
4525 F3	
5501 A7	
5502 A9	
5504 A16	
6500 F19	
6501 G19	
6502 G19	
6503 G18	
7500 B4	
7502 F17	
7503 K2	
7504 E18	
7505 K18	
7506 F20	
I500 G17	
I501 A12	
I502 B14	
I503 C3	
I504 A7	
I505 K2	
I506 H2	
I507 C3	
I508 D3	
I509 A17	
I510 B14	
I511 F19	
I512 B3	
I513 C1	
I514 F2	
I515 D4	
I516 F2	
I517 F4	
I518 G2	
I519 F4	
I520 G4	
I521 G4	
I522 G4	
I523 G20	
I524 F21	
I527 H3	
I530 I3	
I531 H4	
I532 J3	
I535 J3	
I536 K12	
I537 K12	
I539 M12	
I540 M12	
I541 F17	
I542 K12	
I543 K12	
I544 K12	
I545 E4	
I546 M10	
I547 L11	
I548 F3	
I549 L11	
I550 E4	
I551 E4	
I555 K2	
L501 B13	
L502 B14	
L503 I4	
L504 K11	

FEBE: FE Supply / BE Interface


6
CENTAURUS-DRAM-FLASHROM
5
8
(AUDIOL,AUDIOR,RX1_MASTER,DEBUG(11),TX1,TX2,HDASPN,CS0,CS1,HA0,HA1,HA2,HPDIAGN,HIRQ,HDACKN,IORDY,HRDN,HRWN,HDRQ,HRESET,IEC958,AUDIO_FRONT_L,AUDIO_FRONT_R)
(IDE_DMARQ,IDE_DIOWn,IDE_DIORn,IDE_IORDY,IDE_DMACKn,IDE_IRQ,IDE_DA1,IDE_DA0,IDE_DA2,IDE_CS0n,IDE_CS1n,IDE_DASP,RESET_IDEn,IDE_DIAGN)
HD(0:15)
IDE_DD(0:15)
3V3
A3V3
D3V3
+5V25
D1V8
+5V
5VA
+12V
+12VS
+5VS
7603 LD1117DT33
7607 LD1117DT
7606 L5970D
7608 LD1117DT18
7604 TEA1207T
OPTION
CABLE SELECT
SLAVE
MASTER
IDE MODE
EMI-FILTER
F 1.1A SMD1812
BZX384-C15
MM3Z6V2
TR20039_001.eps
14062004

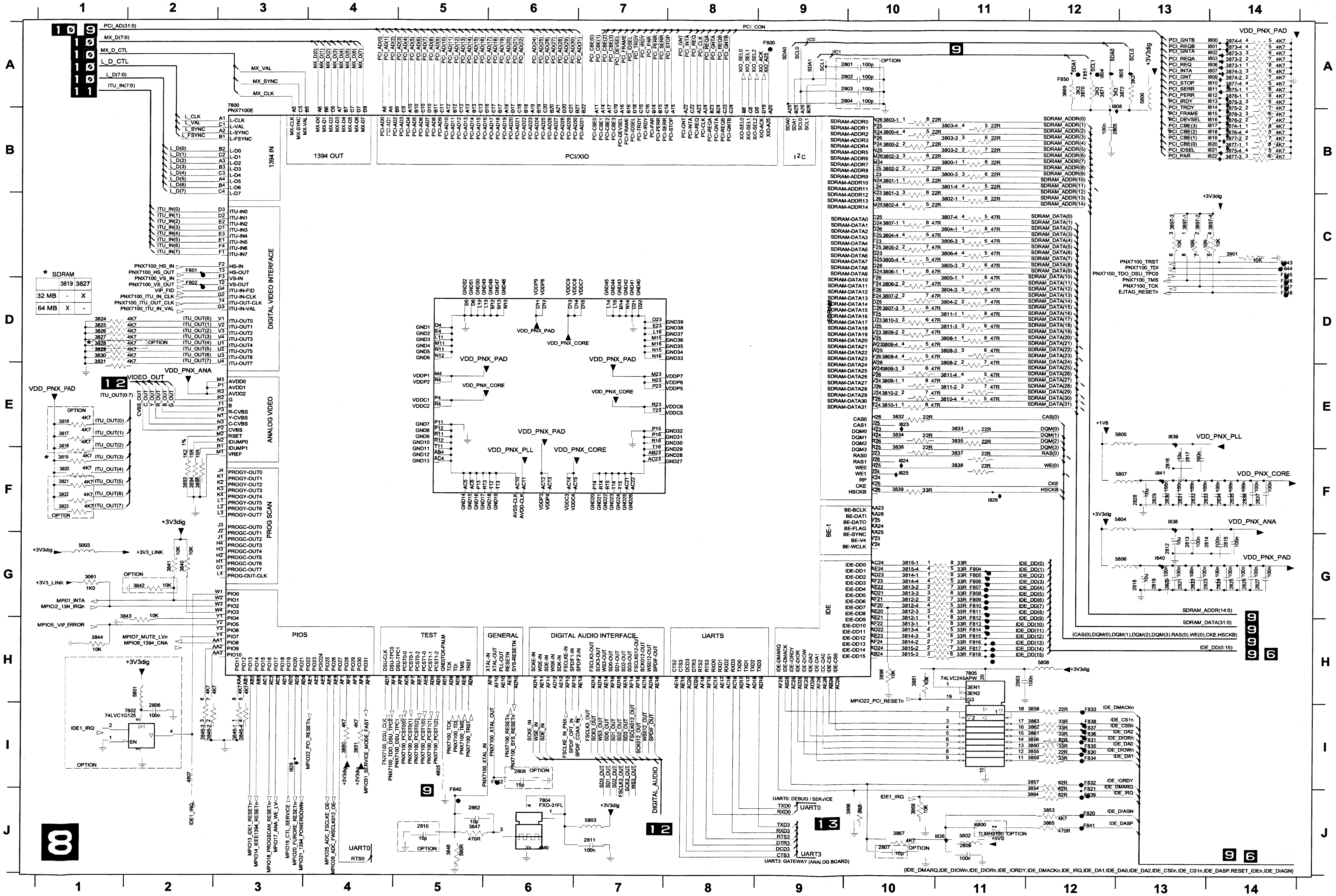
1601	H11
1602	I11
2604	B10
2605	E9
2607	I10
2608	I5
2609	I9
2610	B4
2611	B3
2612	B3
2614	I5
2615	H2
2618	H4
2623	I10
2624	I11
2625	I11
2626	I10
2651	H3
2653	I10
2654	I5
2655	B3
2659	H3
2662	D5
2663	D4
2664	D4
2665	D2
2666	C3
2667	C3
2668	C5
2669	F2
2670	F3
2671	F3
2672	B3
2673	H2
2674	H3
2675	I3
2676	I9
2677	I5
3604	A11
3605	A9
3606	B9
3607	B10
3608	B9
3609	B11
3610	B10
3611	B9
3612	B8
3613	B8
3614	B8
3615-A	C10
3615-B	C10
3615-C	C10
3615-D	C10
3617	A10
3618	B11
3619	C10
3620	C9
3621	D9
3622	D10
3623	D10
3624	D10
3625	D10
3626	E10
3627	D10
3628	E10
3629	E10
3630	E10
3631-1	F9
3631-2	F9
3631-3	F9
3631-4	F9
3635-1	G9
3635-2	F9
3635-3	F9
3635-4	F9
3639-1	G9
3639-2	G9
3639-3	G9
3639-4	G9
3643-1	H9
3643-2	H9
3643-3	G9
3643-4	G9
3647	E11
3648	E10
3650-1	H7
3650-2	H7
3650-3	H7
3650-4	H7
3651-1	H7
3651-2	H7
3651-3	H7
3651-4	H7
3652-1	H8
3652-2	H8
3652-3	H8
3652-4	H8
3653-1	H8
3653-2	H7
3653-3	H8
3653-4	H8
3660	G2
3661	G2
3684	E10
3686	I3
3689	B9
3690	C9
3692	E4
3693	E2
3694	D2
3695	C3
3696	C4
3697	C4
4604	I1
4605	A2
4606	A12
4607	B12
4608	B12
4615	B10
5602	A2
5603	A2
5607	I10
5609	G2
5614	G5
5615	H10
5616	D5
5617	D2
6603	H2
6604	I11
6605	I11
6607	E3
7603	A4
7604	G3
7606	D3
7607	B4
7608	F3
I538	I12
I607	B10
I608	B10
I609	B10
I610	B10
I611	C11
I612	C11
I613	C11
I614	C11
I615	C11
I616	C11
I617	D11
I618	D11
I619	D11
I620	E11
I621	E11
I622	E11
I623	F11
I624	F11
I625	F11
I626	F11
I627	F11
I628	F11
I629	A2
I631	F11
I632	G11
I633	A2
I634	A3
I636	G11
I637	G11
I638	G11
I641	G11
I642	G11
I643	G11
I644	H11
I645	H11
I646	E10
I647	G2
I648	G1
I649	E10
I650	I1
I651	H9
I652	G2
I653	H12
I654	I1
I656	H3
I657	A9
I658	I10
I659	I12
I662	D11
I663	B9
I667	G4
I668	D11
I669	E11
I670	E11
I671	B11
I672	H11
I674	A11
I676	H12
I677	E11
I678	D11
I679	D11
I680	H11
I681	I12
I682	I11
I683	B11
I687	D2
I688	D3
I689	D5
I690	D3
I691	D4
I692	E4
I694	C2
I696	C4
I697	F1
I698	H13

FEBE: FE Tray Motor / Switch Connection & Debug Connectors


7
OPU/CHEETAH_QD/DRIVERS/CENTAURUS/POWER-CONN
{RAD,SERVO-COMM,MOTO1,MRN,RX1_MASTER,TX1,A1,A2,CALF,VRIN,D1_TILTN,D2_TLN,D3_REN,D4_FEN,S1_MIRN,S2,FTC,MON1,MON2,RX2,TX2,PPNO,IRQN,PORN,T1,SCL,SDA,S2-XDN,DRIVER-ON,FO-,FO+,VFOO-,VFOO+,RA,VRAOO,SL+,SL-,FOC+,FOC-,AUDIO_FRONT_L,AUDIO_FRONT_R,TR+,TR-,TRAYSW,EJECTKEY,SL,VSLOO,VMOTO1O}
1 2 4 5 6
DEBUG(0:13)
1700
OPTION
CALF
A2
A1
S2-XDN
VRIN
D1_TILTN
D2_TLN
D3_REN
D4_FEN
S1_MIRN
S2
FTC
MON1
MON2
PPNO
TX1
TX2
RX1_MASTER
RX2
IRQN
PORN
MRN
T1
SCL
SDA
4707
I721
I722
I723
DEBUG(4)
DEBUG(0)
DEBUG(1)
DEBUG(2)
DEBUG(3)
L700
L701
L702
L703
DEBUG(5)
DEBUG(6)
DEBUG(7)
I715
I716
I717
I718
I719
DEBUG(10)
DEBUG(8)
DEBUG(12)
DEBUG(13)
DEBUG(9)
DEBUG(11)
D3V3
3702 10K
3703 10K
3704 10K
3705 10K
3706 10K
3707 10K
OPTION
D3V3
3709 10K
3708 10K
3711 10K
3710 10K
3712 10K
1703
DV
I700
I701
I702
I703
I704
I705
I707
I709
I711
I713
Solder Pads
1702
TRAYSW
TR-
TR+
1705
FO-
VFOO-
FO+
VFOO+
RA
VRAOO
SL
I724
MOTO1
VMOTO1O
SL+
SL-
FOC+
FOC-
RAD
SERVO-COMM
DRIVER-ON
0001
0002
Connection Splitted GND plane
2700 10n
2701 10n
2702 10n
2703 10n
2704 10n
2705 10n
2706 10n
2707 10n
D3V3
3713 10K
3714 10K
3715 10K
3716 10K
JTAG_TRST_CENT
JTAG_TDO_CENT
JTAG_TDI_CENT
JTAG_TMS
JTAG_TCK
JTAG_WE
JTAG_RY_BY
I720
3717 33R
I706
I714
I710
I712
I708
I731
I732
I735
3718 10K
3719 10K
JTAG CONECTION
TR20040_001.eps
14062004

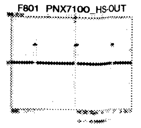
0001	I7
0002	I8
1700	B1
1702	F5
1703	C6
1705	E8
2700	I10
2701	I11
2702	I10
2703	I11
2704	I10
2705	I11
2706	I10
2707	I11
3702	H4
3703	H5
3704	H4
3705	H5
3706	I4
3707	I5
3708	C5
3709	C4
3710	C4
3711	C4
3712	C5
3713	B1
3714	B1
3715	B1
3716	B1
3717	C1
3718	D1
3719	D1
4701-1	B
4701-2	B
4701-3	B
4701-4	B
4702-1	C
4702-2	C
4702-3	C
4702-4	D
4703-1	D
4703-2	C
4703-3	C
4703-4	C
4704-1	E
4704-2	E
4704-3	D
4704-4	E
4705-1	D
4705-2	E
4705-3	F
4705-4	E
4706-1	F
4706-2	F
4706-3	F
4706-4	D
4707	F2
I700	C5
I701	C5
I702	D5
I703	D5
I704	D5
I705	D5
I706	B14
I707	D5
I708	C14
I709	D5
I710	C14
I711	D5
I712	C14
I713	E5
I714	C14
I715	H3
I716	H3
I717	H3
I718	I3
I719	I3
I720	C12
I721	E2
I722	E2
I723	F2
I724	F9
I731	C14
I732	C14
I735	C14
L700	G3
L701	G3
L702	H3
L703	H3

FEBE: BE Chrysalis

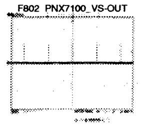

7800
PNX7100E
1394 IN
1394 OUT
PCI/XIO
I2C
DIGITAL VIDEO INTERFACE
ANALOG VIDEO
PROG SCAN
PIOS
TEST
GENERAL
DIGITAL AUDIO INTERFACE
UARTS
IDE
BE-1
VIDEO_OUT
VDD_PNX_PAD
VDD_PNX_CORE
VDD_PNX_PLL
VDD_PNX_ANA
+3V3dig
+3V3_LINK
+1V8
PCI_AD(31:0)
MX_D(7:0)
MX_D_CTL
L_D_CTL
L_D(7:0)
ITU_IN(7:0)
ITU_OUT(7:0)
PCI_CON
SDRAM_ADDR(14:0)
SDRAM_DATA(31:0)
(CAS(0),DQM(0),DQM(1),DQM(2),DQM(3),RAS(0),WE(0),CKE,HSCKB)
IDE_DD(0:15)
(IDE_DMARQ,IDE_DIOWn,IDE_DIORn,IDE_IORDY,IDE_DMACKn,IDE_IRQ,IDE_DA1,IDE_DA0,IDE_DA2,IDE_CS0n,IDE_CS1n,IDE_DASP,RESET_IDEn,IDE_DIAGN)
* SDRAM | 3819 | 3827
32 MB | - | X
64 MB | X | -
OPTION
74LVC1G125
7802
IDE1_IRQ
74LVC245APW
7805
MPIO22_PCI_RESETn
7804
FXO-31FL
DIGITAL_AUDIO
UART0: DEBUG / SERVICE
UART3: GATEWAY (ANALOG BOARD)
TLMH3100
PNX7100_TRST
PNX7100_TDI
PNX7100_TDO_DSU_TPC0
PNX7100_TMS
PNX7100_TCK
EJTAG_RESETn
1 0
1 1
1 2
1 3
8
9
6
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A B C D E F G H I J

2801	A9
2802	A9
2803	A9
2804	A9
2805	B12
2806	I2
2807	J10
2808	I6
2809	J11
2810	J5
2811	J7
2812	G13
2813	G13
2814	G14
2815	G14
2816	F13
2817	F13
2818	G13
2819	G13
2820	G13
2821	G13
2822	G13
2823	G13
2824	G14
2825	G14
2826	G14
2827	G14
2828	F13
2829	F13
2830	F13
2831	F13
2832	F13
2833	F13
2834	F14
2835	F14
2836	F14
2837	F14
2862	J5
2863	H11
3061	G1
3800-1	B11
3800-2	B10
3800-3	B11
3800-4	B10
3801-1	B10
3801-3	C10
3801-4	B11
3802-1	C11
3802-2	B10
3802-3	B10
3802-4	C10
3803-1	B10
3803-2	B11
3803-3	B11
3803-4	B11
3804-1	C11
3804-2	D11
3804-3	D11
3804-4	C10
3805-1	D11
3805-2	C10
3805-3	C11
3805-4	C10
3806-1	C10
3806-2	D10
3806-3	C11
3806-4	C11
3807-1	C10
3807-2	D10
3807-3	D10
3807-4	C11
3808-1	D11
3808-2	E11
3808-3	D11
3808-4	D10
3809-1	E10
3809-2	D10
3809-3	E10
3809-4	D10
3810-1	E10
3810-2	E10
3810-3	D10
3810-4	E11
3811-1	D11
3811-2	E11
3811-3	D11
3811-4	E11
3812-1	H10
3812-2	G10
3812-3	G10
3812-4	G10
3813-1	H10
3813-2	G10
3813-3	G10
3813-4	H10
3814-1	G10
3814-2	H10
3814-3	H10
3814-4	G10
3815-1	G10
3815-2	H10
3815-3	H10
3815-4	G10
3816	E1
3817	E1
3818	F1
3819	F1
3820	F1
3821	F1
3822	F1
3823	F1
3824	D1
3825	D1
3826	D1
3827	D1
3828	D1
3829	D1
3830	D1
3831	E1
3832	E10
3833	E11
3834	E10
3835	E11
3836	F10
3837	F11
3838	F11
3839	F10
3840	G2
3841	G2
3842	G2
3843	H2
3844	H1
3846-1	I3
3846-2	I2
3846-3	I2
3846-4	I3
3847	J5
3848	J5
3851	I4
3853	J12
3854	J12
3855	I12
3856	I12
3857	I12
3858	I12
3859	I12
3860	I12
3861	I12
3862	I12
3863	I12
3864	J12
3865	J12
3866	J10
3867	J10
3868	J10
3869	A12
3870	A12
3871	A12
3872	A13
3873-1	A14
3873-2	A14
3873-3	A14
3873-4	A14
3874-1	B14
3874-2	A14
3874-3	A14
3874-4	A14
3875-1	A14
3875-2	B14
3875-3	A14
3875-4	B14
3876-1	A14
3876-2	B14
3876-3	B14
3876-4	B14
3877-1	B14
3877-2	B14
3877-3	B14
3877-4	A14
3880	I4
3881	H10
3893	F2
3894	F2
3895	F2
3896	H10
3897-1	C13
3897-2	C13
3897-3	C13
3897-4	C14
3901	C14
4805	I5
4807	I2
5003	G1
5800	A13
5801	H2
5802	J11
5803	J7
5804	F13
5805	E13
5806	G13
5807	F13
5808	H12
6800	J11
7800	B3
7802	I2
7804	J6
7805	H11
F800	A9
F801	C2
F802	D2
F804	G11
F805	G11
F806	G11
F807	G11
F808	G11
F809	G11
F810	G11
F811	G11
F812	H11
F813	H11
F814	H11
F815	H11
F816	H11
F817	H11
F818	H11
F820	J12
F821	J12
F830	I12
F831	I12
F832	I12
F833	I12
F834	I12
F835	I12
F836	I12
F837	I12
F838	I12
F839	J12
F840	J5
F841	J12
F842	I6
F843	C14
F844	C14
F845	C14
F846	D14
F847	D14
F848	D14
F850	A12
F851	A12
I800	A14
I801	A14
I802	A14
I803	A14
I804	A12
I805	A13
I806	A14
I807	A14
I808	A12
I809	A14
I810	A14
I811	A14
I812	A14
I813	A14
I814	A14
I815	B14
I816	B14
I817	B14
I818	B14
I819	B14
I820	B14
I821	B14
I822	B14
I823	E10
I824	F10
I825	F10
I826	F11
I828	I3
I836	J11
I838	F13
I839	E13
I840	G13
I841	F13

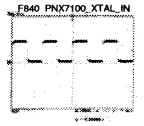
F801 PNX7100_HS-OUT



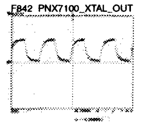
F802 PNX7100_VS-OUT



F840 PNX7100_XTAL_IN

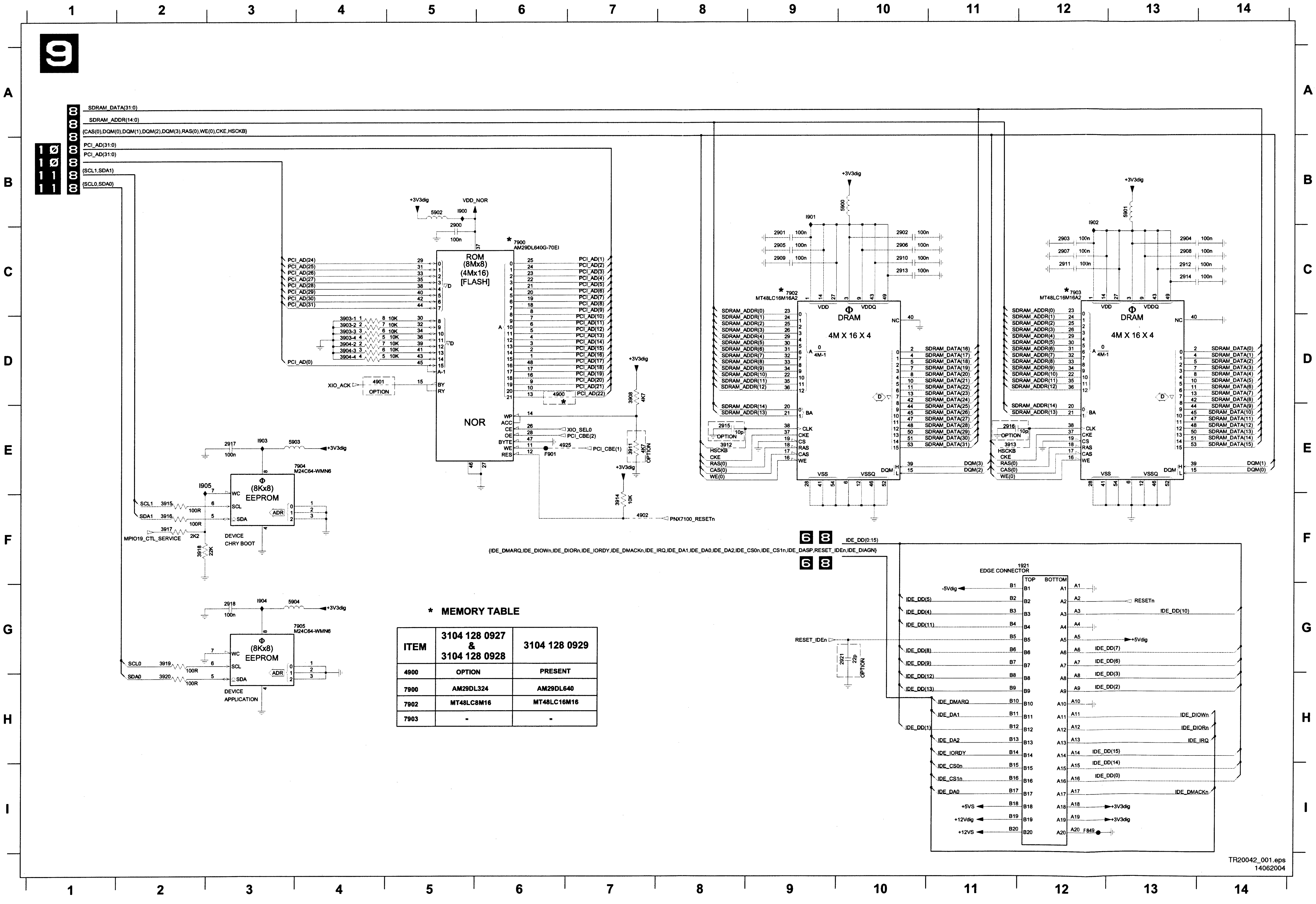


F842 PNX7100_XTAL_OUT



TR20041_001.eps
14062004

FEBE: BE Flash, EEPROM & SDRAM

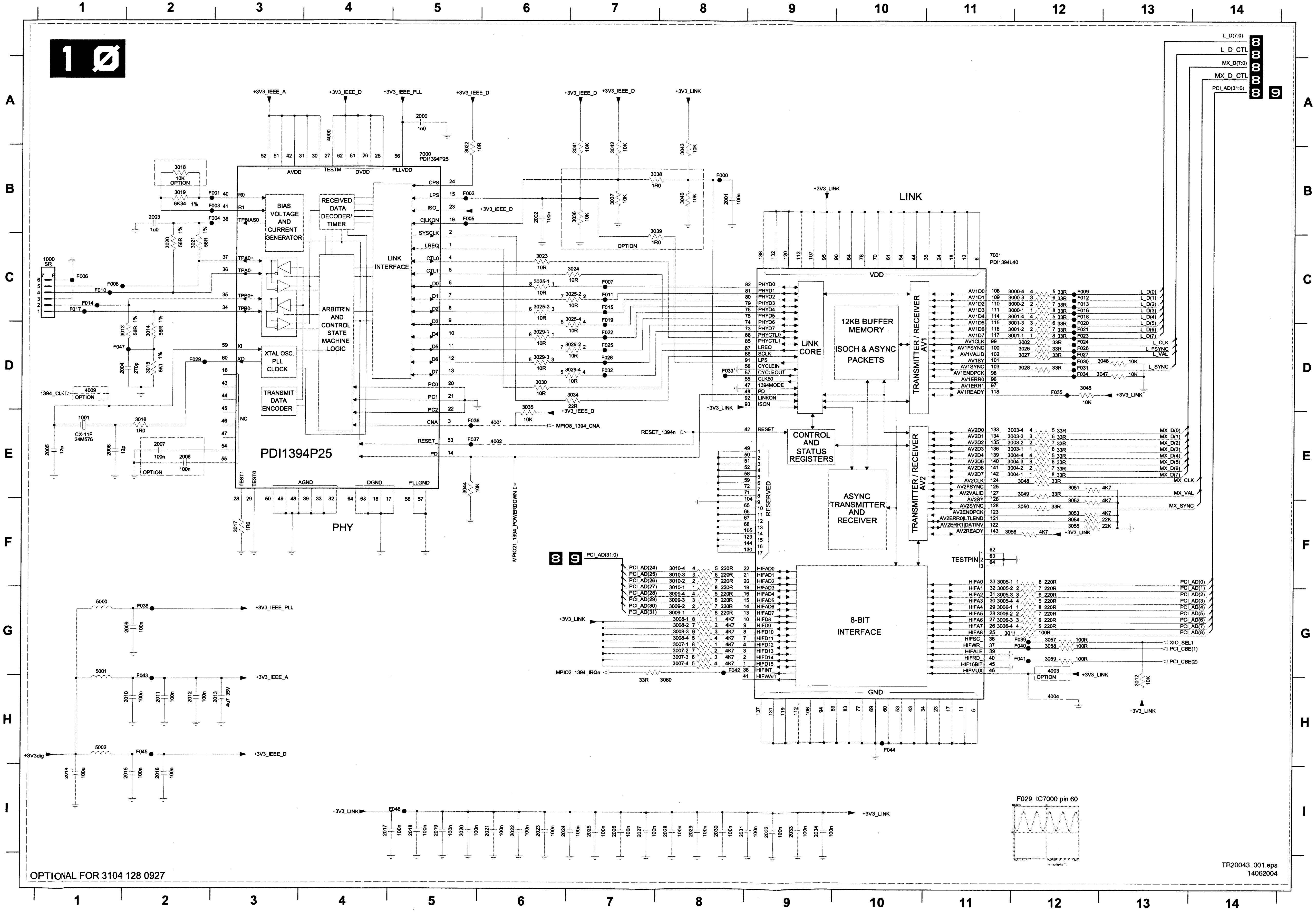

9
SDRAM_DATA(31:0)
SDRAM_ADDR(14:0)
(CAS(0),DQM(0),DQM(1),DQM(2),DQM(3),RAS(0),WE(0),CKE,HSCKB)
PCI_AD(31:0)
(SCL1,SDA1)
(SCL0,SDA0)
+3V3dig
VDD_NOR
5902
I900
2900
100n
7900
AM29DL640G-70EI
ROM
(8Mx8)
(4Mx16)
[FLASH]
NOR
WP
ACC
CE
OE
BYTE
WE
RES
BY
RY
XIO_ACK
4901
OPTION
4900
XIO_SEL0
PCI_CBE(2)
4925
PCI_CBE(1)
F901
3908
4K7
3911
4K7
OPTION
3914
10K
4902
PNX7100_RESETn
2917
I903
5903
7904
M24C64-WMN6
Φ
(8Kx8)
EEPROM
WC
SCL
SDA
ADR
I905
SCL1
3915
SDA1
3916
100R
3917
MPIO19_CTL_SERVICE
2K2
3918
22K
DEVICE
CHRY BOOT
2918
I904
5904
7905
M24C64-WMN6
SCL0
3919
SDA0
3920
DEVICE
APPLICATION
3903-1
3903-2
3903-3
3903-4
3904-2
3904-3
3904-4
10K
I901
5900
2901
2902
2905
2906
2909
2910
2913
7902
MT48LC16M16A2
DRAM
4M X 16 X 4
VDD
VDDQ
VSS
VSSQ
NC
DQM
BA
CLK
CKE
CS
RAS
CAS
WE
2915
10p
OPTION
3912
HSCKB
CKE
RAS(0)
CAS(0)
WE(0)
DQM(3)
DQM(2)
I902
5901
2903
2904
2907
2908
2911
2912
2914
7903
MT48LC16M16A2
2916
3913
DQM(1)
DQM(0)
IDE_DD(0:15)
(IDE_DMARQ,IDE_DIOWn,IDE_DIORn,IDE_IORDY,IDE_DMACKn,IDE_IRQ,IDE_DA1,IDE_DA0,IDE_DA2,IDE_CS0n,IDE_CS1n,IDE_DASP,RESET_IDEn,IDE_DIAGN)
6 8
1921
EDGE CONNECTOR
TOP
BOTTOM
RESET_IDEn
2921
22p
OPTION
-5Vdig
RESETn
+5Vdig
+5VS
+12Vdig
+12VS
+3V3dig
F849
TR20042_001.eps
14062004

*** MEMORY TABLE**

ITEM	3104 128 0927 & 3104 128 0928	3104 128 0929
4900	OPTION	PRESENT
7900	AM29DL324	AM29DL640
7902	MT48LC8M16	MT48LC16M16
7903	-	-

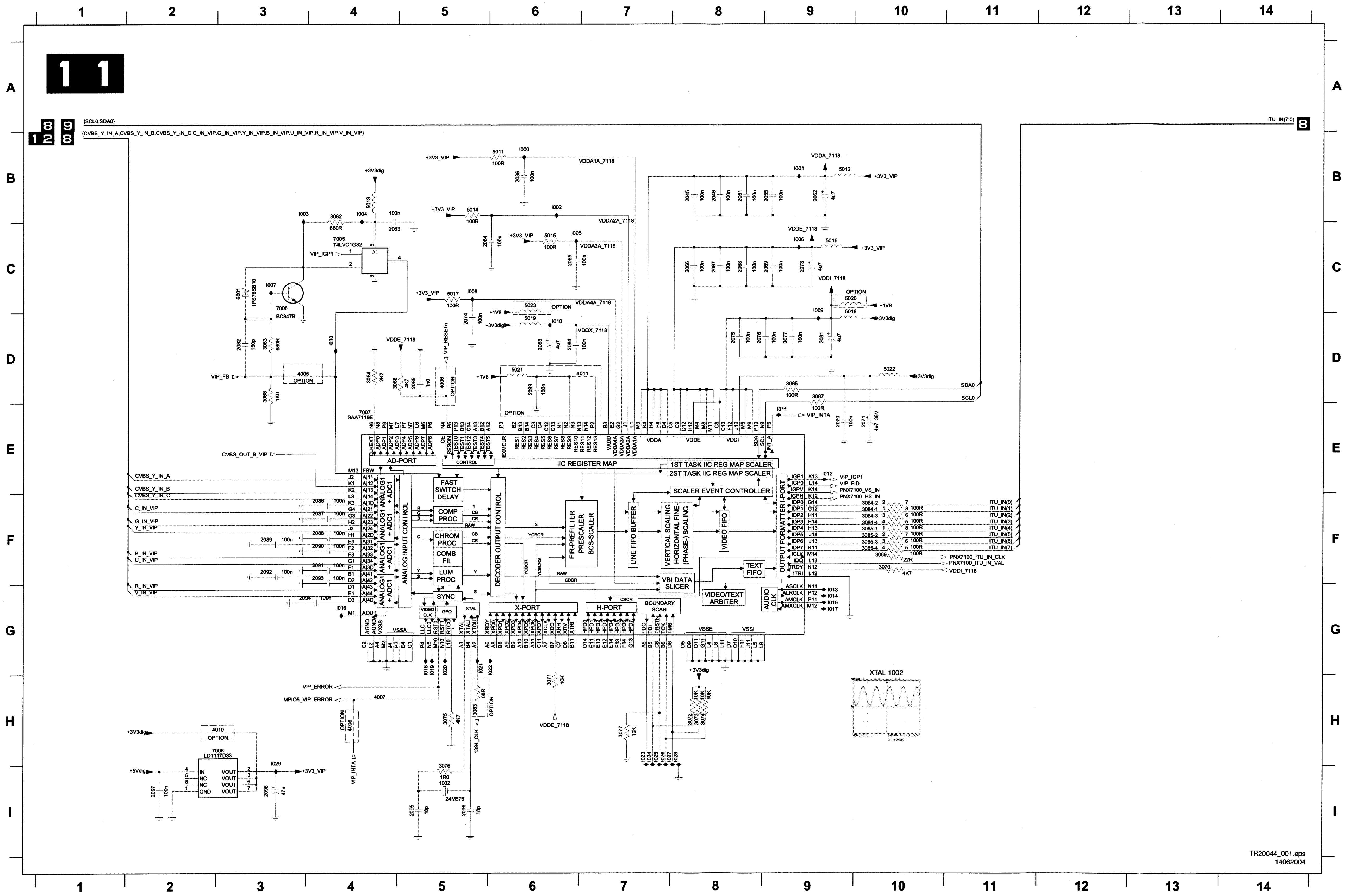
1921	F12
2900	C5
2901	C9
2902	C10
2903	C12
2904	C13
2905	C9
2906	C10
2907	C12
2908	C13
2909	C9
2910	C10
2911	C12
2912	C13
2913	C10
2914	C13
2915	E8
2916	E11
2917	E3
2918	G3
2921	G10
3903-1	D4
3903-2	D4
3903-3	D4
3903-4	D4
3904-2	D4
3904-3	D4
3904-4	D4
3908	D7
3911	E7
3912	E8
3913	E11
3914	F7
3915	F2
3916	F2
3917	F2
3918	F2
3919	G2
3920	H2
4900	D6
4901	D4
4902	F7
4925	E6
5900	B10
5901	B13
5902	B5
5903	E3
5904	G3
7900	C6
7902	C9
7903	C12
7904	E3
7905	G3
F849	I12
F901	E6
I900	B5
I901	B9
I902	B12
I903	E3
I904	G3
I905	E2

FEBE: BE DV In IEEE1394


1 Ø
PDI1394P25
7000
PDI1394P25
BIAS VOLTAGE AND CURRENT GENERATOR
RECEIVED DATA DECODER/ TIMER
LINK INTERFACE
ARBITR'N AND CONTROL STATE MACHINE LOGIC
XTAL OSC. PLL CLOCK
TRANSMIT DATA ENCODER
AVDD
TESTM
DVDD
PLLVDD
AGND
DGND
PLLGND
PHY
+3V3_IEEE_A
+3V3_IEEE_D
+3V3_IEEE_PLL
+3V3_LINK
+3V3dig
1000
1001
CX-11F
24M576
1394_CLK
4009
OPTION
RESET_1394n
MPIO8_1394_CNA
MPIO21_1394_POWERDOWN
MPIO2_1394_IRQn
LINK
7001
PDI1394L40
VDD
GND
LINK CORE
12KB BUFFER MEMORY
ISOCH & ASYNC PACKETS
TRANSMITTER / RECEIVER AV1
TRANSMITTER / RECEIVER AV2
CONTROL AND STATUS REGISTERS
ASYNC TRANSMITTER AND RECEIVER
8-BIT INTERFACE
RESERVED
TESTPIN
L_D(7:0)
L_D_CTL
MX_D(7:0)
MX_D_CTL
PCI_AD(31:0)
L_CLK
L_FSYNC
L_VAL
L_SYNC
MX_CLK
MX_VAL
MX_SYNC
XIO_SEL1
PCI_CBE(1)
PCI_CBE(2)
F029 IC7000 pin 60
OPTIONAL FOR 3104 128 0927
TR20043_001.eps
14062004

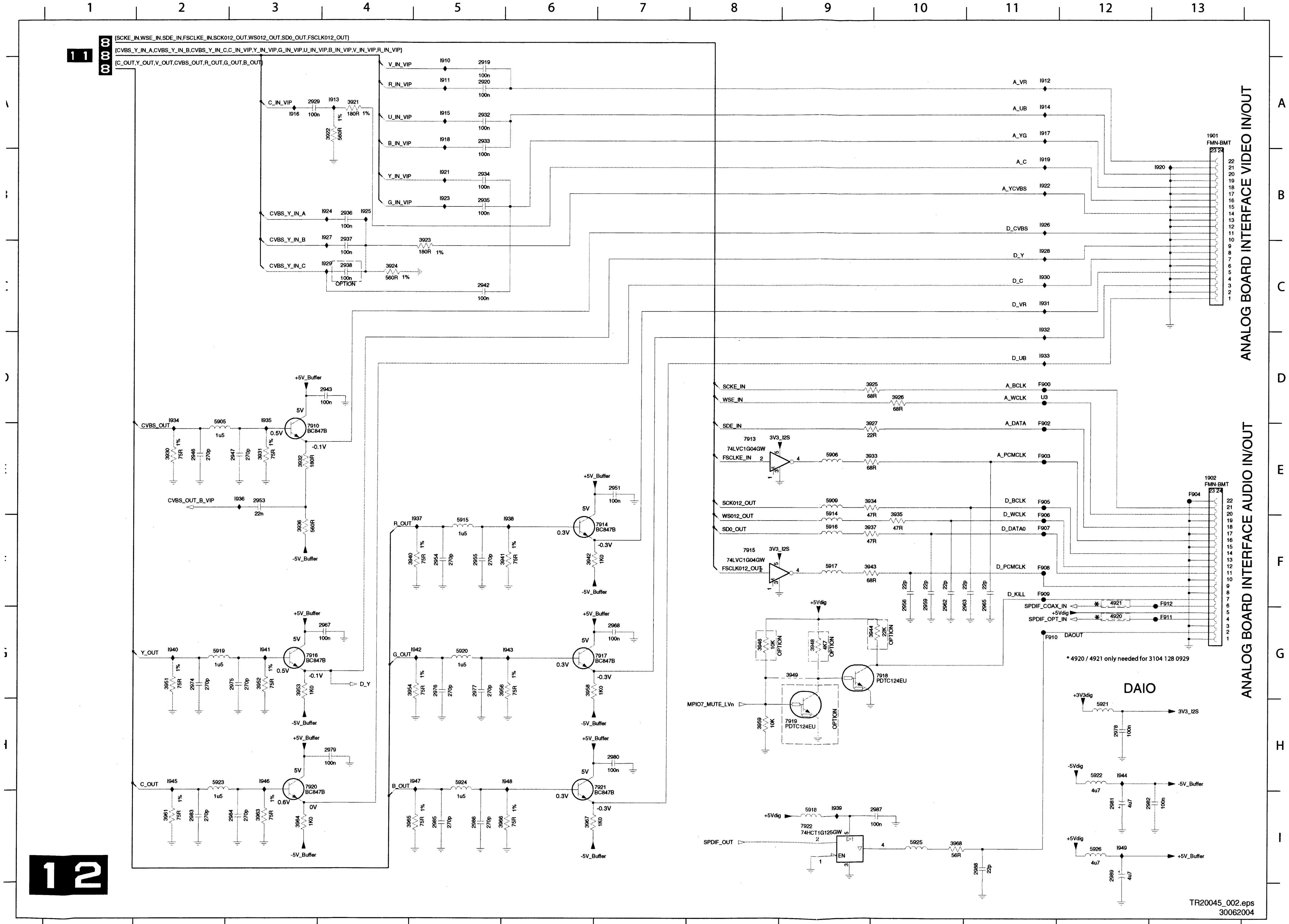
1000 C1	3046 D13
1001 E1	3047 D13
2000 A5	3048 E12
2001 B8	3049 E12
2002 B6	3050 F12
2003 B2	3051 E12
2004 D1	3052 F12
2005 E1	3053 F12
2006 E1	3054 F12
2007 E2	3055 F12
2008 E2	3056 F11
2009 G2	3057 G12
2010 H2	3058 G12
2011 H2	3059 G12
2012 H2	3060 H8
2013 H3	4000 A4
2014 I1	4001 E6
2015 I2	4002 E6
2016 I2	4003 G12
2017 I4	4004 H12
2018 I5	4009 D1
2019 I5	5000 G1
2020 I5	5001 G1
2021 I6	5002 H1
2022 I6	7000 B5
2023 I6	7001 C11
2024 I6	F000 B8
2025 I7	F001 B3
2026 I7	F002 B5
2027 I7	F003 B3
2028 I8	F004 B3
2029 I8	F005 B5
2030 I8	F006 C1
2031 I8	F007 C7
2032 I9	F008 C1
2033 I9	F009 C12
2034 I9	F010 C1
3000-1 C12	F011 C7
3000-2 C12	F012 C12
3000-3 C12	F013 C12
3000-4 C12	F014 C1
3001-1 D12	F015 C7
3001-2 D12	F016 C12
3001-3 D12	F017 C1
3001-4 C12	F018 C12
3002 D12	F019 C7
3003-1 E12	F020 D12
3003-2 E12	F021 D12
3003-3 E12	F022 D7
3003-4 E12	F023 D12
3004-1 E12	F024 D12
3004-2 E12	F025 D7
3004-3 E12	F026 D12
3004-4 E12	F027 D12
3005-1 F12	F028 D7
3005-2 G12	F029 D2
3005-3 G12	F030 D12
3005-4 G12	F031 D12
3006-1 G12	F032 D7
3006-2 G12	F033 D8
3006-3 G12	F034 D12
3006-4 G12	F035 D12
3007-1 G8	F036 E5
3007-2 G8	F037 E5
3007-3 G8	F038 G2
3007-4 G8	F039 G12
3008-1 G8	F040 G12
3008-2 G8	F041 G12
3008-3 G8	F042 G8
3008-4 G8	F043 H2
3009-1 G8	F044 H10
3009-2 G8	F045 H2
3009-3 G8	F046 I5
3009-4 G8	F047 D1
3010-1 G8	
3010-2 F8	
3010-3 F8	
3010-4 F8	
3011 G12	
3012 H13	
3013 D1	
3014 D2	
3015 D2	
3016 E2	
3017 F3	
3018 B2	
3019 B2	
3020 C2	
3021 C2	
3022 B5	
3023 C6	
3024 C7	
3025-1 C6	
3025-2 C7	
3025-3 C6	
3025-4 C7	
3026 D12	
3027 D12	
3028 D12	
3029-1 D6	
3029-2 D7	
3029-3 D6	
3029-4 D7	
3030 D6	
3034 D7	
3035 D6	
3036 B7	
3037 B7	
3038 B7	
3039 B7	
3040 B8	
3041 B7	
3042 B7	
3043 B8	
3044 E5	
3045 D12	

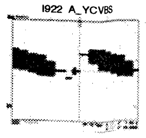
FEBE: BE Video In Processing (VIP)


11
{SCL0,SDA0}
{CVBS_Y_IN_A,CVBS_Y_IN_B,CVBS_Y_IN_C,C_IN_VIP,G_IN_VIP,Y_IN_VIP,B_IN_VIP,U_IN_VIP,R_IN_VIP,V_IN_VIP}
ITU_IN(7:0)
+3V3_VIP
VDDA1A_7118
VDDA2A_7118
VDDA3A_7118
VDDA4A_7118
VDDX_7118
VDDA_7118
VDDE_7118
VDDI_7118
+3V3dig
+1V8
7005 74LVC1G32
VIP_IGP1
7006 BC847B
VIP_FB
4005 OPTION
7007 SAA7118E
VIP_RESETn
CVBS_OUT_B_VIP
CVBS_Y_IN_A
CVBS_Y_IN_B
CVBS_Y_IN_C
C_IN_VIP
G_IN_VIP
Y_IN_VIP
B_IN_VIP
U_IN_VIP
R_IN_VIP
V_IN_VIP
AD-PORT
CONTROL
IIC REGISTER MAP
1ST TASK IIC REG MAP SCALER
2ST TASK IIC REG MAP SCALER
SCALER EVENT CONTROLLER
ANALOG INPUT CONTROL
FAST SWITCH DELAY
COMP PROC
CHROM PROC
COMB FIL
LUM PROC
SYNC
DECODER OUTPUT CONTROL
FIR-PREFILTER PRESCALER BCS-SCALER
LINE FIFO BUFFER
VERTICAL SCALING HORIZONTAL FINE-(PHASE-) SCALING
VIDEO FIFO
TEXT FIFO
VBI DATA SLICER
VIDEO/TEXT ARBITER
AUDIO CLK
OUTPUT FORMATTER I-PORT
X-PORT
H-PORT
BOUNDARY SCAN
VIDEO CLK
GPO
XTAL
ANALOG1 + ADC1
VSSA
VSSE
VSSI
VDDA
VDDE
VDDI
SDA0
SCL0
VIP_INTA
VIP_IGP1
VIP_FID
PNX7100_VS_IN
PNX7100_HS_IN
PNX7100_ITU_IN_CLK
PNX7100_ITU_IN_VAL
VDDI_7118
VIP_ERROR
MPIO5_VIP_ERROR
4007
4008 OPTION
VIP_INTA
1394_CLK
VDDE_7118
+3V3dig
4010 OPTION
7008 LD1117D33
+5Vdig
IN
NC
GND
VOUT
+3V3_VIP
1002 24M576
XTAL 1002
TR20044_001.eps
14062004

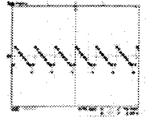
Ref.	Location
1002	I5
2036	B6
2045	B8
2046	B8
2051	B8
2055	B9
2062	B9
2063	C4
2064	C5
2065	C6
2066	C8
2067	C8
2068	C8
2069	C9
2070	E9
2071	E10
2073	C9
2074	D5
2075	D8
2076	D8
2077	D9
2081	D9
2082	D3
2083	D6
2084	D6
2085	D5
2086	F4
2087	F4
2088	F4
2089	F3
2090	F4
2091	F4
2092	F3
2093	F4
2094	G3
2095	I5
2096	I5
2097	I2
2098	I3
2099	D6
3062	B4
3063	D3
3064	D4
3065	D9
3066	D4
3067	D9
3068	D3
3069	F10
3070	F10
3071	H6
3072	H8
3073	H8
3074	H8
3075	H5
3076	I5
3077	H7
3083	H5
3084-1	F10
3084-2	F10
3084-3	F10
3084-4	F10
3085-1	F10
3085-2	F10
3085-3	F10
3085-4	F10
4005	D3
4006	D5
4007	H4
4008	H4
4010	H3
4011	D7
5011	B6
5012	B9
5013	B4
5014	B5
5015	C6
5016	C9
5017	C5
5018	D9
5019	D6
5020	C9
5021	D6
5022	D10
5023	C6
6001	C3
7005	C4
7006	C3
7007	E4
7008	H3
I000	B6
I001	B9
I002	B6
I003	B3
I004	B4
I005	C6
I006	C9
I007	C3
I008	C5
I009	C9
I010	D6
I011	E9
I012	E9
I013	G9
I014	G9
I015	G9
I016	G4
I017	G9
I018	G5
I019	G5
I020	G5
I021	G5
I022	G6
I023	H7
I024	H7
I025	H7
I026	H7
I027	H7
I028	H8
I029	H3
I030	D4

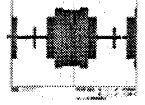
FEBE: BE Audio & Video In/Out

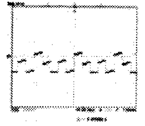

1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H I
11
12
[SCKE_IN,WSE_IN,SDE_IN,FSCLKE_IN,SCK012_OUT,WS012_OUT,SD0_OUT,FSCLK012_OUT]
[CVBS_Y_IN_A,CVBS_Y_IN_B,CVBS_Y_IN_C,C_IN_VIP,Y_IN_VIP,G_IN_VIP,U_IN_VIP,B_IN_VIP,V_IN_VIP,R_IN_VIP]
[C_OUT,Y_OUT,V_OUT,CVBS_OUT,R_OUT,G_OUT,B_OUT]
V_IN_VIP
R_IN_VIP
C_IN_VIP
U_IN_VIP
B_IN_VIP
Y_IN_VIP
G_IN_VIP
CVBS_Y_IN_A
CVBS_Y_IN_B
CVBS_Y_IN_C
OPTION
A_VR
A_UB
A_YG
A_C
A_YCVBS
D_CVBS
D_Y
D_C
D_VR
D_UB
1901
FMN-BMT
1902
FMN-BMT
ANALOG BOARD INTERFACE VIDEO IN/OUT
ANALOG BOARD INTERFACE AUDIO IN/OUT
SCKE_IN
WSE_IN
SDE_IN
FSCLKE_IN
SCK012_OUT
WS012_OUT
SD0_OUT
FSCLK012_OUT
74LVC1G04GW
3V3_I2S
A_BCLK
A_WCLK
A_DATA
A_PCMCLK
D_BCLK
D_WCLK
D_DATA0
D_PCMCLK
D_KILL
SPDIF_COAX_IN
+5Vdig
SPDIF_OPT_IN
DAOUT
* 4920 / 4921 only needed for 3104 128 0929
MPIO7_MUTE_LVn
7918
PDTC124EU
7919
PDTC124EU
DAIO
+3V3dig
-5Vdig
-5V_Buffer
+5V_Buffer
SPDIF_OUT
7922
74HCT1G125GW
EN
CVBS_OUT
CVBS_OUT_B_VIP
7910
BC847B
Y_OUT
7916
BC847B
D_Y
C_OUT
7920
BC847B
R_OUT
7914
BC847B
G_OUT
7917
BC847B
B_OUT
7921
BC847B
TR20045_002.eps
30062004

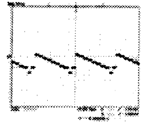

I922 A_YCVBS

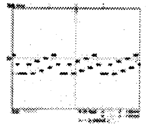
I926 D_CVBS

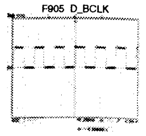

I928 D_Y

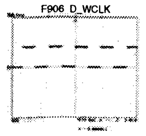

I930 D_C

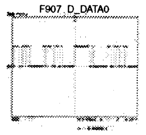

I931 D_VR

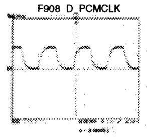

I932 D_YG


I933 D_UB


F905 D_BCLK

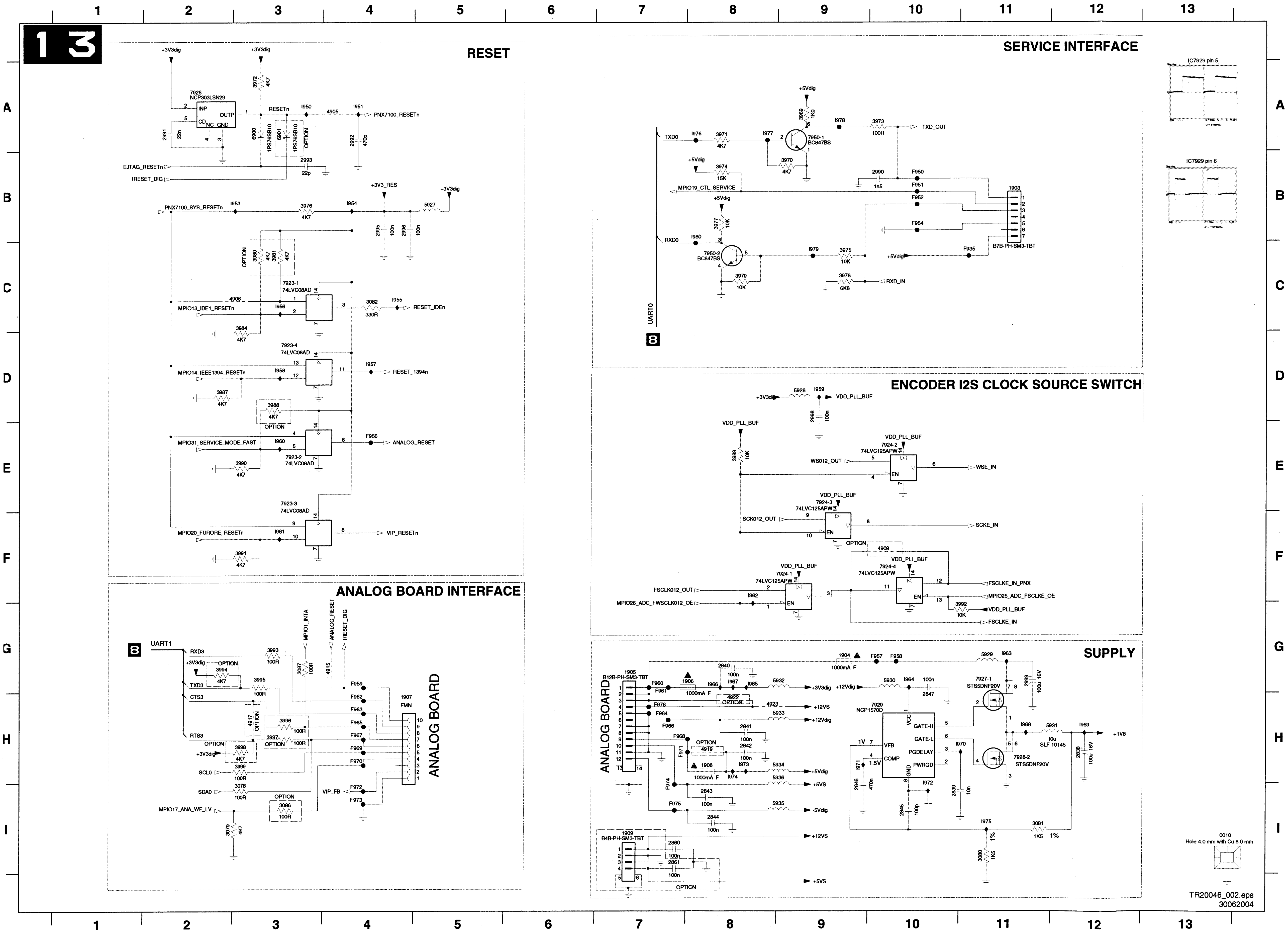

F906 D_WCLK


F907 D_DATA0


F908 D_PCMCLK

U3	D11
1901	A13
1902	E13
2919	A5
2920	A5
2929	A3
2932	A5
2933	A5
2934	B5
2935	B5
2936	B4
2937	C4
2938	C4
2942	C5
2943	D4
2946	E2
2947	E3
2951	E7
2953	E3
2954	F5
2955	F5
2956	F10
2959	F10
2962	F10
2963	F11
2965	F11
2967	G4
2968	G7
2974	G2
2975	G3
2976	G5
2977	G5
2978	H12
2979	H4
2980	H7
2981	I12
2982	I13
2983	I2
2984	I3
2985	I5
2986	I5
2987	I10
2988	I11
2989	I12
3921	A4
3922	A4
3923	C5
3924	C4
3925	D9
3926	D10
3927	E9
3930	E2
3931	E3
3932	E3
3933	E9
3934	E9
3935	F10
3936	F3
3937	F9
3940	F5
3941	F6
3942	F6
3943	F9
3944	G10
3946	G8
3948	G9
3949	G9
3951	G2
3952	G3
3953	G3
3954	G5
3956	G6
3958	G6
3959	H8
3961	I2
3963	I3
3964	I3
3965	I5
3966	I6
3967	I6
3968	I10
4920	G12
4921	F12
5905	E2
5906	E9
5909	E9
5914	F9
5915	F5
5916	F9
5917	F9
5918	I9
5919	G2
5920	G5
5921	H12
5922	H12
5923	H2
5924	H5
5925	I10
5926	I12
7910	E3
7913	E8
7914	F7
7915	F8
7916	G3
7917	G7
7918	G10
7919	H9
7920	H3
7921	H7
7922	I9
F900	D11
F902	E11
F903	E11
F904	E13
F905	E11
F906	F11
F907	F11
F908	F11
F909	F11
F910	G11
F911	G13
F912	F13
I910	A5
I911	A5
I912	A11
I913	A4
I914	A11
I915	A5
I916	A3
I917	A11
I918	A5
I919	B11
I920	B13
I921	B5
I922	B11
I923	B5
I924	B4
I925	B4
I926	B11
I927	B4
I928	C11
I929	C4
I930	C11
I931	C11
I932	C11
I933	D11
I934	D2
I935	D3
I936	E3
I937	F5
I938	F6
I939	I9
I940	G2
I941	G3
I942	G5
I943	G6
I944	H12
I945	H2
I946	H3
I947	H5
I948	H6
I949	I12

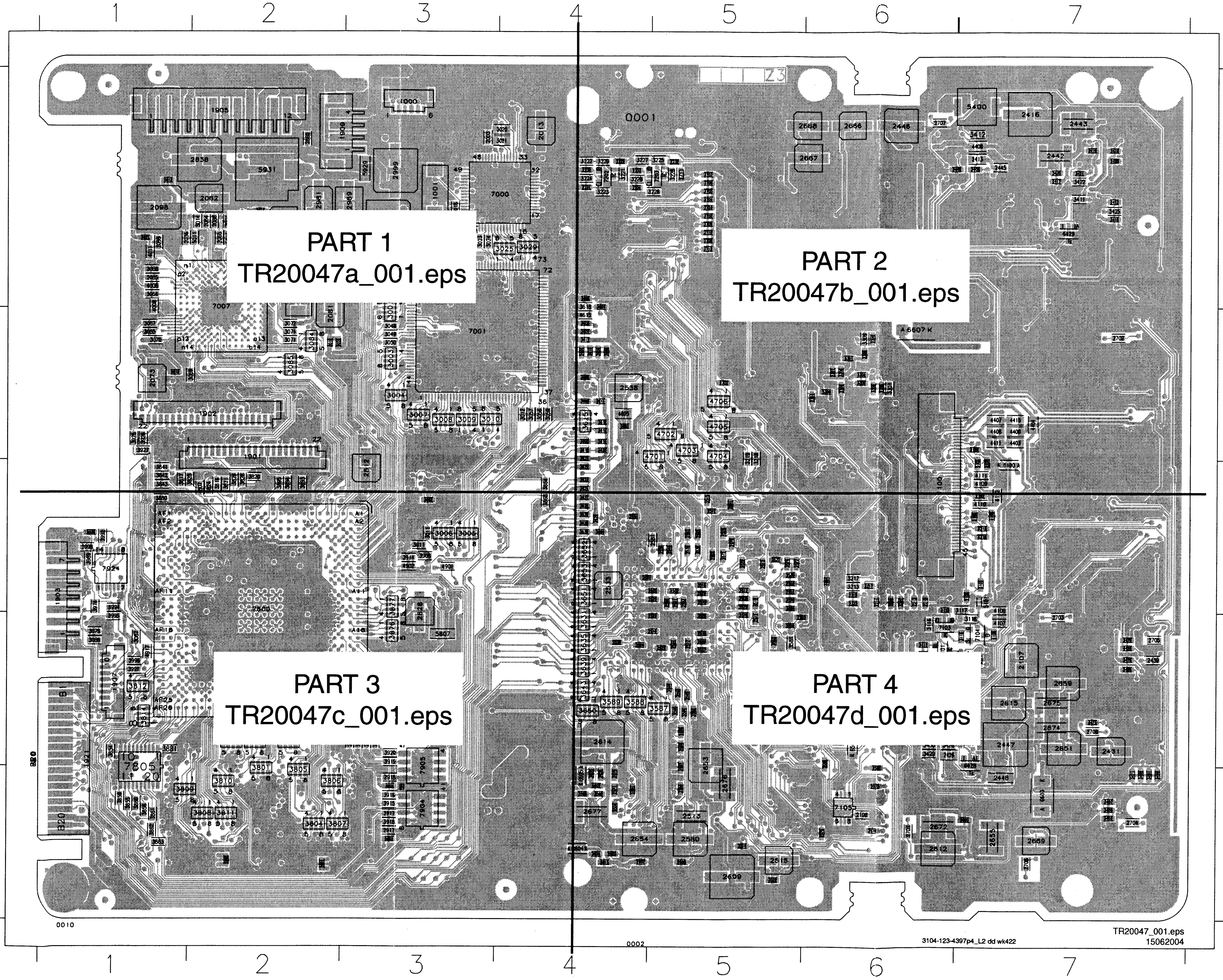
FEBE: BE Supply, Reset, UART, Encorder I2S Clock Source Switch


13
RESET
SERVICE INTERFACE
ENCODER I2S CLOCK SOURCE SWITCH
ANALOG BOARD INTERFACE
SUPPLY
ANALOG BOARD
UART0
UART1
IC7929 pin 5
IC7929 pin 6
7926 NCP303LSN29
PNX7100_RESETn
EJTAG_RESETn
IRESET_DIG
PNX7100_SYS_RESETn
+3V3_RES
+3V3dig
7923-1 74LVC08AD
MPIO13_IDE1_RESETn
RESET_IDEn
7923-4 74LVC08AD
MPIO14_IEEE1394_RESETn
RESET_1394n
MPIO31_SERVICE_MODE_FAST
ANALOG_RESET
7923-2 74LVC08AD
7923-3 74LVC08AD
MPIO20_FURORE_RESETn
VIP_RESETn
TXD0
RXD0
TXD_OUT
RXD_IN
MPIO19_CTL_SERVICE
7950-1 BC847BS
7950-2 BC847BS
1903 B7B-PH-SM3-TBT
+5Vdig
VDD_PLL_BUF
WS012_OUT
WSE_IN
SCK012_OUT
SCKE_IN
FSCLK012_OUT
MPIO26_ADC_FWSCLK012_OE
FSCLKE_IN_PNX
MPIO25_ADC_FSCLKE_OE
FSCLKE_IN
7924-1 74LVC125APW
7924-2 74LVC125APW
7924-3 74LVC125APW
7924-4 74LVC125APW
RXD3
TXD3
CTS3
RTS3
SCL0
SDA0
MPIO17_ANA_WE_LV
MPIO1_INTA
ANALOG_RESET
IRESET_DIG
VIP_FB
1907 FMN
1905 B12B-PH-SM3-TBT
1909 B4B-PH-SM3-TBT
+3V3dig
+12VS
+12Vdig
+5Vdig
+5VS
-5Vdig
+1V8
7929 NCP1570D
7927-1 STS5DNF20V
7928-2 STS5DNF20V
GATE-H
GATE-L
PGDELAY
PWRGD
VFB
COMP
VCC
GND
SLF 10145
OPTION
0010
Hole 4.0 mm with Cu 8.0 mm

TR20046_002.eps
30062004

0010	I13
1903	B11
1904	G9
1905	G7
1906	G8
1907	H4
1908	H8
1909	I7
2838	H12
2839	I10
2840	G8
2841	H8
2842	H8
2843	I8
2844	I8
2845	I10
2846	I9
2847	H10
2860	I7
2861	I7
2990	B10
2991	A2
2992	A4
2993	B3
2995	B4
2996	B4
2998	D9
2999	G11
3078	I3
3079	I2
3080	I11
3081	I11
3082	C4
3086	I3
3087	G3
3969	A9
3970	B9
3971	A8
3972	A3
3973	A10
3974	B8
3975	C9
3976	B3
3977	B8
3978	C9
3979	C8
3980	C3
3981	C3
3984	C3
3987	D2
3988	D3
3989	E8
3990	E3
3991	F3
3992	G11
3993	G3
3994	G2
3995	G3
3996	H3
3997	H3
3998	H3
3999	H3
4905	A4
4906	C3
4909	F10
4915	G4
4917	H3
4919	H8
4922	H8
4923	H8
5927	B5
5928	D9
5929	G11
5930	G10
5931	H12
5932	G9
5933	H9
5934	H9
5935	I9
5936	H9
6900	A3
6901	A3
7923-1	C3
7923-2	E3
7923-3	E3
7923-4	D3
7924-1	F9
7924-2	E10
7924-3	E9
7924-4	F10
7926	A2
7927-1	G11
7928-2	H11
7929	H10
7950-1	A9
7950-2	C8
F935	C11
F950	B10
F951	B10
F952	B10
F954	B10
F956	E4
F957	G10
F958	G10
F959	G4
F960	G7
F961	H7
F962	H4
F963	H4
F964	H7
F965	H4
F966	H7
F967	H4
F968	H7
F969	H4
F970	H4
F971	H7
F972	I4
F973	I4
F974	I7
F975	I7
F976	H7
I950	A3
I951	A4
I953	B3
I954	B4
I955	C4
I956	C3
I957	D4
I958	D3
I959	D9
I960	E3
I961	F3
I962	F8
I963	G11
I964	G10
I965	G8
I966	G8
I967	G8
I968	H11
I969	H12
I970	H11
I971	H9
I972	I10
I973	H8
I974	H8
I975	I11
I976	A8
I977	A8
I978	A9
I979	C9
I980	B8

Layout: FEBE Top View



1000	A3
1001	A3
1002	A2
1100	C6
1901	B2
1902	B2
1903	C1
1905	A2
1907	D1
1909	A2
2003	A3
2013	A4
2014	A3
2036	A1
2062	A2
2064	A2
2065	A2
2071	A2
2073	B1
2074	A2
2081	B2
2083	A2
2084	A2
2085	A1
2088	A2
2090	A2
2091	A2
2092	A2
2093	A2
2098	A1
2099	A1
2100	C7
2102	C7
2103	C7
2104	B7
2105	C7
2106	D6
2107	D7
2108	E6
2211	C6
2212	C6
2217	C6
2218	C6
2219	C6
2223	C6
2229	A4
2230	A4
2231	A4
2232	A5
2233	A4
2234	A4
2300	B6
2301	B6
2306	B6
2307	B6
2309	B6
2310	B6
2405	A7
2407	E7
2412	A7
2413	A7
2416	A7
2417	A7
2418	A7
2419	A7
2420	A7
2426	D6
2427	D7
2431	D7
2439	D7
2440	A6
2442	A7
2443	A7
2445	A7
2446	A6
2447	D7
2448	E7
2500	C5
2501	C5
2502	C5
2503	D5
2509	C5
2511	D5
2512	C5
2513	E5
2514	E5
2515	E5
2516	D5
2517	D5
2518	D5
2519	C5
2520	C5
2521	C4
2522	C5
2523	D5
2524	D4
2525	D5
2526	D5
2527	D5
2528	D5
2529	C5
2530	D4
2531	D5
2533	C4
2534	C4
2536	C5
2538	B4
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2552	C5
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2563	D5
2564	D5
2565	D5
2566	D5
2567	E5
2568	E5
2569	E5
2570	E4
2571	E4
2573	E6
2574	E6
2575	E6
2576	D6
2577	C5
2578	C5
2579	C5
2580	E5
2581	C5
2582	C5
2583	C5
2584	D6
2585	D6
2586	D6
2604	B4
2605	D6
2607	E4
2609	E5
2612	E6
2614	D4
2615	D7
2623	E4
2624	E4
2625	E4
2626	E4
2651	D7
2653	D5
2654	E4
2655	E7
2659	D7
2666	A6
2667	A6
2668	A6
2669	E7
2672	E6
2674	D7
2675	D7
2676	E5
2677	E4
2700	D7
2701	E6
2702	B7
2703	D7
2704	E7
2705	D7
2706	E7
2707	A6
2801	D3
2802	D3
2803	D3
2804	D3
2807	D3
2809	D3
2812	C3
2818	D3
2828	C3
2838	A2
2860	A2
2917	E3
2918	E3
2981	A2
2989	A3
2998	C1
2999	A3
3000	A3
3001	B3
3002	A3
3003	B3
3004	B3
3005	C3
3006	C3
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3011	C3
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3059	B4
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3066	A1
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3069	B2
3070	B1
3071	B2
3072	B2
3074	B2
3076	A2
3079	D1
3082	C3
3083	A2
3084	B2
3085	B2
3086	D1
3087	D1
3104	C7
3108	D6
3110	D6
3111	D7
3112	D6
3113	D6
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3116	D7
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3118	C6
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3217	C6
3218	B5
3219	B5
3220	A4
3221	A4
3222	A4
3223	A4
3224	A4
3225	A5
3226	A5
3227	A4
3228	A5
3229	A4
3301	B6
3304	B6
3305	B6
3306	B6
3308	B6
3309	B6
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3490	E7
3491	E7
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3504	C5
3515	C5
3516	C5
3517	C5
3518	D5
3519	C5
3520	C5
3522	E5
3524	D5
3527	C5
3529	C5
3530	C5
3534	D5
3535	C5
3536	C5
3547	C5
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3551	C5
3561	D6
3574	C5
3577	C5
3578	D5
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3612	B4
3613	B4
3614	B4
3615	B4
3617	B4
3618	A4
3619	B4
3620	B4
3621	B4
3622	C4
3623	C4
3624	C4
3625	C4
3626	C4
3627	C4
3628	C4
3629	C4
3630	C4
3631	D4
3635	D4
3639	D4
3643	D4
3650	D4
3651	C4
3652	C4
3653	C4
3684	C4
3689	B4
3690	B4
3702	A5
3703	A5
3704	A5
3705	A5
3706	A5
3707	A5
3708	A5
3709	A5
3710	A5
3711	A5
3712	A5
3800	D2
3801	E2
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3829	C2
3841	C1
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3843	C1
3853	D3
3854	D1
3855	E1
3856	E1
3859	E1
3860	E1
3861	E1
3862	E1
3863	E1
3864	C4
3865	B4
3867	D3
3868	C4
3873	D3
3876	D3
3877	C3
3880	C1
3881	D1
3893	C2
3894	C2
3895	C2
3908	C3
3911	C3
3914	C3
3915	E3
3916	E3
3917	E3
3918	E3
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3926	B1
3927	B1
3974	C1
3989	C1
3992	C1
3994	C1
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3996	D1
3997	D1
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4011	A1
4100	C7
4106	D7
4107	D7
4108	C7
4109	C7
4110	C7
4111	C7
4112	C7
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4403	B7
4404	B7
4406	B7
4407	B7
4408	A7
4410	B7
4411	B7
4422	D7
4502	C5
4503	D6
4504	D6
4519	D5
4520	D6
4525	C5
4604	C6
4605	B4
4615	B4
4701	B5
4702	B5
4703	B5
4704	B5
4705	B5
4706	B5
4707	B5
4807	C2
4901	C3
4902	C3
4917	D1
5000	A3
5002	A3
5011	A2
5012	A1
5014	A2
5015	A2
5016	B1
5017	A2
5018	B2
5019	A2
5020	B2
5021	A1
5022	A2
5023	A2
5101	C7
5103	C7
5300	B6
5301	B6
5400	A7
5501	D6
5502	D5
5504	E4
5602	B4
5603	E7
5607	E4
5615	E4
5802	D3
5806	D3
5807	D3
5900	E2
5901	E2
5903	E3
5904	E3
5928	C1
5929	A3
5931	A2
6100	C7
6426	D6
6427	D6
6428	D7
6429	A7
6500	D6
6501	D6
6502	D6
6503	D6
6603	E7
6604	E4
6605	E4
6607	B6
6800	D3
7000	A4
7001	B3
7007	A2
7101	D6
7102	D7
7103	D6
7104	D7
7105	E6
7202	A4
7203	A5
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7506	D6
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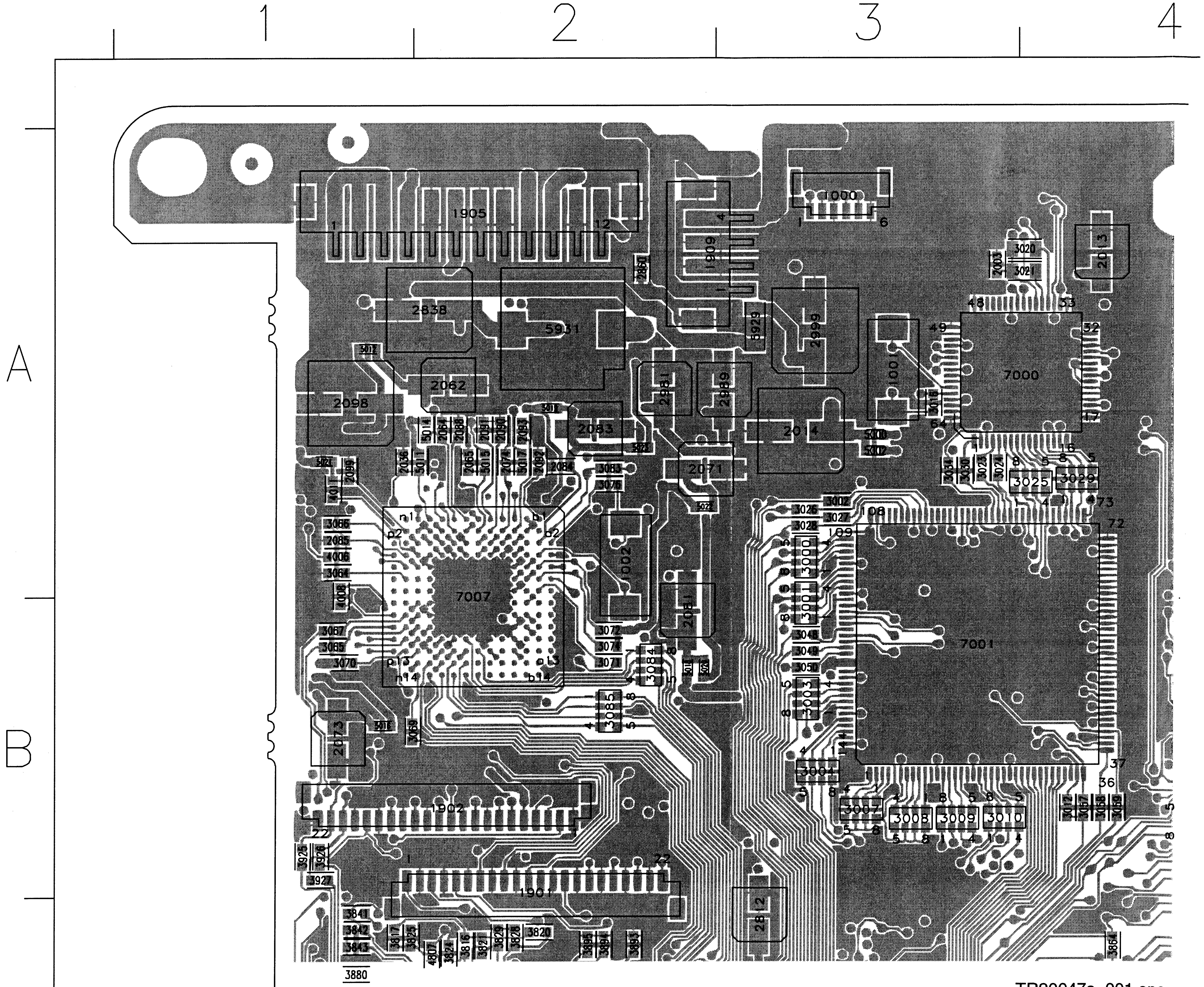
Layout: FEBE Top View Part 1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2062
2083
2081
2089
2014
2071
7007
1002
2081
7001
3025
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2073
1902
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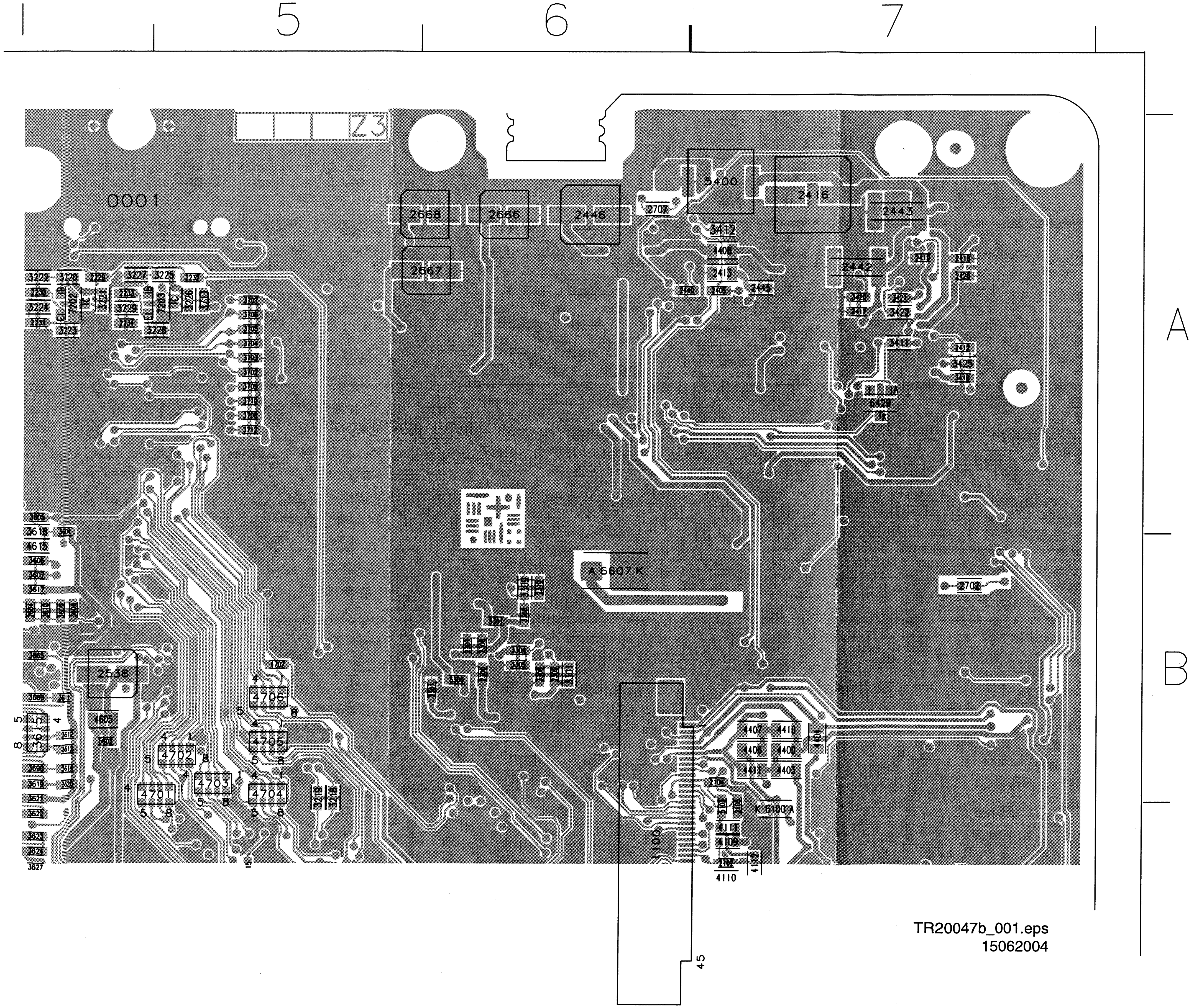
TR20047a_001.eps
15062004

Layout: FEBE Top View Part 2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7203
3221
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3606
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4615
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4605
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4701
4703
4704
4705
4706
4707
3219
3218
A 6607 K
4407
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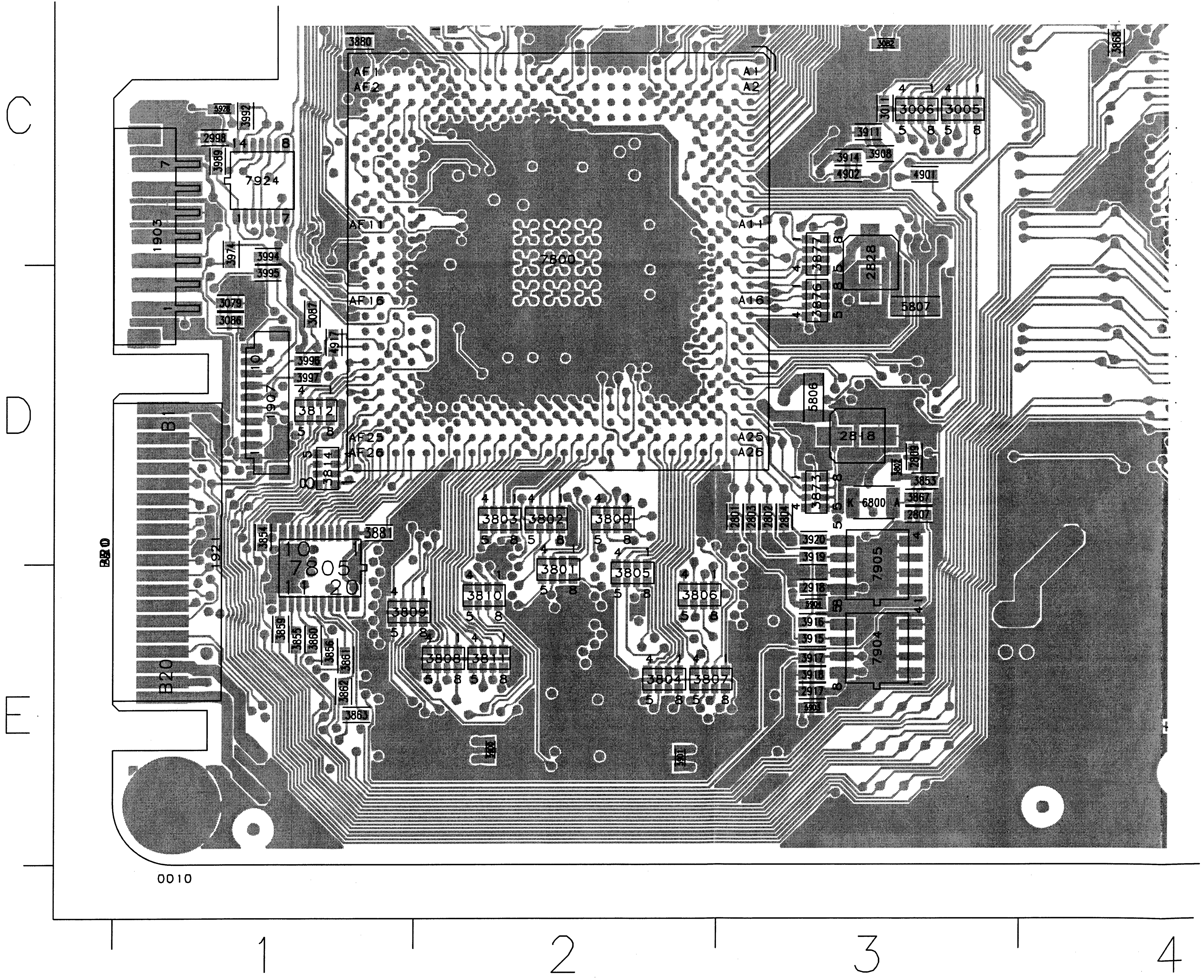
4112
1001
2702
45

TR20047b_001.eps
15062004

Layout: FEBE Top View Part 3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A16
A25
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3868
3006
3005
3011
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3914
3908
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4901
3978
3992
2998
3989
7924
1903
3974
3994
3995
3079
3086
3087
4917
3996
3997
1907
3812
3814
B1
B20
1921
3854
7805
3881
3859
3855
3860
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3863
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3805
3810
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3877
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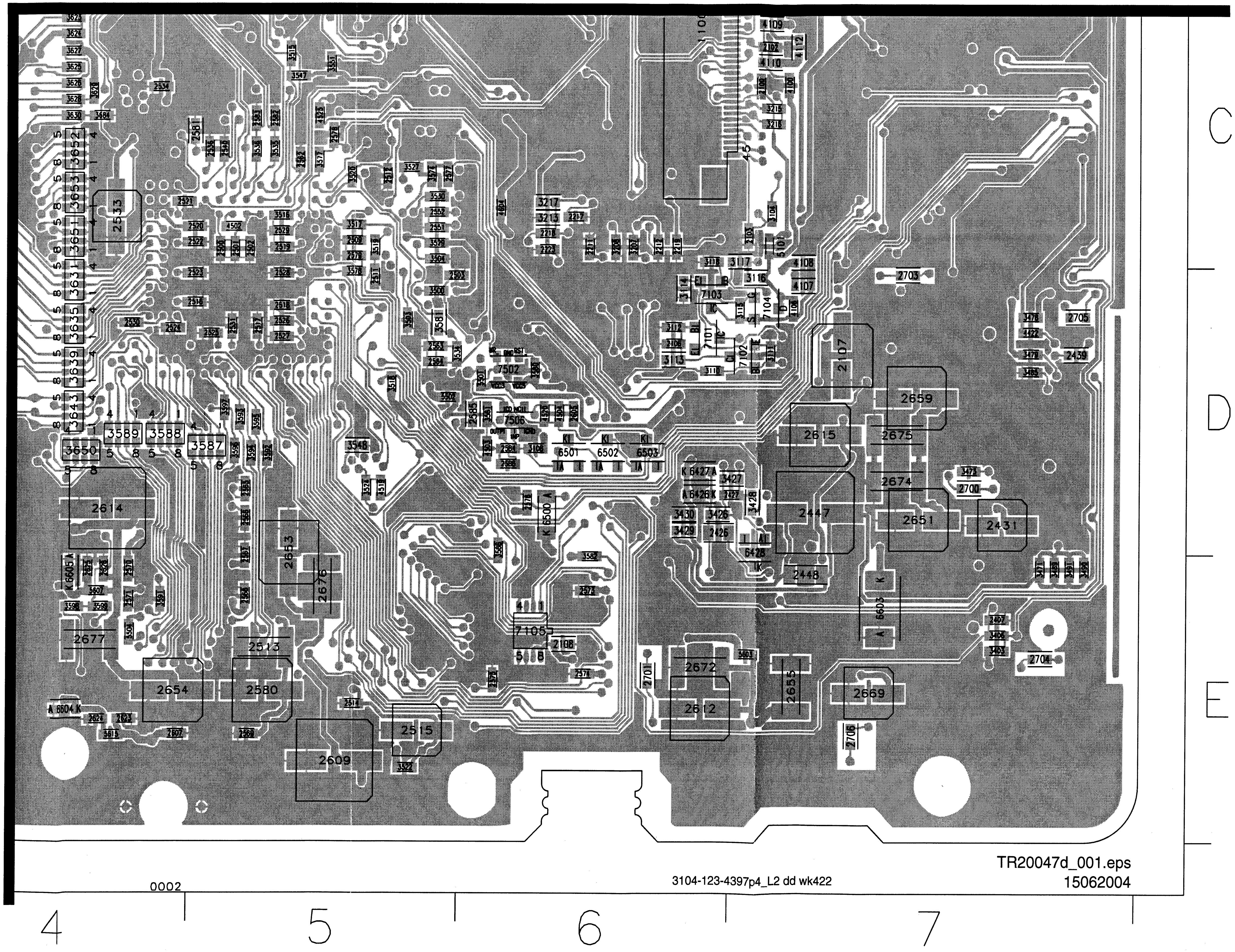
TR20047c_001.eps
30062004

Layout: FEBE Top View Part 4


C
D
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3104-123-4397p4_L2 dd wk422
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7105
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2612
2655
2669
2447
2448
2615
2675
2674
2659
2651
2431
2107
2700
2705
2439
2703
2704
2706
2701
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6502
6503
7502
7506
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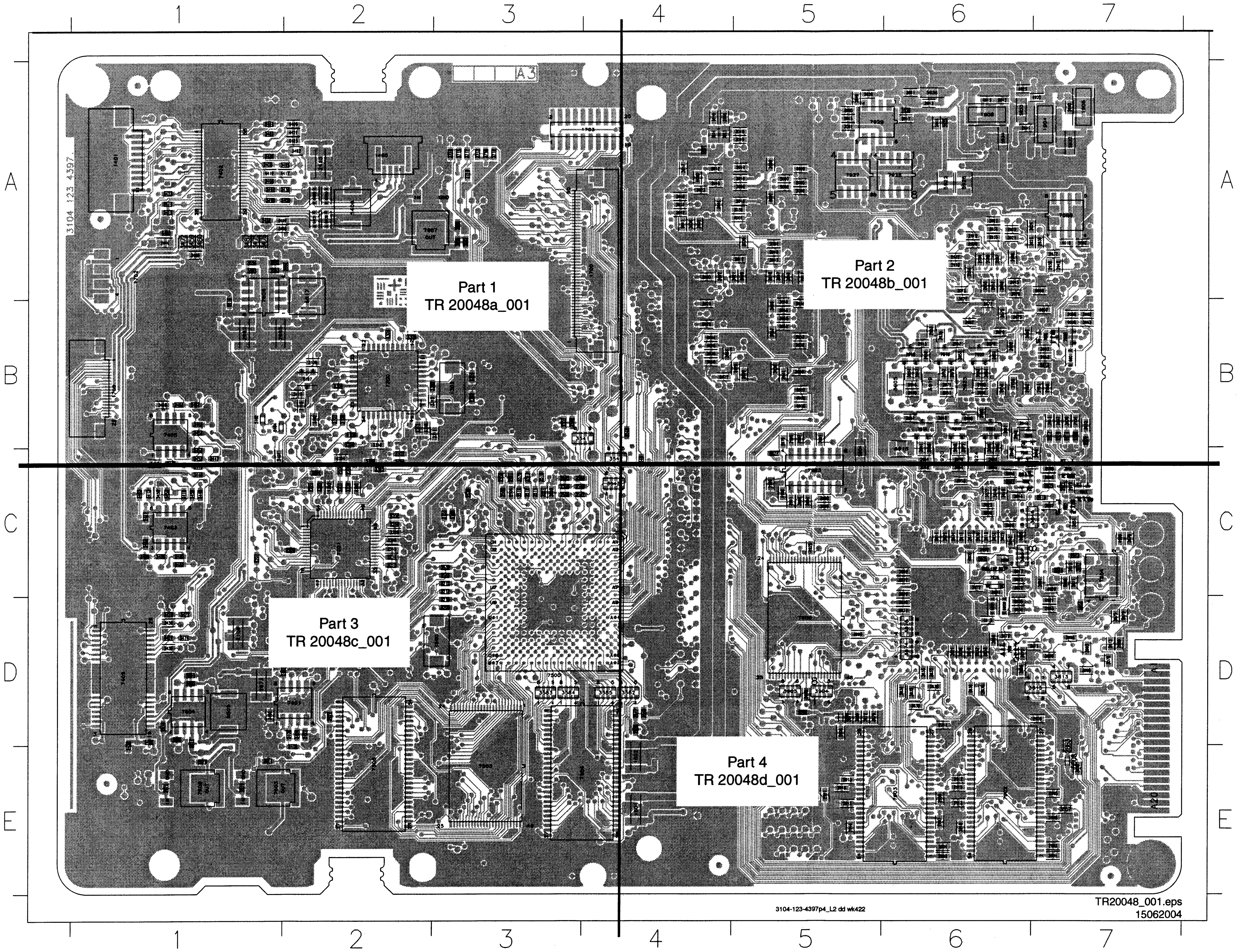
TR20047d_001.eps
15062004

Layout: FEBE Bottom View



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1702	A1
1703	A4
1705	B1
1904	A7
1906	A7
1908	A6
2000	A5
2001	A5
2002	A4
2004	A4
2005	A5
2006	A5
2007	A5
2008	A5
2009	A5
2010	A5
2011	A5
2012	A4
2015	A4
2016	A5
2017	A5
2018	A5
2019	A5
2020	A5
2021	A5
2022	A4
2023	A4
2024	B4
2025	B4
2026	B4
2027	B4
2028	B5
2029	B5
2030	B5
2031	B5
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2033	B5
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2045	A6
2046	A6
2051	A6
2055	A6
2063	B7
2066	A6
2067	B6
2068	B6
2069	A7
2070	B6
2075	B6
2076	A6
2077	B6
2082	B7
2086	A6
2087	A6
2089	A6
2094	A6
2095	A6
2096	A6
2097	A7
2101	C1
2109	D1
2110	B2
2204	C2
2205	C2
2209	C2
2210	C2
2213	C2
2214	C2
2215	C2
2221	C2
2228	C2
2302	B2
2303	B3
2304	B3
2305	B2
2308	C2
2311	B3
2312	B2
2400	A1
2401	D2
2406	D2
2409	A2
2411	A1
2414	A1
2415	A1
2421	D2
2430	E1
2432	A1
2433	A2
2434	D1
2435	D1
2436	A2
2438	A1
2441	C1
2444	A1
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2505	C3
2506	C3
2507	C3
2550	C3
2561	C3
2572	D2
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2611	E1
2618	D1
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2664	A2
2665	B1
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2671	E1
2673	D1
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2806	C6
2808	C7
2810	C7
2811	C7
2813	C6
2814	C6
2815	C6
2816	C6
2817	C6
2819	D6
2820	D6
2821	D6
2822	C6
2823	C6
2824	C6
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2827	C6
2829	C6
2830	D6
2831	D6
2832	D6
2833	D6
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2841	A6
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2845	A5
2846	A5
2847	A6
2861	A6
2862	C7
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2900	D5
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2903	E6
2904	E6
2905	E7
2906	E7
2907	E6
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2915	E6
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2992	C6
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3042	A4
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3078	D7
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3212	C3
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3405	E2
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4005	B7
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4921	D7
4922	A7
4923	A6
4925	C5
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5003	A5
5013	B7
5102	B1
5104	B1
5202	C2
5405	D1
5406	A2
5609	D1
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5617	A2
5800	D5
5801	C6
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5804	C5
5805	C6
5808	E7
5902	D5
5905	B6
5906	B7
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5935	A6
5936	A6
6001	B7
6400	A2
6401	A2
6402	A2
6403	A2
6900	D6
6901	D6
7005	B7
7006	B7
7008	A7
7107	B2
7201	C2
7300	B2
7401	D2
7402	A1
7403	C1
7405	B1
7409	D1
7500	D3
7503	E3
7504	E4
7505	E2
7603	E1
7604	D1
7606	A1
7607	A2
7608	E1
7802	C6
7804	C7
7900	D5
7902	E6
7903	E6
7910	B6
7913	C7
7914	B6
7915	C7
7916	B6
7917	B6
7918	B6
7919	C6
7920	B6
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7929	A5
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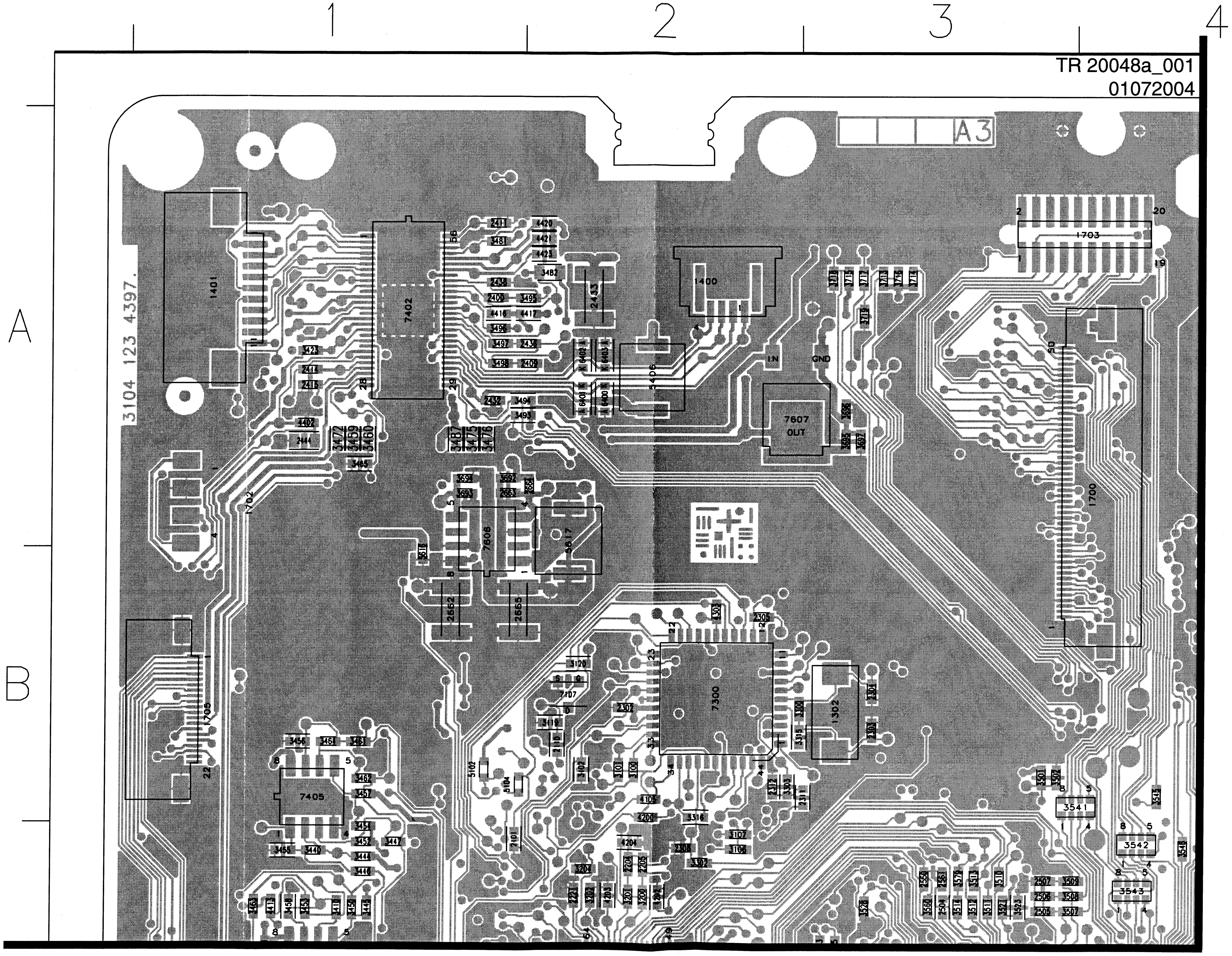
Layout: FEBE Bottom View Part 1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A3
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1400
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1700
5406
7607
OUT
IN
GND
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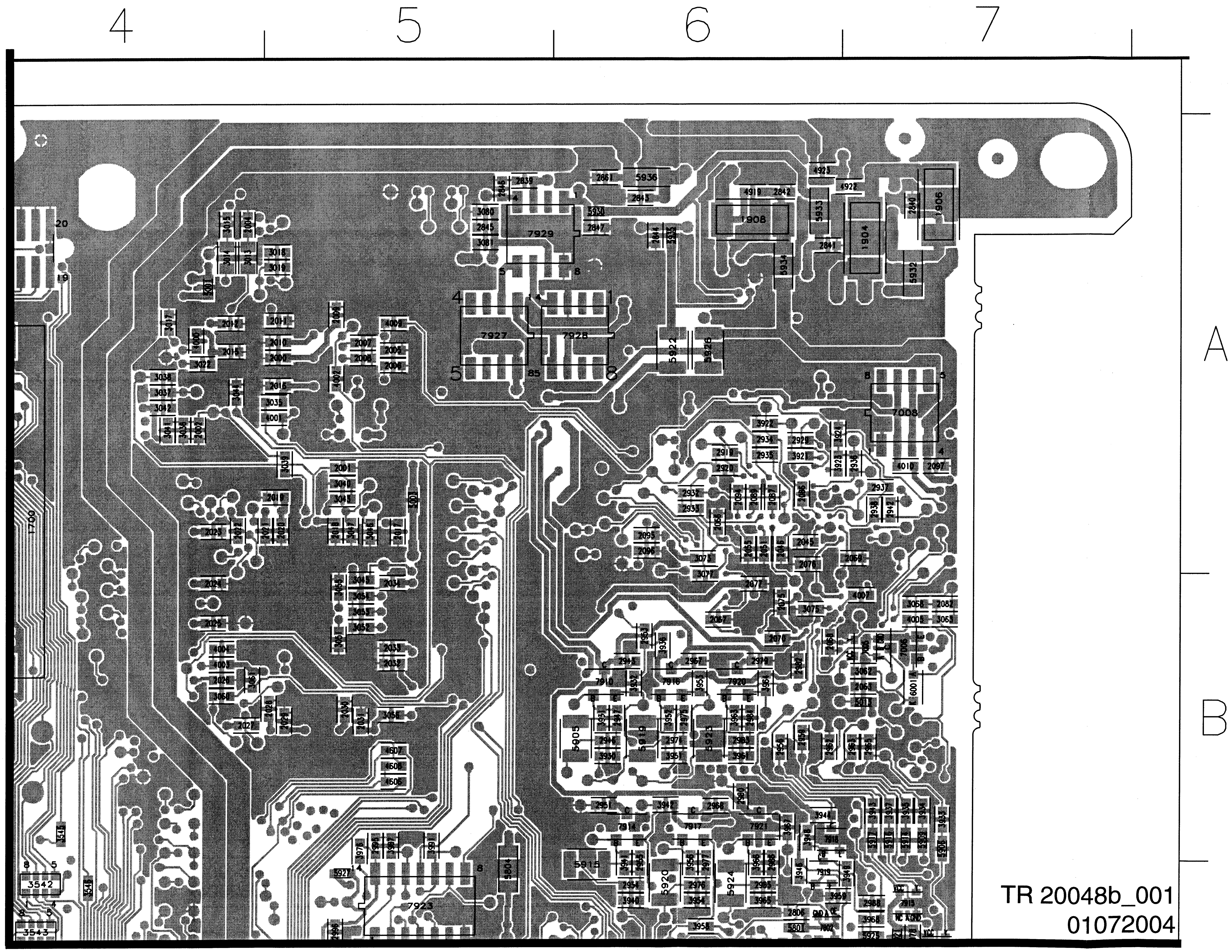
3543

Layout: FEBE Bottom View Part 2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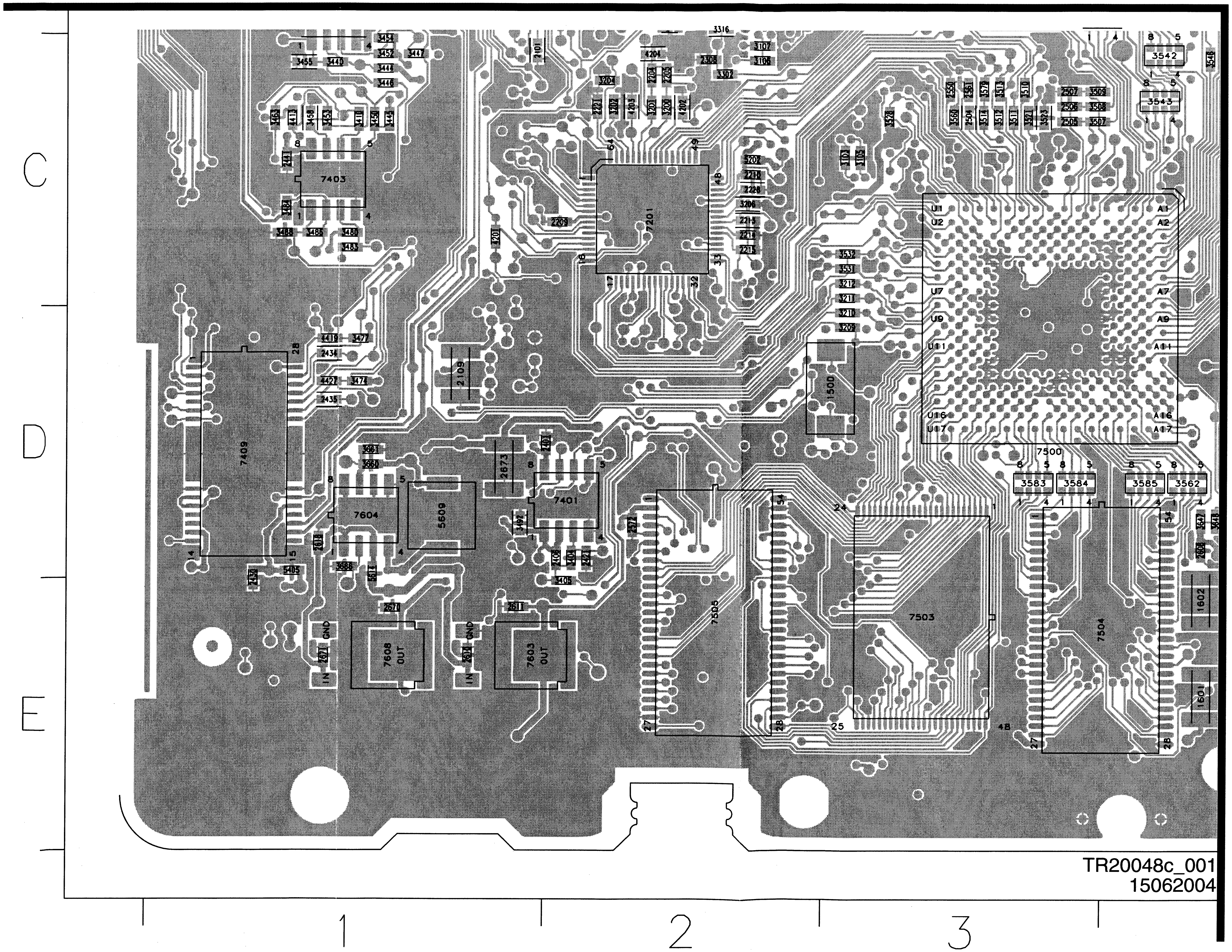
TR 20048b_001
01072004

Layout: FEBE Bottom View Part 3


C
D
E
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4204
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3204
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2209
3202
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3209
1500
2101
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2434
4427
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3660
7604
5600
7401
3405
3406
2405
2670
2671
7608
OUT
7603
GND
IN
7505
7503
7504
7500
U1
U2
U7
U9
U11
U16
U17
A1
A2
A7
A9
A11
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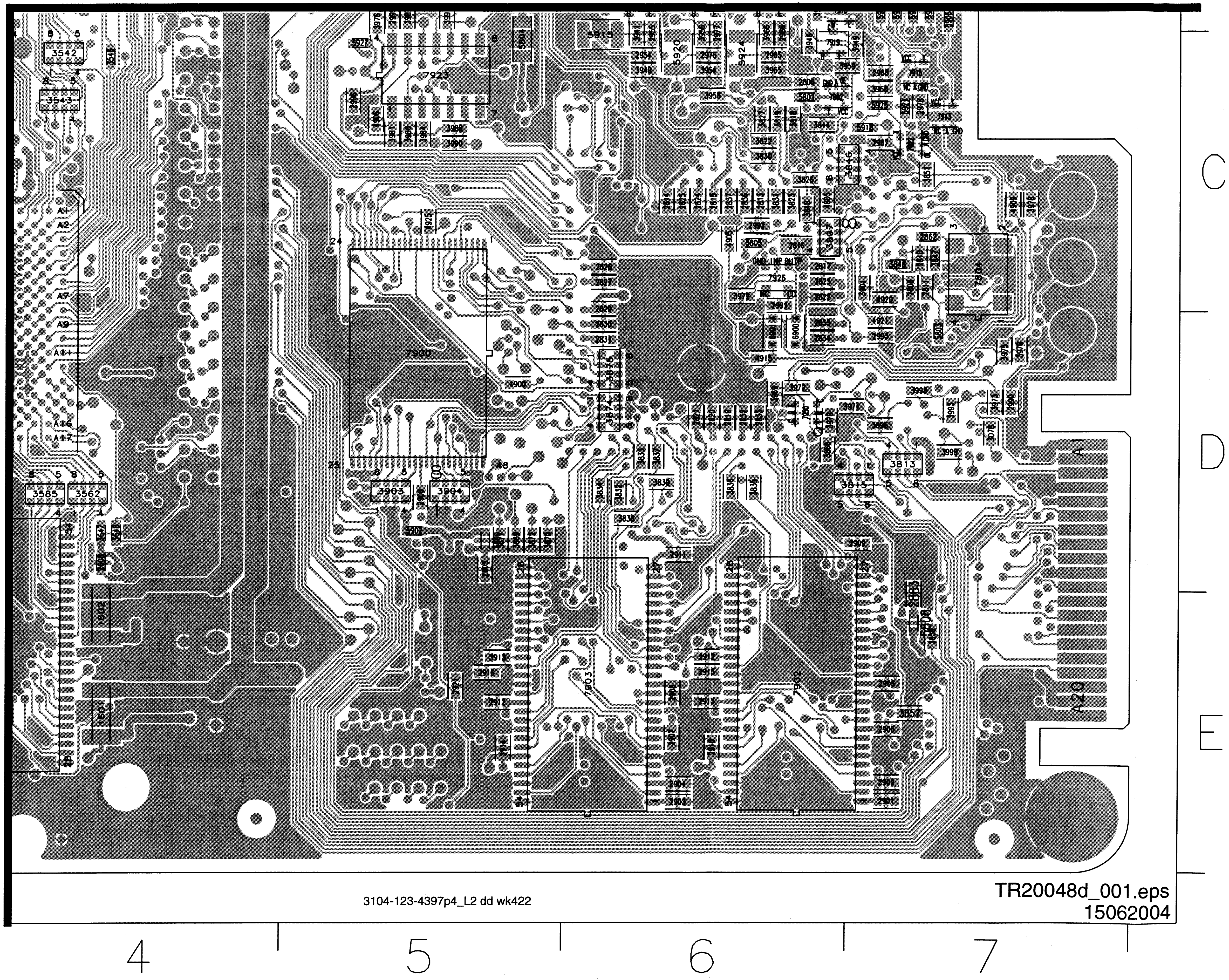
TR20048c_001
15062004

Layout: FEBE Bottom View Part 4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1604
5915
5920
5924
A1
A20
C
D
E
4
5
6
7
3104-123-4397p4_L2 dd wk422
TR20048d_001.eps
15062004

LECO: Fe Opu Interface

1100	D2
2032	H10
2100	E6
2101	K6
2102	F6
2103	B7
2104	K5
2105	K5
2106	F9
2107	E10
2109	I8
2110	F14
3100	H7
3101	H7
3104	B8
3110	F14
3111	G14
3112	F13
3113	E14
3114	F11
3115	D12
3116	D11
3117	E11
3118	F11
4112	D11
5101	D6
5102	I6
5103	I6
5104	J6
6100	J7
7101	E12
7102	F13
7103	E11
7104	E11
7105	H10
I100	B7
I101	B8
I102	H6
I103	J6
I104	J6
I106	J6
I107	K6
I108	I6
I110	G6
I111	H6
I112	G6
I113	J5
I114	J6
I115	F6
I116	H6
I117	H6
I118	H6
I119	I6
I120	D5
I121	D10
I122	E11
I123	E12
I124	E11
I125	E13
I126	E12
I127	F14
I128	I5
I129	I5
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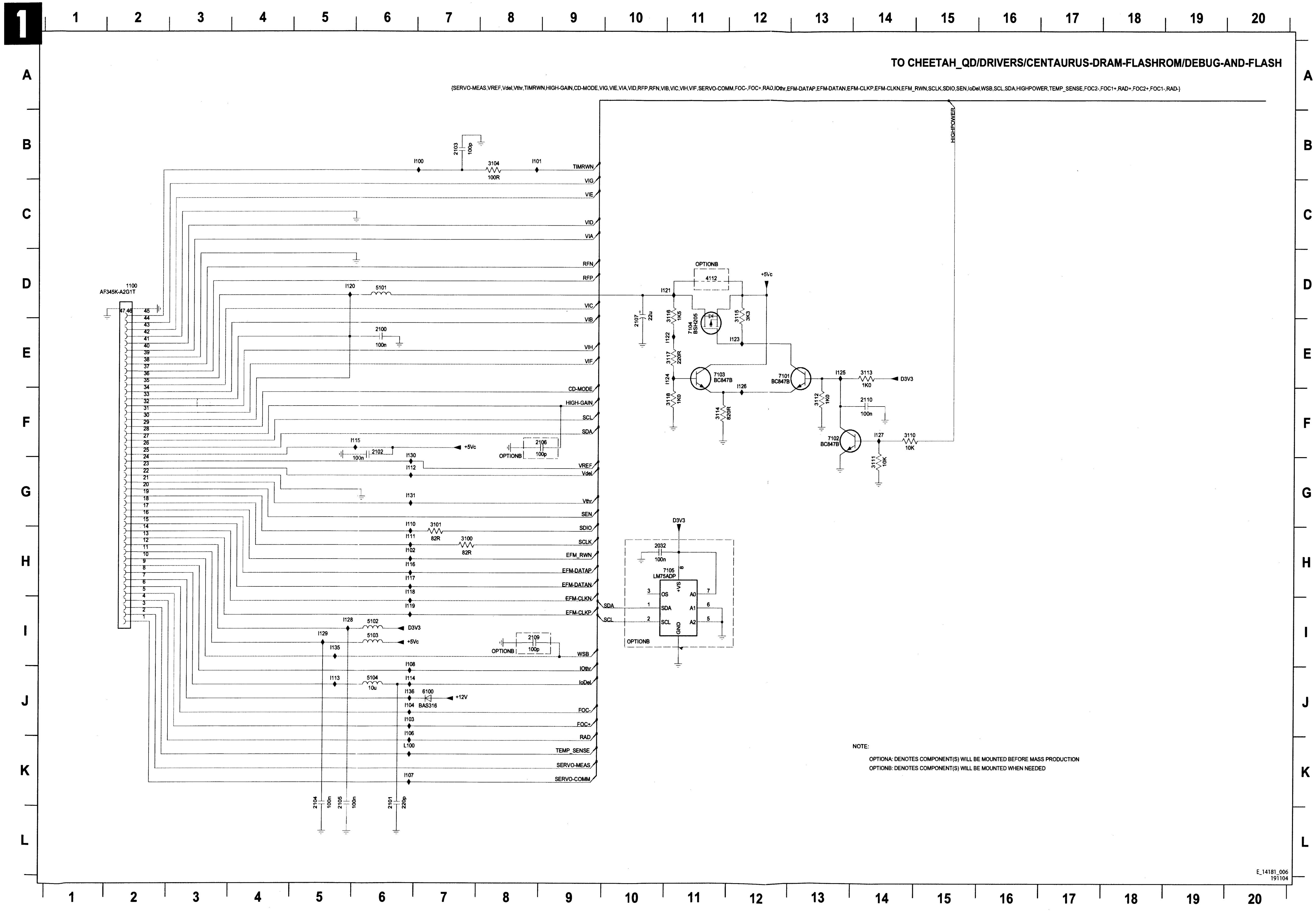
L100	K6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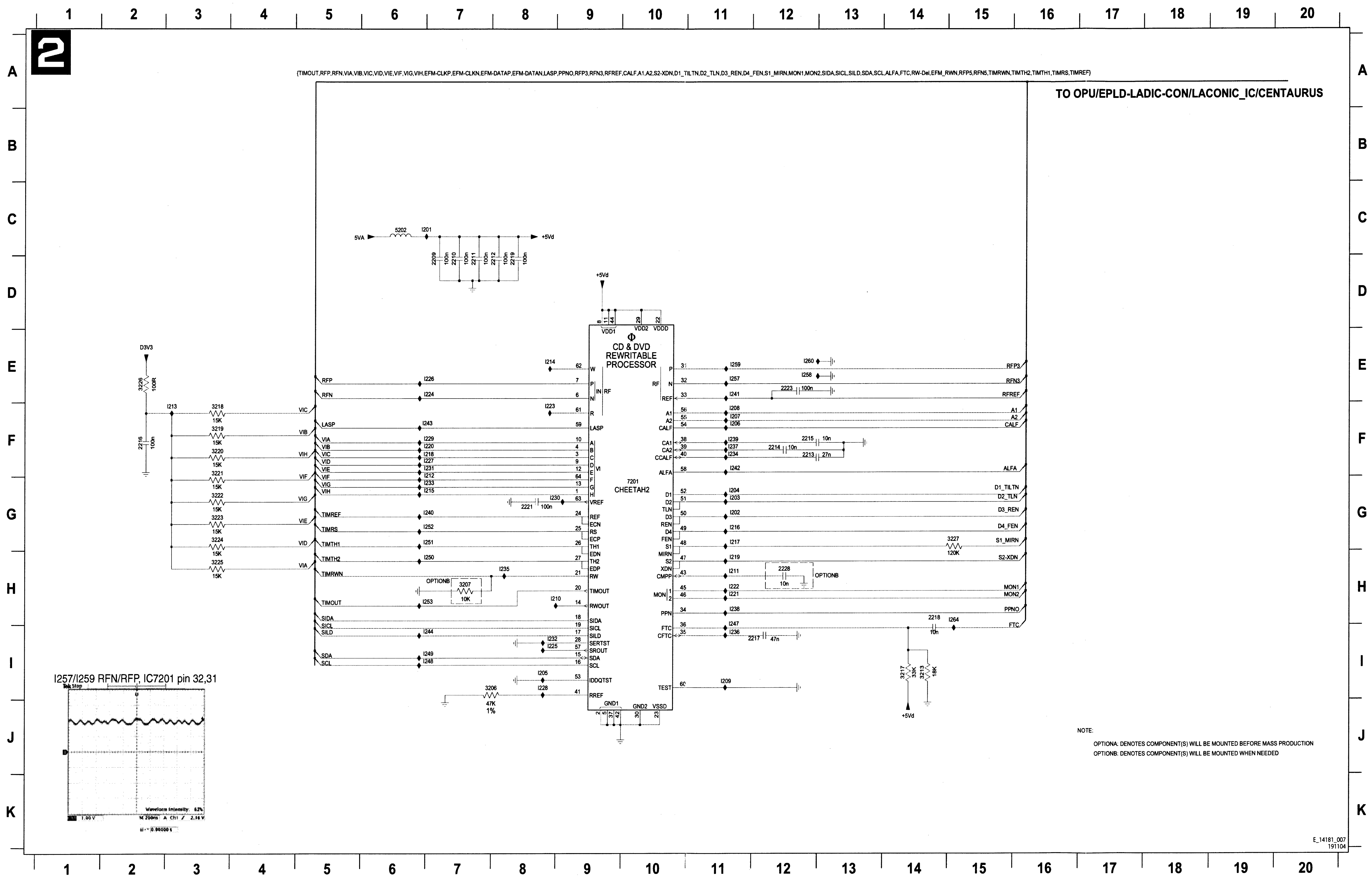
TO CHEETAH_QD/DRIVERS/CENTAURUS-DRAM-FLASHROM/DEBUG-AND-FLASH
{SERVO-MEAS,VREF,Vdel,Vthr,TIMRWN,HIGH-GAIN,CD-MODE,VIG,VIE,VIA,VID,RFP,RFN,VIB,VIC,VIH,VIF,SERVO-COMM,FOC-,FOC+,RAD,IOthr,EFM-DATAP,EFM-DATAN,EFM-CLKP,EFM-CLKN,EFM_RWN,SCLK,SDIO,SEN,IoDel,WSB,SCL,SDA,HIGHPOWER,TEMP_SENSE,FOC2-,FOC1+,RAD+,FOC2+,FOC1-,RAD-}
HIGHPOWER
1100
AF345K-A2G1T
TIMRWN
VIG
VIE
VID
VIA
RFN
RFP
VIC
VIB
VIH
VIF
CD-MODE
HIGH-GAIN
SCL
SDA
VREF
Vdel
Vthr
SEN
SDIO
SCLK
EFM_RWN
EFM-DATAP
EFM-DATAN
EFM-CLKN
EFM-CLKP
WSB
IOthr
IoDel
FOC-
FOC+
RAD
TEMP_SENSE
SERVO-MEAS
SERVO-COMM
2103 100p
I100
3104 100R
I101
I120
5101
2100 100n
I115
2102 100n
+5Vc
I130
I112
OPTIONB
2106 100p
I131
I110
3101 82R
I111
3100 82R
I102
I116
I117
I118
I119
I128
5102
D3V3
I129
5103
+5Vc
I135
OPTIONB
2109 100p
I108
I113
5104 10u
I114
I136
6100 BAS316
+12V
I104
I103
I106
L100
I107
2104 100n
2105 100n
2101 220p
OPTIONB
4112
+5Vc
I121
2107 22u
3116 1K5
7104 BSH205
3115 3K3
I122
I123
3117 220R
I124
7103 BC847B
I126
3118 1K0
3114 820R
7101 BC847B
I125
3113 1K0
D3V3
3112 1K0
2110 100n
7102 BC847B
I127
3110 10K
3111 10K
D3V3
2032 100n
7105 LM75ADP
OS
SDA
SCL
+VS
GND
A0
A1
A2
SDA
SCL
OPTIONB
E_14181_006 191104

NOTE:

OPTIONA: DENOTES COMPONENT(S) WILL BE MOUNTED BEFORE MASS PRODUCTION
OPTIONB: DENOTES COMPONENT(S) WILL BE MOUNTED WHEN NEEDED

LECO: Fe Pre-Processing

2209 D7
2210 D7
2211 D7
2212 D8
2213 F12
2214 F12
2215 F12
2216 F2
2217 I12
2218 H14
2219 D8
2221 G8
2223 E12
2228 H12
3206 I7
3207 H7
3213 I14
3217 I14
3218 F3
3219 F3
3220 F3
3221 F3
3222 G3
3223 G3
3224 G3
3225 H3
3226 E2
3227 G15
5202 C6
7201 G10
I201 C6
I202 G11
I203 G11
I204 G11
I205 I8
I206 F11
I207 F11
I208 F11
I209 I11
I210 H8
I211 H11
I212 F7
I213 F3
I214 E8
I215 G7
I216 G11
I217 G11
I218 F7
I219 H11
I220 F7
I221 H11
I222 H11
I223 F8
I224 E7
I225 I8
I226 E7
I227 F7
I228 I8
I229 F7
I230 G8
I231 F7
I232 I8
I233 G7
I234 F11
I235 H8
I236 I11
I237 F11
I238 H11
I239 F11
I240 G7
I241 E11
I242 F11
I243 F7
I244 I7
I247 H11
I248 I7
I249 I7
I250 H7
I251 G7
I252 G7
I253 H7
I257 E11
I258 E12
I259 E11
I260 E12
I264 H15

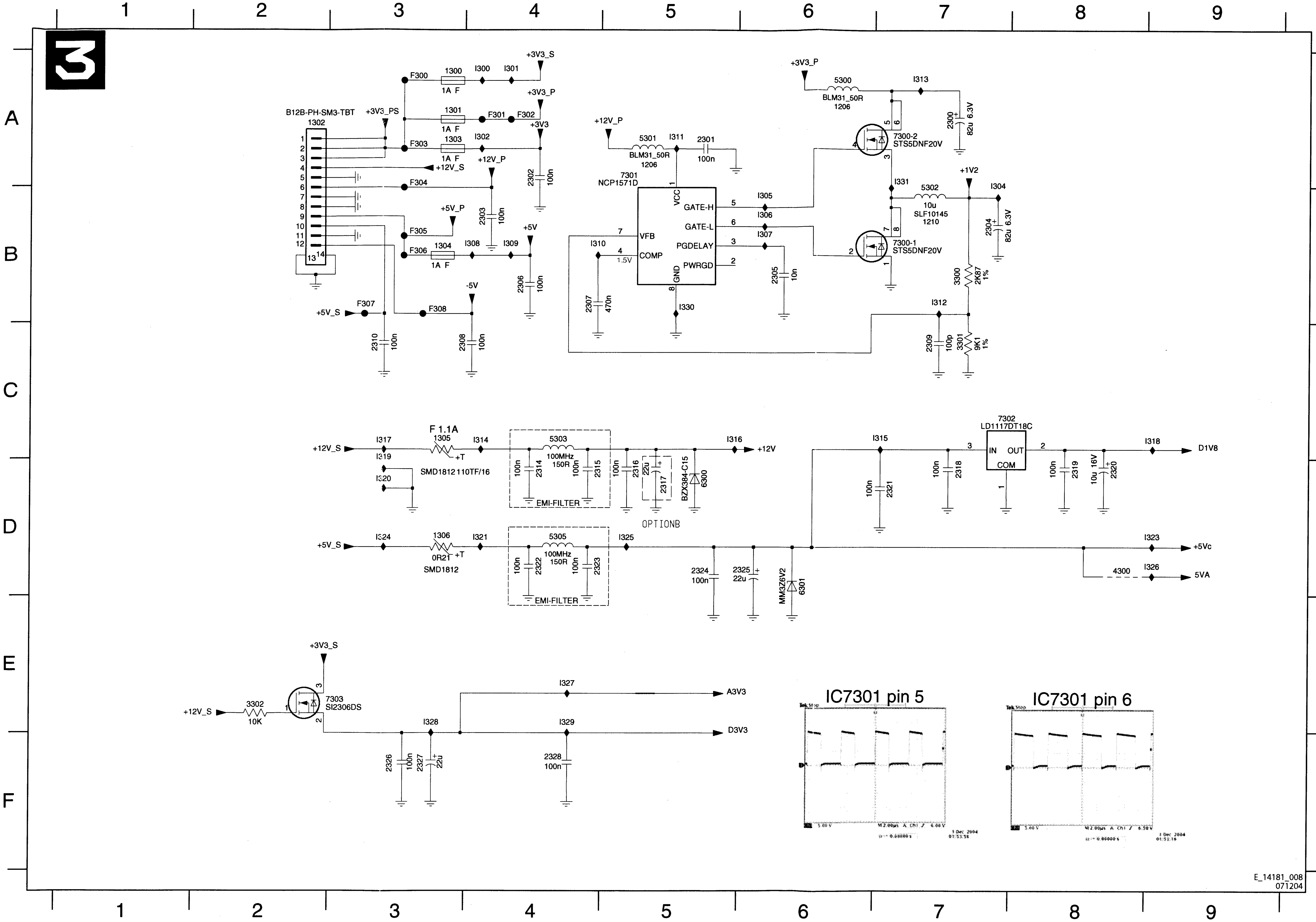

2
(TIMOUT,RFP,RFN,VIA,VIB,VIC,VID,VIE,VIF,VIG,VIH,EFM-CLKP,EFM-CLKN,EFM-DATAP,EFM-DATAN,LASP,PPNO,RFP3,RFN3,RFREF,CALF,A1,A2,S2-XDN,D1_TILTN,D2_TLN,D3_REN,D4_FEN,S1_MIRN,MON1,MON2,SIDA,SICL,SILD,SDA,SCL,ALFA,FTC,RW-Del,EFM_RWN,RFP5,RFN5,TIMRWN,TIMTH2,TIMTH1,TIMRS,TIMREF)
TO OPU/EPLD-LADIC-CON/LACONIC_IC/CENTAURUS
5VA
5202
I201
+5Vd
2209 100n
2210 100n
2211 100n
2212 100n
2219 100n
7201
CHEETAH2
CD & DVD REWRITABLE PROCESSOR
VDD1
VDD2
VDDD
GND1
GND2
VSSD
D3V3
3226 100R
2216 100n
I213
3218 15K
3219 15K
3220 15K
3221 15K
3222 15K
3223 15K
3224 15K
3225 15K
VIC
VIB
VIH
VIF
VIG
VIE
VID
VIA
RFP
RFN
LASP
TIMREF
TIMRS
TIMTH1
TIMTH2
TIMRWN
TIMOUT
SIDA
SICL
SILD
SDA
SCL
OPTIONB
3207 10K
3206 47K 1%
2221 100n
RREF
IDDQTST
TEST
RWOUT
SERTST
SROUT
P
N
REF
RF
A1
A2
CALF
CA1
CA2
CCALF
ALFA
D1
D2
TLN
D3
REN
D4
FEN
S1
MIRN
S2
XDN
CMPP
MON
PPN
FTC
CFTC
2223 100n
2215 10n
2214 10n
2213 27n
2228 10n
2217 47n
2218 10n
3227 120K
3217 33K
3213 18K
RFP3
RFN3
RFREF
D1_TILTN
D2_TLN
D3_REN
D4_FEN
S1_MIRN
S2-XDN
MON1
MON2
PPNO
I257/I259 RFN/RFP, IC7201 pin 32,31
Tek Stop
1.00 V
M 200ns A Ch1 ƒ 2.16 V
Waveform intensity: 62%
E_14181_007
191104

NOTE:

OPTIONA: DENOTES COMPONENT(S) WILL BE MOUNTED BEFORE MASS PRODUCTION

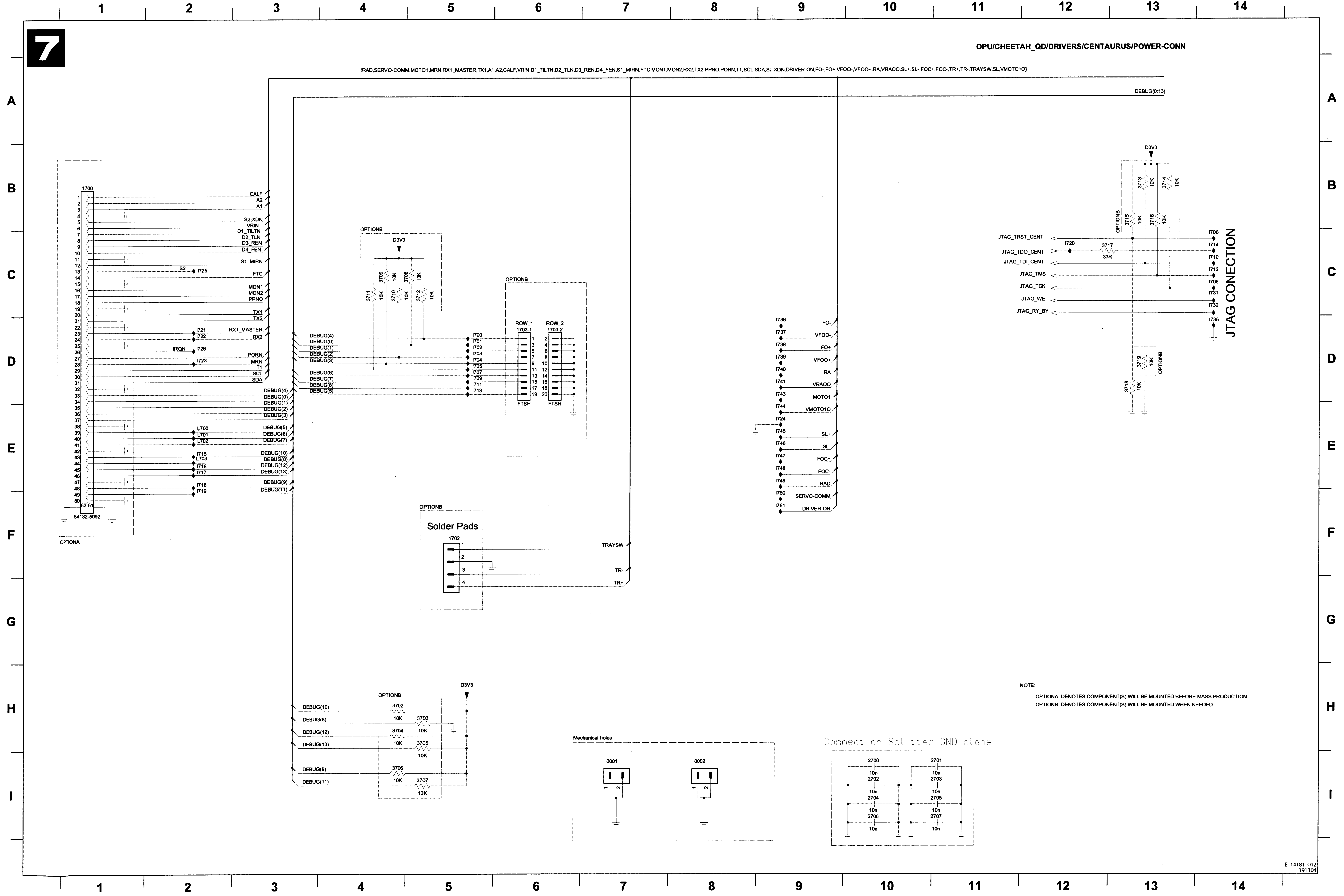
OPTIONB: DENOTES COMPONENT(S) WILL BE MOUNTED WHEN NEEDED

LECO: Fe be Power Supply


3
B12B-PH-SM3-TBT
1302
+3V3_PS
F300
1300
1A F
I300
I301
+3V3_S
1301
F301
F302
+3V3_P
+3V3
F303
1303
I302
+12V_P
+12V_S
2302
100n
F304
+5V_P
2303
100n
F305
F306
1304
I308
I309
+5V
2306
100n
-5V
F307
+5V_S
F308
2310
100n
2308
100n
+12V_P
5301
BLM31_50R
1206
I311
2301
100n
7301
NCP1571D
VCC
GATE-H
GATE-L
PGDELAY
PWRGD
VFB
COMP
GND
1.5V
I305
I306
I307
I310
I330
2305
10n
2307
470n
+3V3_P
5300
BLM31_50R
1206
I313
2300
82u 6.3V
7300-2
STS5DNF20V
I331
5302
10u
SLF10145
1210
+1V2
I304
2304
82u 6.3V
7300-1
STS5DNF20V
I312
3300
2K87
1%
2309
100p
3301
9K1
1%
F 1.1A
1305
+T
SMD1812110TF/16
I317
I319
I320
I314
5303
100MHz
150R
2314
2315
100n
EMI-FILTER
I316
+12V
2316
2317
22u
BZX384-C15
6300
OPTIONB
I315
2321
100n
2318
100n
7302
LD1117DT18C
IN
OUT
COM
2319
100n
2320
10u 16V
I318
D1V8
I324
1306
0R21
SMD1812
I321
5305
100MHz
150R
2322
2323
100n
EMI-FILTER
I325
2324
100n
2325
22u
MM3Z6V2
6301
I323
+5Vc
4300
I326
5VA
+3V3_S
+12V_S
3302
10K
7303
SI2306DS
I328
I327
A3V3
I329
D3V3
2326
100n
2327
22u
2328
100n
IC7301 pin 5
IC7301 pin 6
E_14181_008
071204

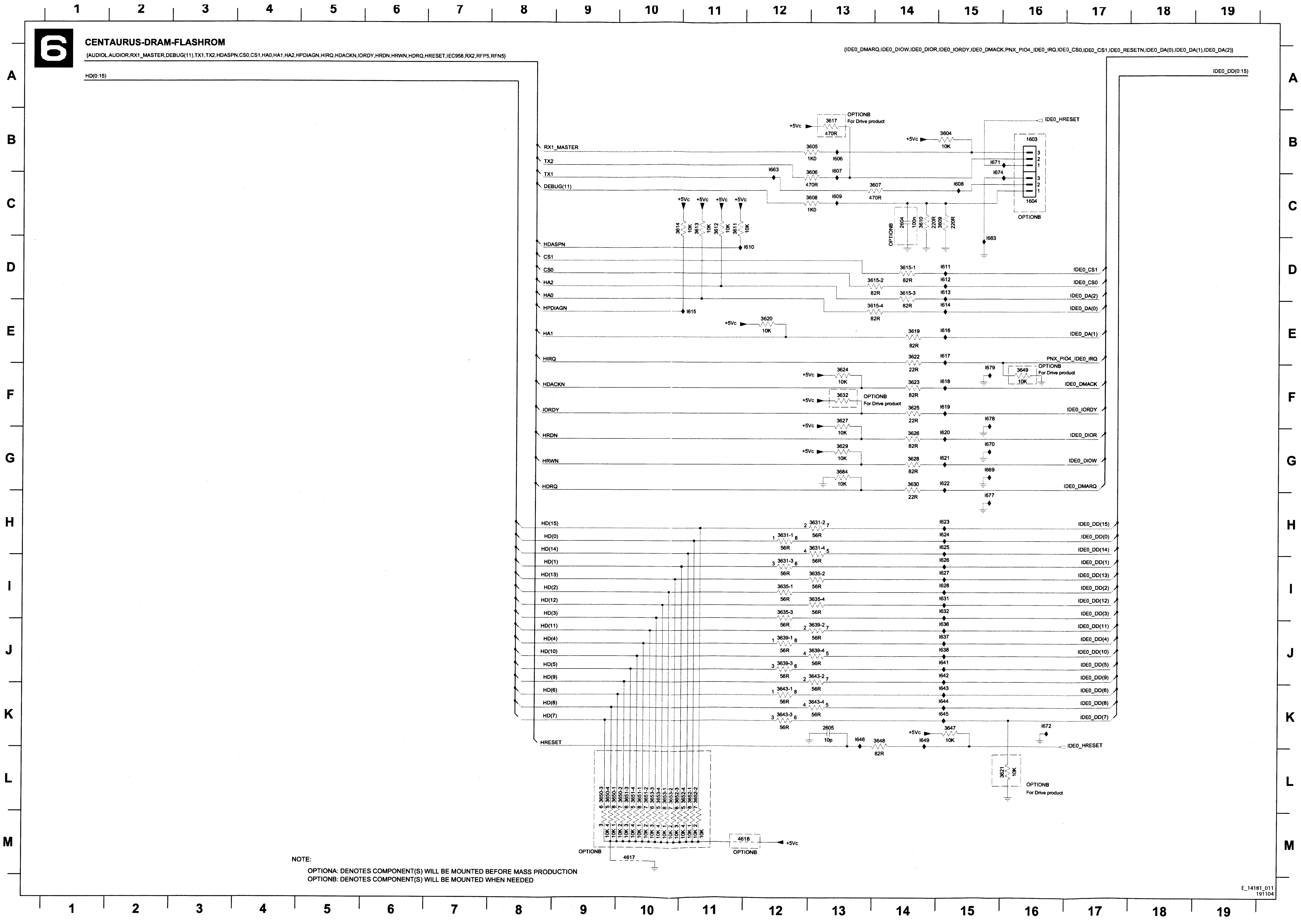
1300	A3
1301	A3
1302	A2
1303	A3
1304	B3
1305	C3
1306	D3
2300	A7
2301	A5
2302	A4
2303	B4
2304	B7
2305	B6
2306	B4
2307	B4
2308	C3
2309	C7
2310	C3
2314	D4
2315	D4
2316	D5
2317	D5
2318	D7
2319	D8
2320	D8
2321	D7
2322	D4
2323	D4
2324	D5
2325	D6
2326	F3
2327	F3
2328	F4
3300	B7
3301	C7
3302	E2
4300	D8
5300	A6
5301	A5
5302	B7
5303	C4
5305	D4
6300	D5
6301	D6
7300-1	B7
7300-2	A7
7301	A5
7302	C7
7303	E2
F300	A3
F301	A4
F302	A4
F303	A3
F304	A3
F305	B3
F306	B3
F307	B3
F308	B3
I300	A4
I301	A4
I302	A4
I304	A7
I305	B6
I306	B6
I307	B6
I308	B4
I309	B4
I310	B4
I311	A5
I312	B7
I313	A7
I314	C4
I315	C7
I316	C5
I317	C3
I318	C9
I319	C3
I320	D3
I321	D4
I323	D9
I324	D3
I325	D5
I326	D9
I327	E4
I328	E3
I329	E4
I330	B5
I331	A7

LECO: Be Debug Connectors


7
OPU/CHEETAH_QD/DRIVERS/CENTAURUS/POWER-CONN
RAD,SERVO-COMM,MOTO1,MRN,RX1_MASTER,TX1,A1,A2,CALF,VRIN,D1_TILTN,D2_TLN,D3_REN,D4_FEN,S1_MIRN,FTC,MON1,MON2,RX2,TX2,PPNO,PORN,T1,SCL,SDA,S2-XDN,DRIVER-ON,FO-,FO+,VFOO-,VFOO+,RA,VRAOO,SL+,SL-,FOC+,FOC-,TR+,TR-,TRAYSW,SL,VMOTO1O)
DEBUG(0:13)
1700
CALF
A2
A1
S2-XDN
VRIN
D1_TILTN
D2_TLN
D3_REN
D4_FEN
S1_MIRN
S2
I725
FTC
MON1
MON2
PPNO
TX1
TX2
I721
I722
RX1_MASTER
RX2
IRQN
I726
PORN
I723
MRN
T1
SCL
SDA
DEBUG(4)
DEBUG(0)
DEBUG(1)
DEBUG(2)
DEBUG(3)
L700
L701
L702
DEBUG(5)
DEBUG(6)
DEBUG(7)
I715
L703
I716
I717
DEBUG(10)
DEBUG(8)
DEBUG(12)
DEBUG(13)
I718
I719
DEBUG(9)
DEBUG(11)
52 51
54132-5092
OPTIONA
OPTIONB
D3V3
3709 10K
3708 10K
3711 10K
3710 10K
3712 10K
OPTIONB
ROW_1
1703-1
ROW_2
1703-2
I700
I701
I702
I703
I704
I705
I707
I709
I711
I713
DEBUG(6)
DEBUG(7)
DEBUG(8)
DEBUG(5)
FTSH
FTSH
OPTIONB
Solder Pads
1702
TRAYSW
TR-
TR+
I736 FO-
I737 VFOO-
I738 FO+
I739 VFOO+
I740 RA
I741 VRAOO
I743 MOTO1
I744 VMOTO1O
I724
I745 SL+
I746 SL-
I747 FOC+
I748 FOC-
I749 RAD
I750 SERVO-COMM
I751 DRIVER-ON
D3V3
OPTIONB
3713 10K
3714 10K
3715 10K
3716 10K
JTAG_TRST_CENT
I720
3717 33R
JTAG_TDO_CENT
JTAG_TDI_CENT
JTAG_TMS
JTAG_TCK
JTAG_WE
JTAG_RY_BY
I706
I714
I710
I712
I708
I731
I732
I735
JTAG CONECTION
3719 10K
OPTIONB
3718 10K
D3V3
OPTIONB
DEBUG(10)
3702 10K
DEBUG(8)
3703 10K
DEBUG(12)
3704 10K
DEBUG(13)
3705 10K
DEBUG(9)
3706 10K
DEBUG(11)
3707 10K
Mechanical holes
0001
0002
Connection Splitted GND plane
2700 10n
2701 10n
2702 10n
2703 10n
2704 10n
2705 10n
2706 10n
2707 10n
NOTE:
OPTIONA: DENOTES COMPONENT(S) WILL BE MOUNTED BEFORE MASS PRODUCTION
OPTIONB: DENOTES COMPONENT(S) WILL BE MOUNTED WHEN NEEDED
E_14181_012
191104

0001	I7
0002	I8
1700	B1
1702	F5
1703-1	D6
1703-2	D6
2700	I10
2701	I11
2702	I10
2703	I11
2704	I10
2705	I11
2706	I10
2707	I11
3702	H4
3703	H5
3704	H4
3705	H5
3706	I4
3707	I5
3708	C5
3709	C4
3710	C4
3711	C4
3712	C5
3713	B13
3714	B13
3715	B13
3716	B13
3717	C12
3718	D13
3719	D13
I700	D5
I701	D5
I702	D5
I703	D5
I704	D5
I705	D5
I706	C14
I707	D5
I708	C14
I709	D5
I710	C14
I711	D5
I712	C14
I713	D5
I714	C14
I715	E2
I716	E2
I717	E2
I718	E2
I719	F2
I720	C12
I721	D2
I722	D2
I723	D2
I724	E9
I725	C2
I726	D2
I731	C14
I732	C14
I735	D14
I736	D9
I737	D9
I738	D9
I739	D9
I740	D9
I741	D9
I743	D9
I744	E9
I745	E9
I746	E9
I747	E9
I748	E9
I749	E9
I750	F9
I751	F9
L700	E2
L701	E2
L702	E2
L703	E2

LECO: FeBe Interface

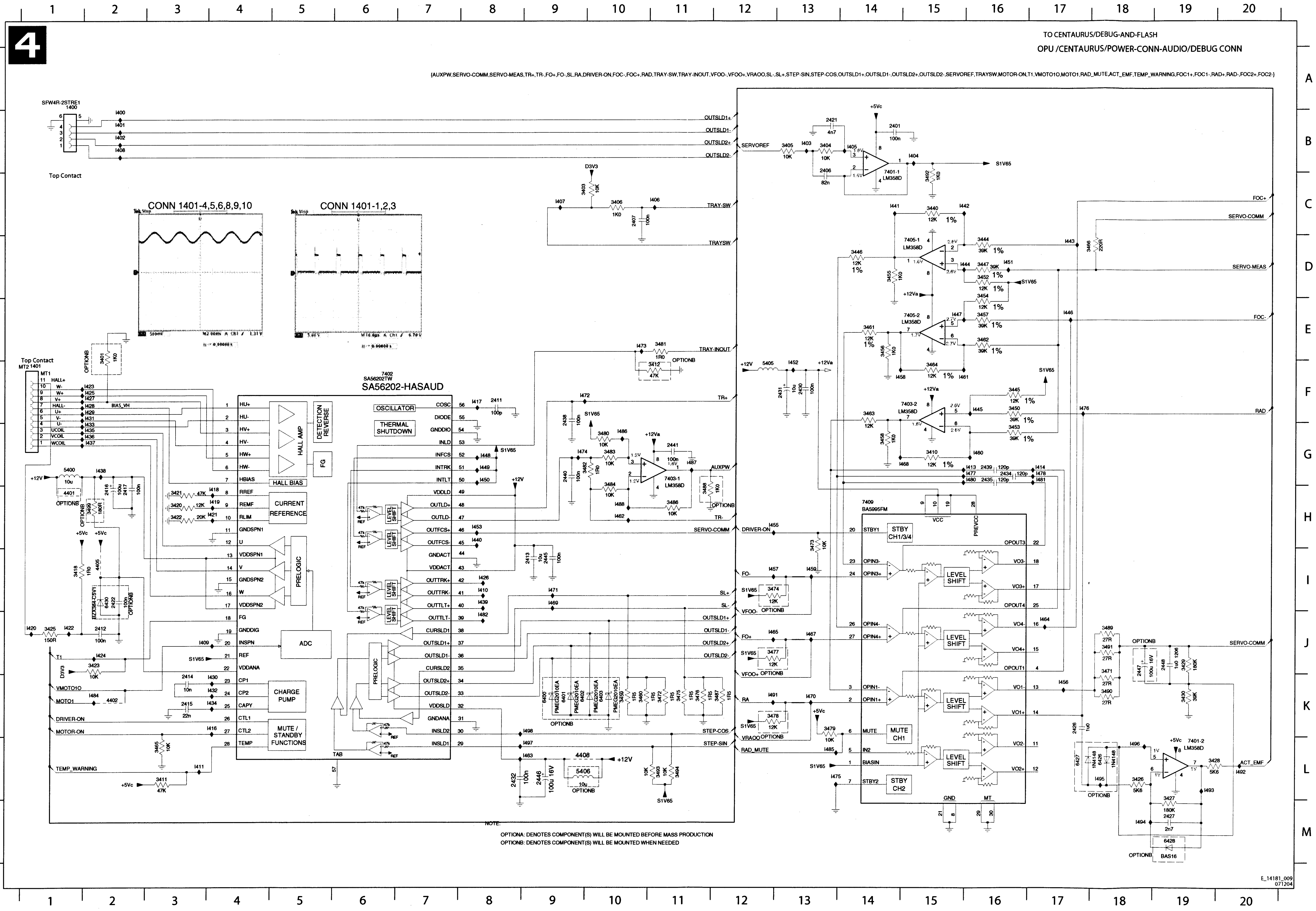

6
CENTAURUS-DRAM-FLASHROM
{AUDIOL,AUDIOR,RX1_MASTER,DEBUG(11),TX1,TX2,HDASPN,CS0,CS1,HA0,HA1,HA2,HPDIAGN,HIRQ,HDACKN,IORDY,HRDN,HRWN,HDRQ,HRESET,IEC958,RX2,RFP5,RFN5}
HD(0:15)
{IDE0_DMARQ,IDE0_DIOW,IDE0_DIOR,IDE0_IORDY,IDE0_DMACK,PNX_PIO4_IDE0_IRQ,IDE0_CS0,IDE0_CS1,IDE0_RESETN,IDE0_DA(0),IDE0_DA(1),IDE0_DA(2)}
IDE0_DD(0:15)
OPTIONB
For Drive product
IDE0_HRESET
RX1_MASTER
TX2
TX1
DEBUG(11)
HDASPN
CS1
CS0
HA2
HA0
HPDIAGN
HA1
HIRQ
HDACKN
IORDY
HRDN
HRWN
HDRQ
HRESET
IDE0_CS1
IDE0_CS0
IDE0_DA(2)
IDE0_DA(0)
IDE0_DA(1)
PNX_PIO4_IDE0_IRQ
IDE0_DMACK
IDE0_IORDY
IDE0_DIOR
IDE0_DIOW
IDE0_DMARQ
1603
1604
+5Vc
470R
1K0
10K
82R
22R
56R
10p
100n
220R
4617
4618
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
A B C D E F G H I J K L M
E_14181_011
191104

NOTE:

OPTIONA: DENOTES COMPONENT(S) WILL BE MOUNTED BEFORE MASS PRODUCTION
OPTIONB: DENOTES COMPONENT(S) WILL BE MOUNTED WHEN NEEDED

1603	B16
1604	C16
2604	C14
2605	K13
3604	B15
3605	B13
3606	C13
3607	C14
3608	C13
3609	C15
3610	C14
3611	C11
3612	C11
3613	C11
3614	C10
3615-1	D14
3615-2	D14
3615-3	D14
3615-4	E14
3617	B13
3619	E14
3620	E12
3621	L16
3622	E14
3623	F14
3624	F13
3625	F14
3626	G14
3627	F13
3628	G14
3629	G13
3630	G14
3631-1	H12
3631-2	H13
3631-3	I12
3631-4	H13
3632	F13
3635-1	I12
3635-2	I13
3635-3	I12
3635-4	I13
3639-1	J12
3639-2	J13
3639-3	J12
3639-4	J13
3643-1	K12
3643-2	J13
3643-3	K12
3643-4	K13
3647	K15
3648	K14
3649	F16
3650-1	L9
3650-2	L10
3650-3	L9
3650-4	L9
3651-1	L10
3651-2	L10
3651-3	L10
3651-4	L10
3652-1	L11
3652-2	L11
3652-3	L10
3652-4	L11
3653-1	L10
3653-2	L10
3653-3	L10
3653-4	L10
3684	G13
4617	M10
4618	M12
I606	B13
I607	B13
I608	C15
I609	C13
I610	D12
I611	D15
I612	D15
I613	D15
I614	E15
I615	E11
I616	E15
I617	E15
I618	F15
I619	F15
I620	G15
I621	G15
I622	G15
I623	H15
I624	H15
I625	H15
I626	I15
I627	I15
I628	I15
I631	I15
I632	I15
I636	J15
I637	J15
I638	J15
I641	J15
I642	J15
I643	K15
I644	K15
I645	K15
I646	K13
I649	K14
I663	B12
I669	G15
I670	G15
I671	B15
I672	K16
I674	B15
I677	H15
I678	F15
I679	F15
I683	D15

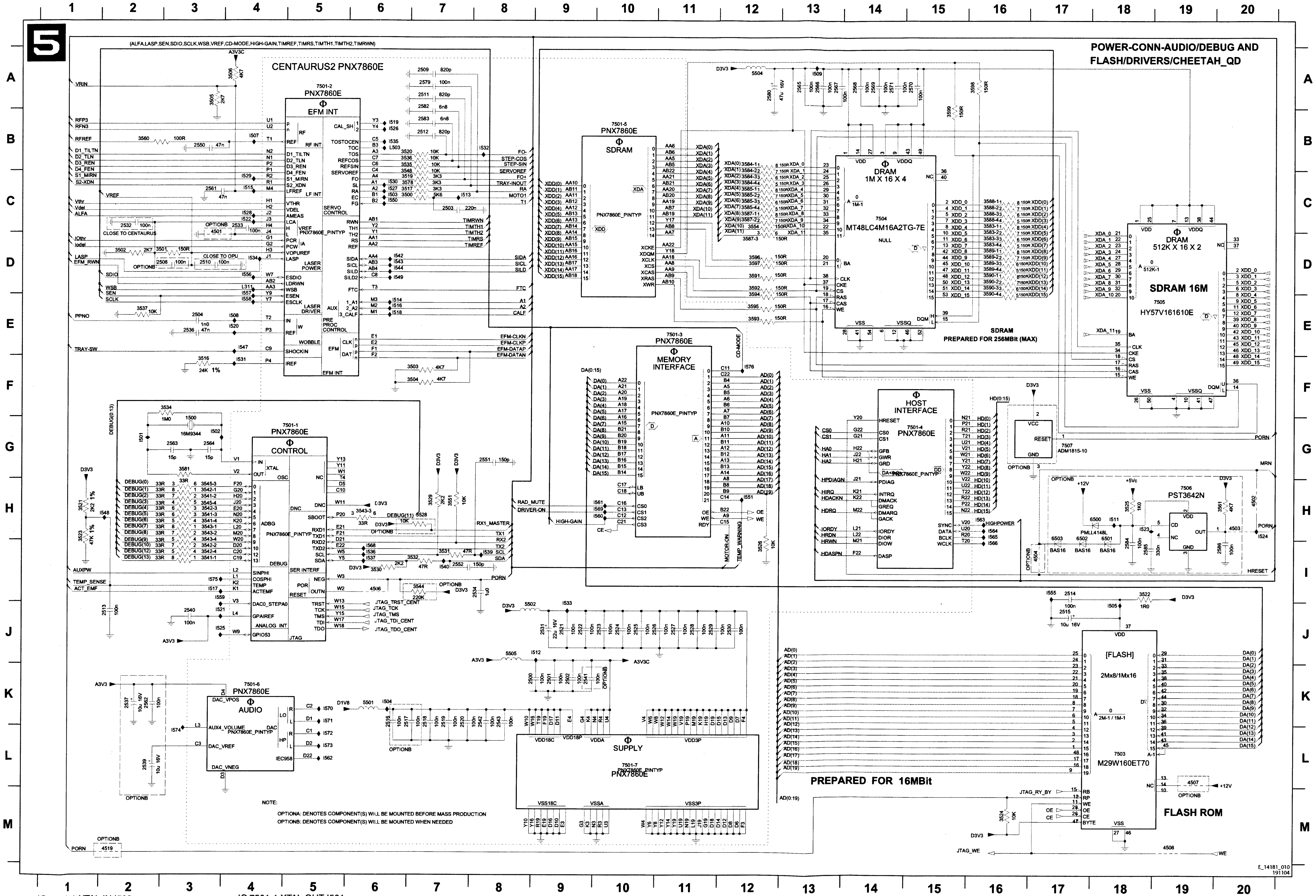
LECO: Fe Drivers


4
TO CENTAURUS/DEBUG-AND-FLASH
OPU /CENTAURUS/POWER-CONN-AUDIO/DEBUG CONN
SFW4R-2STRE1 1400
Top Contact
CONN 1401-4,5,6,8,9,10
CONN 1401-1,2,3
Top Contact MT2 1401
7402 SA56202TW
SA56202-HASAUD
HALL AMP
DETECTION REVERSE
OSCILLATOR
THERMAL SHUTDOWN
FG
HALL BIAS
CURRENT REFERENCE
PRELOGIC
ADC
CHARGE PUMP
MUTE / STANDBY FUNCTIONS
LEVEL SHIFT
7401-1 LM358D
7403-1 LM358D
7405-1 LM358D
7405-2 LM358D
7403-2 LM358D
7401-2 LM358D
7409 BA5995FM
STBY CH1/3/4
MUTE CH1
STBY CH2
OUTSLD1+
OUTSLD1-
OUTSLD2+
OUTSLD2-
SERVOREF
S1V65
TRAY-SW
TRAYSW
TRAY-INOUT
TR+
TR-
AUXPW
SERVO-COMM
DRIVER-ON
FO-
FO+
VFOO-
VFOO+
SL+
SL-
RA
VRAOO
RAD_MUTE
STEP-COS
STEP-SIN
FOC+
SERVO-COMM
SERVO-MEAS
FOC-
RAD
ACT_EMF
T1
VMOTO1O
MOTO1
DRIVER-ON
MOTOR-ON
TEMP_WARNING
OPTIONB
E_14181_009 071204

NOTE:
OPTIONA: DENOTES COMPONENT(S) WILL BE MOUNTED BEFORE MASS PRODUCTION
OPTIONB: DENOTES COMPONENT(S) WILL BE MOUNTED WHEN NEEDED

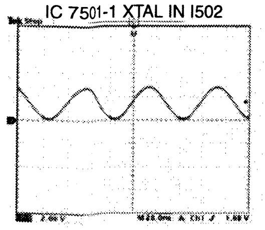
1400	A1
1401	F1
2401	B14
2406	C13
2407	C10
2411	F8
2412	J2
2413	I9
2414	K3
2415	K3
2416	H2
2417	H2
2421	B13
2422	I2
2426	K17
2427	M19
2430	F13
2431	F13
2432	L8
2434	G16
2435	G16
2438	F9
2439	G16
2440	G9
2441	G11
2445	I9
2446	L9
2447	J18
2448	J19
3401	E2
3403	C9
3404	B13
3405	B13
3406	C10
3410	G15
3411	L3
3412	F11
3418	I1
3420	H3
3421	H3
3422	H3
3423	J2
3425	J1
3426	L18
3427	M19
3428	L19
3429	J19
3430	K19
3440	C15
3444	D16
3445	F16
3446	D14
3447	D16
3450	F16
3452	D16
3453	G16
3454	E16
3455	D14
3456	E14
3457	E16
3458	G14
3459	K10
3460	K10
3461	E14
3462	E16
3463	F14
3464	F15
3465	L3
3466	D17
3471	J18
3472	K11
3473	H13
3474	I12
3475	K11
3476	K11
3477	J12
3478	K12
3479	K13
3480	G10
3481	E11
3482	G10
3483	G10
3484	H10
3486	H11
3487	K12
3488	H11
3489	J18
3490	K18
3491	J18
3492	C15
3493	L11
3494	L11
3499	H2
4401	H1
4402	K2
4405	I2
4408	L9
5400	G1
5405	F12
5406	L9
6400	K9
6401	K9
6402	K9
6403	K10
6426	L18
6427	L17
6428	M19
6430	I2
7401-1	C14
7401-2	L19
7402	F6
7403-1	G11
7403-2	F15
7405-1	D15
7405-2	E15
7409	H14
I400	B2
I401	B2
I402	B2
I403	B13
I404	B15
I405	B14
I406	C11
I407	C9
I408	B2
I409	J3
I410	I8
I411	L3
I413	G16
I414	G17
I416	K4
I417	F8
I418	H4
I419	H4
I420	J1
I421	H4
I422	J1
I423	F2
I424	J2
I425	F2
I426	I8
I427	F2
I428	F2
I429	F2
I430	K4
I431	F2
I432	K4
I433	G2
I434	K4
I435	G2
I436	G2
I437	G2
I438	G2
I439	I8
I440	H8
I441	C14
I442	C15
I443	D17
I444	D15
I445	F16
I446	E17
I447	E15
I448	G8
I449	G8
I450	G8
I451	D16
I452	F13
I453	H8
I455	H12
I456	K17
I457	I12
I458	F14
I459	I13
I460	G16
I461	F15
I462	H10
I463	L9
I464	J17
I465	J12
I467	J13
I468	G15
I469	I9
I470	K13
I471	I9
I472	F9
I473	E10
I474	G9
I475	L13
I476	F17
I477	G16
I478	G17
I480	G16
I481	G17
I482	J8
I484	K2
I485	L13
I486	G10
I487	G11
I488	H10
I491	K12
I492	L20
I493	L19
I494	M18
I495	L18
I496	L18
I497	L9
I498	K9

LECO: Fe Processor

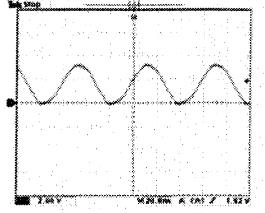

5
CENTAURUS2 PNX7860E
7501-2 PNX7860E EFM INT
7501-5 PNX7860E SDRAM
7504 DRAM 1M X 16 X 4 MT48LC4M16A2TG-7E
SDRAM PREPARED FOR 256MBit (MAX)
POWER-CONN-AUDIO/DEBUG AND FLASH/DRIVERS/CHEETAH_QD
7505 DRAM 512K X 16 X 2 SDRAM 16M HY57V161610E
7501-3 PNX7860E MEMORY INTERFACE
7501-1 PNX7860E CONTROL
7501-4 PNX7860E HOST INTERFACE
7507 ADM1815-10
7506 PST3642N
7501-6 PNX7860E AUDIO
7501-7 PNX7860E SUPPLY
7503 [FLASH] 2Mx8/1Mx16 M29W160ET70
FLASH ROM
PREPARED FOR 16MBit
NOTE:
OPTIONA: DENOTES COMPONENT(S) WILL BE MOUNTED BEFORE MASS PRODUCTION
OPTIONB: DENOTES COMPONENT(S) WILL BE MOUNTED WHEN NEEDED
E_14181_010 191104

1500	G3
2500	K9
2501	K9
2502	K9
2503	C7
2504	E3
2508	D2
2509	A7
2510	D3
2511	A7
2512	B7
2513	J2
2514	I17
2515	J17
2516	K6
2517	K7
2518	K7
2519	K7
2520	K7
2521	J9
2522	J9
2523	J10
2524	J10
2525	J10
2526	J11
2527	J11
2528	J11
2529	J11
2530	J12
2531	J9
2532	C2
2533	C4
2534	I8
2536	E3
2537	K2
2539	L2
2540	J3
2541	K9
2542	K8
2543	K8
2550	B3
2551	G8
2552	I7
2561	C3
2562	K2
2563	G3
2564	G3
2565	A13
2566	A13
2567	A13
2568	A14
2569	A14
2570	A15
2571	A14
2579	A7
2580	A12
2582	A7
2583	B7
2584	I18
2585	I18
2586	I20
3500	C6
3501	D2
3502	D2
3503	F7
3504	F7
3505	A3
3506	A4
3516	F3
3517	C6
3519	C6
3520	B6
3521	H1
3522	I18
3523	H1
3524	M16
3525	H18
3526	I12
3528	H7
3529	H7
3530	I6
3531	I7
3532	I7
3534	F3
3535	B6
3536	B6
3537	E2
3541-1	I3
3541-2	H3
3541-3	H3
3541-4	H3
3542-1	H3
3542-2	I3
3542-3	H3
3542-4	I3
3543-1	H3
3543-2	H3
3543-3	H6
3543-4	H3
3544	I7
3545-3	H3
3545-4	H3
3548	C6
3551	H7
3554	C12
3560	B2
3561	H20
3578	C6
3581	G3
3583-1	C16
3583-2	D16
3583-3	D16
3583-4	D16
3584-1	B12
3584-2	C12
3584-3	C12
3584-4	C12
3585-1	C12
3585-2	C12
3585-3	C12
3585-4	C12
3587-1	C12
3587-2	C12
3587-3	D12
3588-1	C16
3588-2	C16
3588-3	C16
3588-4	C16
3589-1	D16
3589-2	D16
3589-3	D16
3589-4	D16
3590-1	D16
3590-2	D16
3590-3	D16
3590-4	E16
3591	D12
3592	D12
3593	E12
3594	E12
3595	E12
3596	D12
3597	D12
3598	A16
3599	B15
4501	D3
4502	H20
4503	H20
4504	I17
4506	I6
4507	L19
4508	M19
4519	M2
5501	K6
5502	J8
5504	A12
5505	J8
6500	H18
6501	H18
6502	H17
6503	H17
7501-1	G5
7501-2	A5
7501-3	E11
7501-4	G15
7501-5	B10
7501-6	K4
7501-7	L10
7503	L18
7504	C14
7505	E19
7506	H19
7507	G17
I501	G2
I502	G3
I503	C6
I504	K6
I505	J18
I507	B4
I508	E4
I509	A13
I511	H18
I512	J9
I513	C7
I514	E6
I515	C4
I516	E6
I517	I3
I518	E6
I519	B6
I520	E4
I521	J3
I522	C4
I523	H18
I524	H20
I525	J3
I526	B6
I527	C6
I528	C4
I529	C4
I530	C6
I531	F4
I532	B8
I533	J9
I534	D4
I535	B6
I536	I6
I537	I6
I539	I8
I540	I7
I542	D6
I543	D6
I544	D6
I547	E4
I548	H2
I549	D6
I550	C6
I551	H12
I555	I17
I556	D4
I557	D4
I558	E4
I559	I3
I560	H10
I561	H10
I562	L5
I563	H16
I564	H16
I565	H16
I566	I16
I568	I6
I569	H10
I570	K5
I571	K5
I572	L5
I573	L5
I574	L3
I575	I3
I576	F12
L311	D4
L503	B6

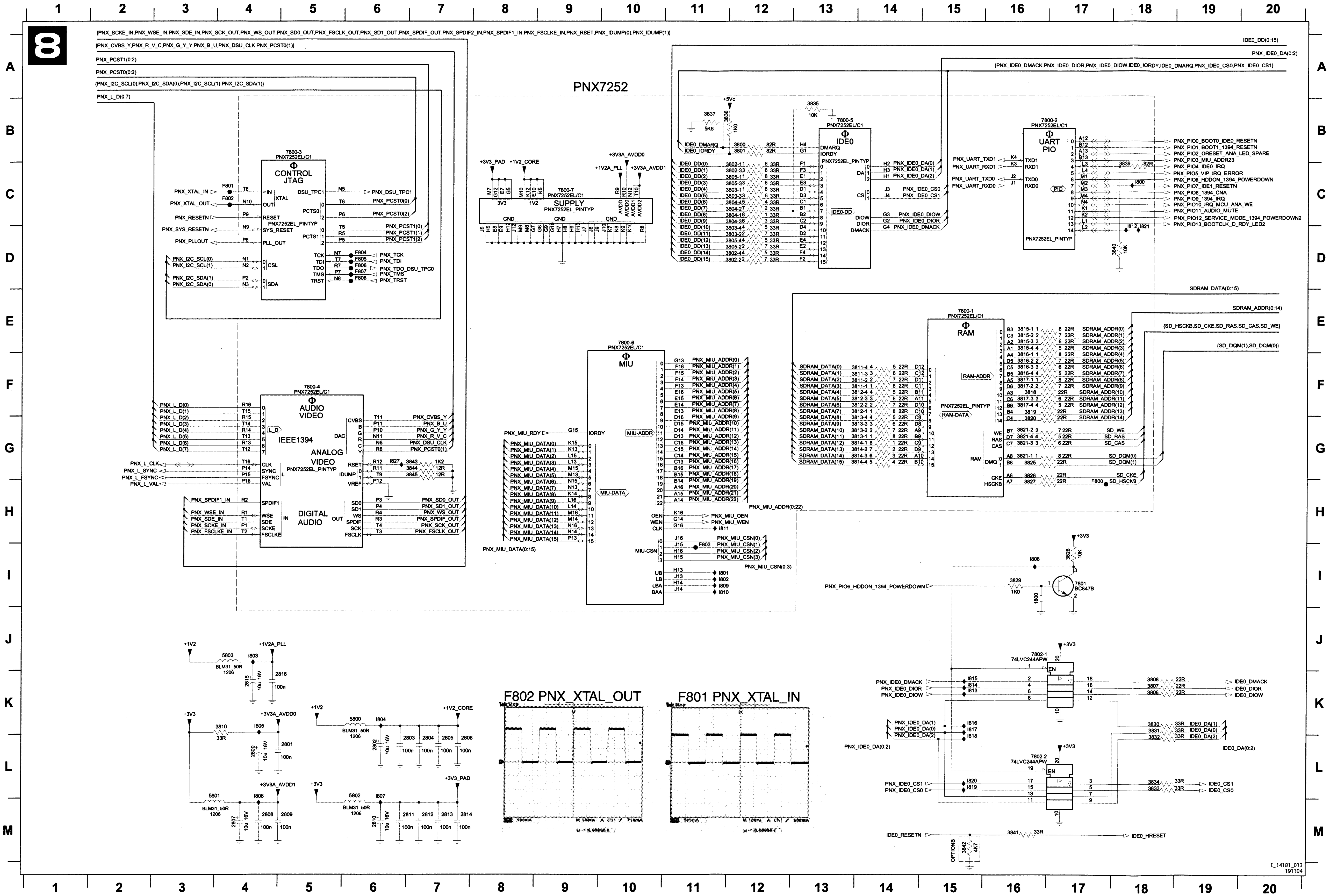
IC 7501-1 XTAL IN I502



IC 7501-1 XTAL OUT I501

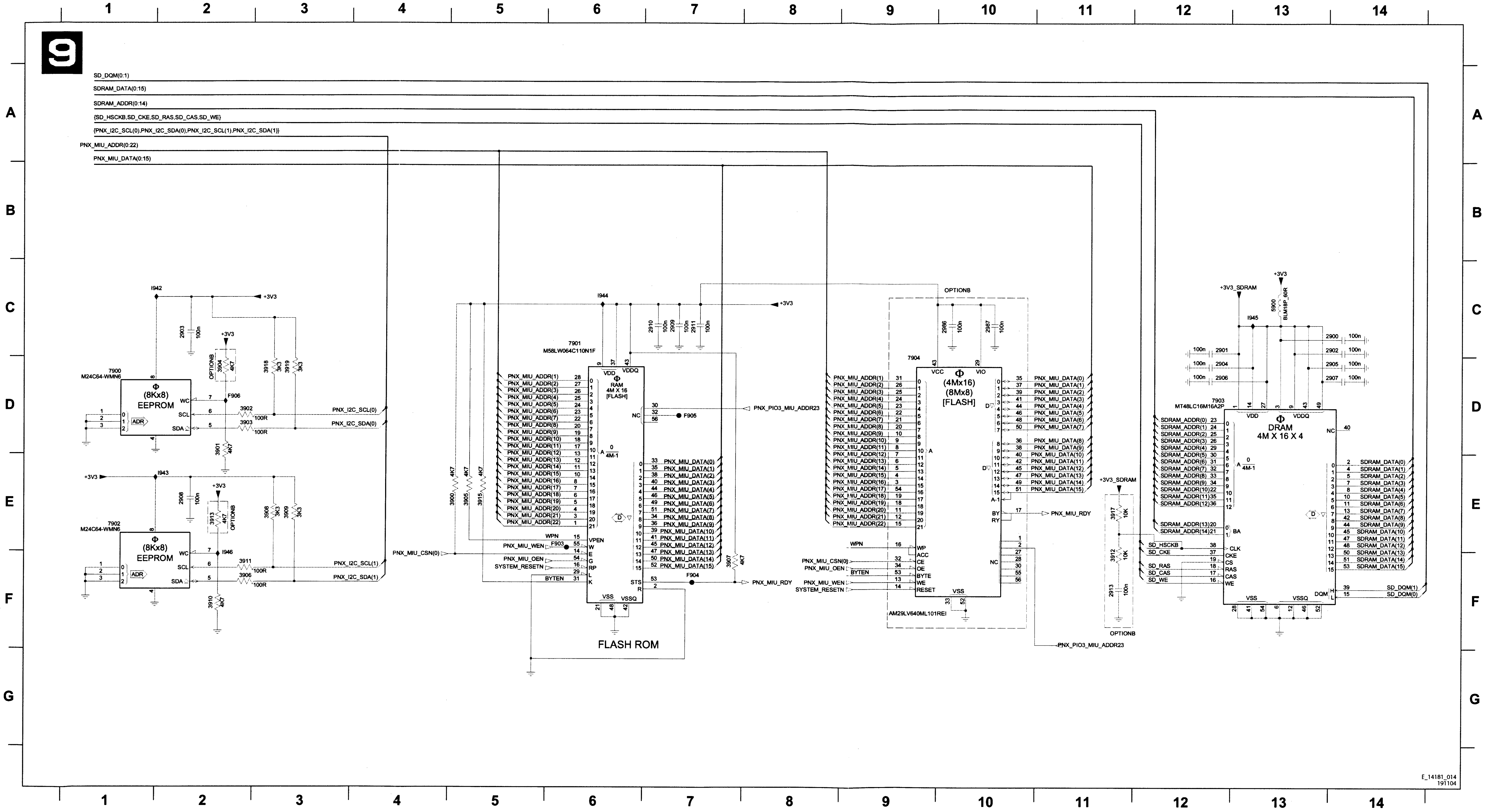


LECO: Be LECO


8
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
A B C D E F G H I J K L M
PNX7252
7800-3 PNX7252EL/C1 CONTROL JTAG
7800-7 PNX7252EL/C1 SUPPLY
7800-5 PNX7252EL/C1 IDE0
7800-2 PNX7252EL/C1 UART PIO
7800-4 PNX7252EL/C1 AUDIO VIDEO IEEE1394 ANALOG VIDEO DIGITAL AUDIO
7800-6 PNX7252EL/C1 MIU
7800-1 PNX7252EL/C1 RAM
7801 BC847B
7802-1 74LVC244APW
7802-2 74LVC244APW
F802 PNX_XTAL_OUT
F801 PNX_XTAL_IN
IDE0_DD(0:15)
IDE0_DA(0:2)
SDRAM_DATA(0:15)
SDRAM_ADDR(0:14)
PNX_MIU_ADDR(0:22)
PNX_MIU_DATA(0:15)
PNX_MIU_CSN(0:3)
PNX_L_D(0:7)
PNX_I2C_SCL(0),PNX_I2C_SDA(0),PNX_I2C_SCL(1),PNX_I2C_SDA(1)
PNX_PIO6_HDDON_1394_POWERDOWN
IDE0_RESETN
IDE0_HRESET
+1V2 +1V2A_PLL +3V3 +3V3A_AVDD0 +3V3A_AVDD1 +1V2_CORE +3V3_PAD +5Vc
E_14181_013 191104

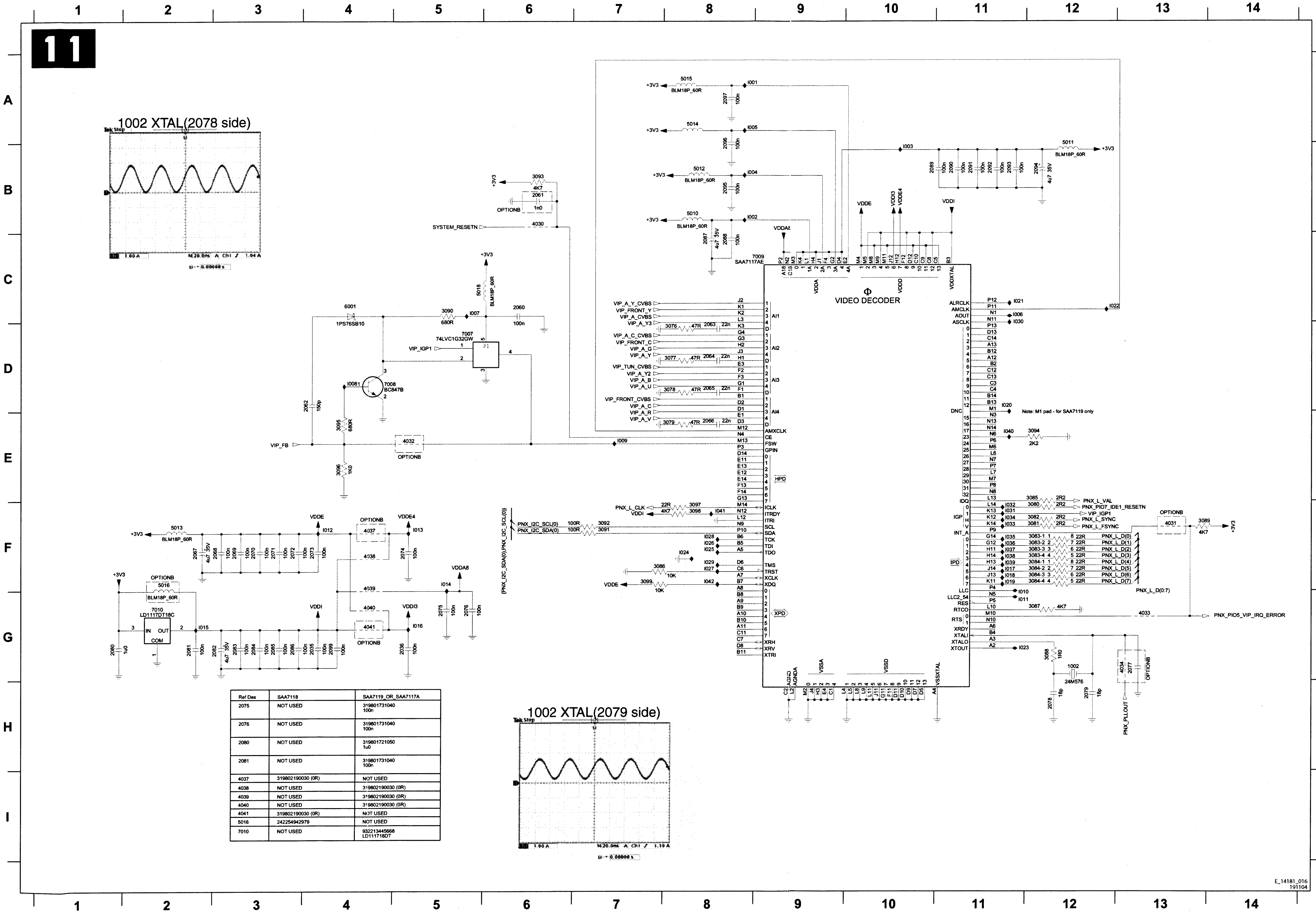
1800	I16
2800	L4
2801	L5
2802	L6
2803	L7
2804	L7
2805	L7
2806	L7
2807	M4
2808	M4
2809	M5
2810	M6
2811	M7
2812	M7
2813	M7
2814	M7
2815	K4
2816	K5
3800	B12
3801	B12
3802-1	C12
3802-2	D12
3802-3	C12
3802-4	D12
3803-1	C12
3803-2	D12
3803-3	C12
3803-4	D12
3804-1	C12
3804-2	C12
3804-3	C12
3804-4	C12
3805-1	C12
3805-2	D12
3805-3	C12
3805-4	D12
3806	K18
3807	K18
3808	K18
3810	K4
3811-1	F14
3811-2	F14
3811-3	F14
3811-4	F14
3812-1	F14
3812-2	F14
3812-3	F14
3812-4	F14
3813-1	G14
3813-2	G14
3813-3	G14
3813-4	G14
3814-1	G14
3814-2	G14
3814-3	G14
3814-4	G14
3815-1	E16
3815-2	E16
3815-3	E16
3815-4	E16
3816-1	F16
3816-2	F16
3816-3	F16
3816-4	F16
3817-1	F16
3817-2	F16
3817-3	F16
3817-4	F16
3818	F16
3819	F16
3820	G16
3821-1	G16
3821-2	G16
3821-3	G16
3821-4	G16
3825	G16
3826	G16
3827	H16
3828	I17
3829	I16
3830	K18
3831	K18
3832	L18
3833	L18
3834	L18
3835	B13
3836	B11
3837	B11
3839	C18
3840	D18
3841	M16
3842	M15
3843	G7
3844	G7
3845	G7
5800	K6
5801	L4
5802	L6
5803	J4
7800-1	E15
7800-2	B17
7800-3	B5
7800-4	F5
7800-5	B13
7800-6	E10
7800-7	C9
7801	I17
7802-1	J17
7802-2	L17
F800	H17
F801	C4
F802	C4
F803	I11
F804	D6
F805	D6
F806	D6
F807	D6
F808	D6
I800	C18
I801	I11
I802	I11
I803	J4
I804	K6
I805	K4
I806	L4
I807	L6
I808	I16
I809	I11
I810	I11
I811	H11
I812	D18
I813	K15
I814	K15
I815	K15
I816	K15
I817	K15
I818	L15
I819	L15
I820	L15
I821	D18
I827	G6

LECO: Be Memory


9
SD_DQM(0:1)
SDRAM_DATA(0:15)
SDRAM_ADDR(0:14)
{SD_HSCKB,SD_CKE,SD_RAS,SD_CAS,SD_WE}
{PNX_I2C_SCL(0),PNX_I2C_SDA(0),PNX_I2C_SCL(1),PNX_I2C_SDA(1)}
PNX_MIU_ADDR(0:22)
PNX_MIU_DATA(0:15)
7900
M24C64-WMN6
(8Kx8)
EEPROM
7902
M24C64-WMN6
(8Kx8)
EEPROM
WC
SCL
SDA
ADR
PNX_I2C_SCL(0)
PNX_I2C_SDA(0)
PNX_I2C_SCL(1)
PNX_I2C_SDA(1)
+3V3
I942
I943
I946
F906
OPTIONB
100R
4K7
3K3
100n
7901
M58LW064C110N1F
RAM
4M X 16
[FLASH]
VDD
VDDQ
VPEN
STS
NC
VSS
VSSQ
I944
F903
F904
F905
WPN
PNX_MIU_WEN
PNX_MIU_OEN
SYSTEM_RESETN
BYTEN
PNX_MIU_CSN(0)
PNX_PIO3_MIU_ADDR23
PNX_MIU_RDY
FLASH ROM
7904
(4Mx16)
(8Mx8)
[FLASH]
VCC
VIO
WP
ACC
CE
OE
BYTE
WE
RESET
VSS
AM29LV640ML101REI
OPTIONB
+3V3_SDRAM
7903
MT48LC16M16A2P
DRAM
4M X 16 X 4
VDD
VDDQ
5900
BLM18P_60R
I945
CLK
CKE
CS
RAS
CAS
WE
BA
DQM
SD_HSCKB
SD_CKE
SD_RAS
SD_CAS
SD_WE
SD_DQM(0)
SD_DQM(1)
E_14181_014
191104

2900	C14
2901	C12
2902	C14
2903	C2
2904	D12
2905	D14
2906	D12
2907	D14
2908	E2
2909	C7
2910	C7
2911	C7
2913	F11
2986	C10
2987	C10
3900	E5
3901	D2
3902	D2
3903	D2
3904	D2
3905	E5
3906	F2
3907	F7
3908	E3
3909	E3
3910	F2
3911	F2
3912	F11
3913	E2
3915	E5
3917	E11
3918	D3
3919	D3
5900	C13
7900	D1
7901	C6
7902	E1
7903	D12
7904	D9
F903	E6
F904	F7
F905	D7
F906	D2
I942	C1
I943	E2
I944	C6
I945	C13
I946	F2

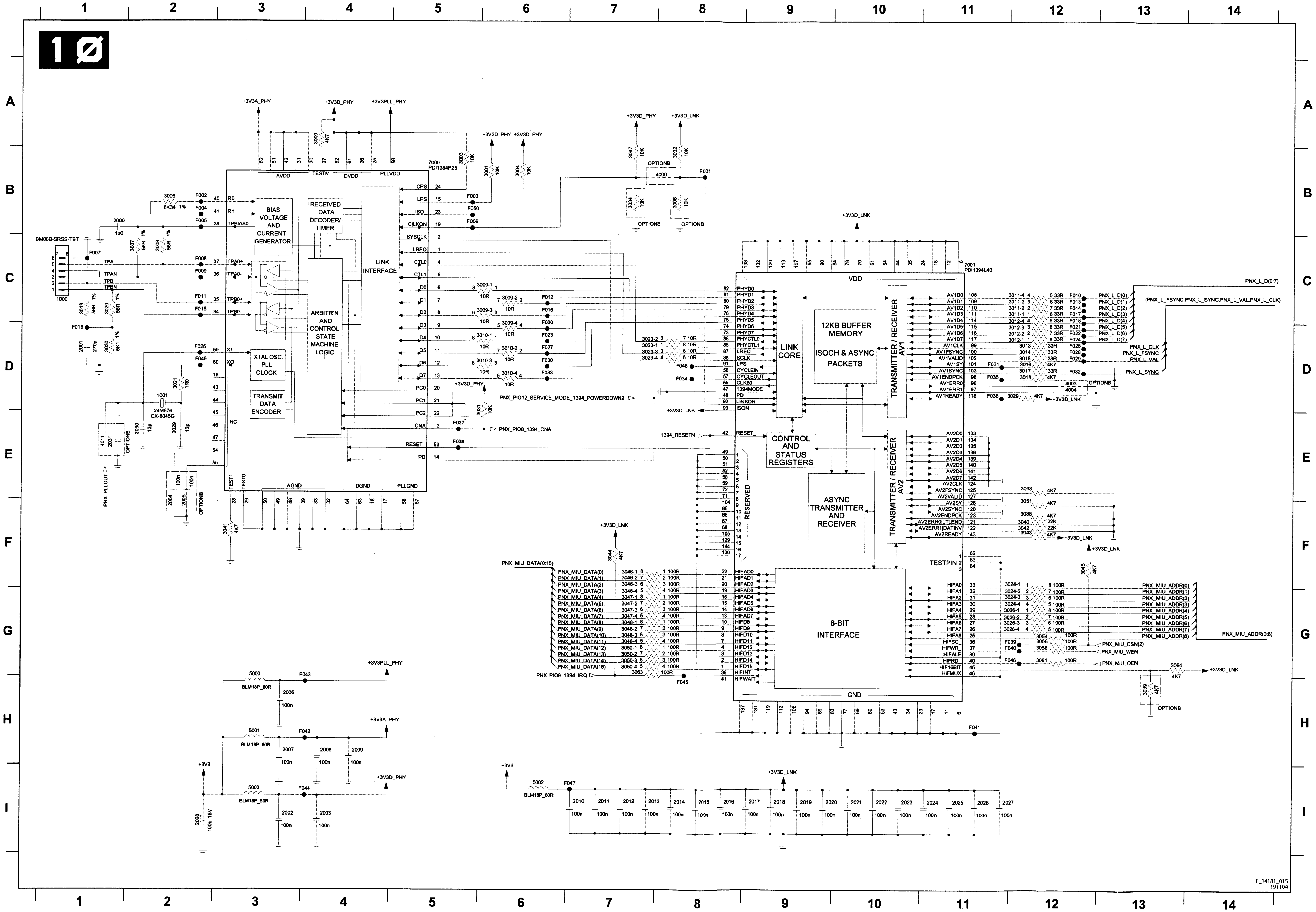
LECO: Be Video In


11
1002 XTAL(2078 side)
1002 XTAL(2079 side)
VIDEO DECODER
7009
SAA7117AE
7007
74LVC1G32GW
7008
BC847B
7010
LD1117DT18C
6001
1PS76SB10
OPTIONB
SYSTEM_RESETN
VIP_IGP1
VIP_FB
VIP_A_Y_CVBS
VIP_FRONT_Y
VIP_A_CVBS
VIP_A_Y3
VIP_A_C_CVBS
VIP_FRONT_C
VIP_A_G
VIP_A_Y
VIP_TUN_CVBS
VIP_A_Y2
VIP_A_B
VIP_A_U
VIP_FRONT_CVBS
VIP_A_C
VIP_A_R
VIP_A_V
PNX_L_CLK
PNX_I2C_SCL(0)
PNX_I2C_SDA(0)
PNX_L_VAL
PNX_PIO7_IDE1_RESETN
VIP_IGP1
PNX_L_SYNC
PNX_L_FSYNC
PNX_L_D(0:7)
PNX_PIO5_VIP_IRQ_ERROR
PNX_PLLOUT
24M576
+3V3
VDDE
VDDA8
VDDI
VDDI3
VDDE4
Note: M1 pad - for SAA7119 only
E_14181_016
191104

Ref Des	SAA7118	SAA7119_OR_SAA7117A
2075	NOT USED	319801731040 100n
2076	NOT USED	319801731040 100n
2080	NOT USED	319801721050 1u0
2081	NOT USED	319801731040 100n
4037	319802190030 (0R)	NOT USED
4038	NOT USED	319802190030 (0R)
4039	NOT USED	319802190030 (0R)
4040	NOT USED	319802190030 (0R)
4041	319802190030 (0R)	NOT USED
5016	242254942979	NOT USED
7010	NOT USED	932213445668 LD111718DT

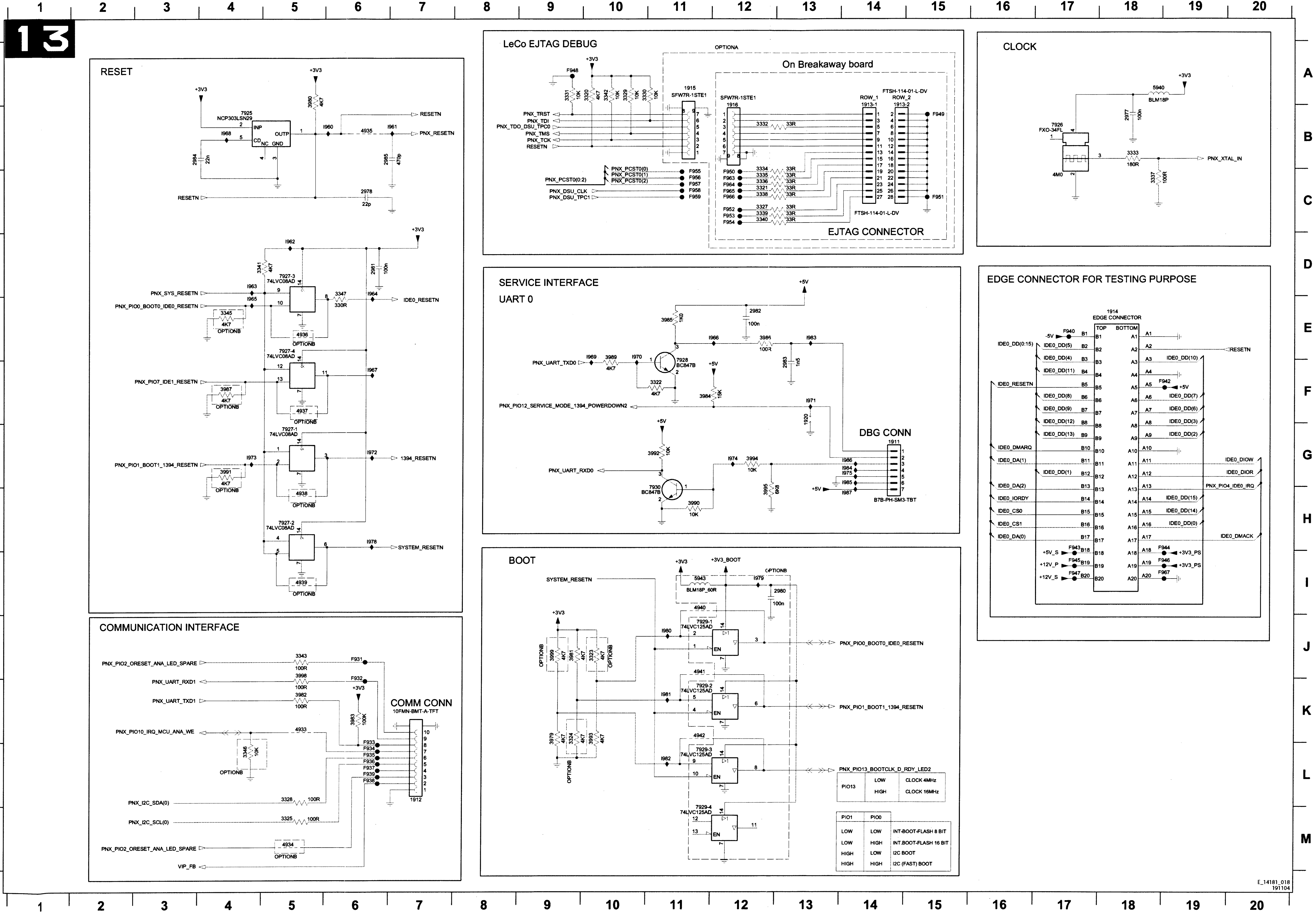
1002	G12
2035	G4
2036	G5
2060	C6
2061	B6
2062	D4
2063	D8
2064	D8
2065	D8
2066	E8
2067	F2
2068	F3
2069	F3
2070	F3
2071	F3
2072	F3
2073	F4
2074	F5
2075	G5
2076	G5
2077	G13
2078	H12
2079	H12
2080	G1
2081	G2
2082	G2
2083	G3
2084	G3
2085	G3
2086	G3
2087	C8
2088	C8
2089	B10
2090	B11
2091	B11
2092	B11
2093	B11
2094	B12
2095	B8
2096	B8
2097	A8
2099	G4
3076	D8
3077	D8
3078	D8
3079	E8
3080	F12
3081	F12
3082	F12
3083-1	F12
3083-2	F12
3083-3	F12
3083-4	F12
3084-1	F12
3084-2	F12
3084-3	F12
3084-4	F12
3085	E12
3086	F7
3087	G12
3088	G12
3089	F13
3090	C5
3091	F7
3092	F7
3093	B6
3094	E12
3095	E4
3096	E4
3097	F8
3098	F8
3099	F7
4030	B6
4031	F13
4032	E5
4033	G13
4034	G13
4037	F4
4038	F4
4039	F4
4040	G4
4041	G4
5010	B8
5011	B12
5012	B8
5013	F2
5014	A8
5015	A8
5016	F2
5018	C5
6001	C4
7007	D5
7008	D4
7009	C9
7010	G2
I001	A8
I002	B8
I003	B10
I004	B8
I005	A8
I006	C11
I007	C5
I008	D4
I009	E7
I010	G11
I011	G11
I012	F4
I013	F5
I014	F5
I015	G2
I016	G5
I017	F11
I018	F11
I019	F11
I020	D11
I021	C11
I022	C12
I023	G11
I024	F8
I025	F8
I026	F8
I027	F8
I028	F8
I029	F8
I030	C11
I031	F11
I032	F11
I033	F11
I034	F11
I035	F11
I036	F11
I037	F11
I038	F11
I039	F11
I040	E11
I041	F8
I042	F8

LECO: Be IEEE 1934


1 Ø
7000
PDI1394P25
AVDD
TESTM
DVDD
PLLVDD
BIAS VOLTAGE AND CURRENT GENERATOR
RECEIVED DATA DECODER/ TIMER
LINK INTERFACE
ARBITR'N AND CONTROL STATE MACHINE LOGIC
XTAL OSC. PLL CLOCK
TRANSMIT DATA ENCODER
AGND
DGND
PLLGND
BM06B-SRSS-TBT
1000
1001
24M576
CX-8045G
+3V3A_PHY
+3V3D_PHY
+3V3PLL_PHY
+3V3D_LNK
+3V3
7001
PDI1394L40
VDD
GND
LINK CORE
12KB BUFFER MEMORY
ISOCH & ASYNC PACKETS
TRANSMITTER / RECEIVER AV1
TRANSMITTER / RECEIVER AV2
CONTROL AND STATUS REGISTERS
ASYNC TRANSMITTER AND RECEIVER
8-BIT INTERFACE
RESERVED
TESTPIN
OPTIONB
PNX_L_D(0:7)
(PNX_L_FSYNC,PNX_L_SYNC,PNX_L_VAL,PNX_L_CLK)
PNX_L_CLK
PNX_L_FSYNC
PNX_L_VAL
PNX_L_SYNC
PNX_MIU_DATA(0:15)
PNX_MIU_ADDR(0:8)
PNX_MIU_CSN(2)
PNX_MIU_WEN
PNX_MIU_OEN
PNX_PIO12_SERVICE_MODE_1394_POWERDOWN2
PNX_PIO8_1394_CNA
PNX_PIO9_1394_IRQ
1394_RESETN
PNX_PLLOUT
BLM18P_60R
E_14181_015
191104

1000	C1
1001	D2
2000	B1
2001	D1
2002	I3
2003	I4
2004	F2
2005	F2
2006	H3
2007	H3
2008	H4
2009	H4
2010	I7
2011	I7
2012	I7
2013	I7
2014	I8
2015	I8
2016	I8
2017	I9
2018	I9
2019	I9
2020	I9
2021	I10
2022	I10
2023	I10
2024	I11
2025	I11
2026	I11
2027	I11
2028	I2
2029	E2
2030	E2
2031	E1
3000	A4
3001	B6
3002	B8
3003	B5
3004	B6
3005	B2
3006	B8
3007	C2
3008	C2
3009-1	C6
3009-2	C6
3009-3	C6
3009-4	D6
3010-1	D6
3010-2	D6
3010-3	D6
3010-4	D6
3011-1	C12
3011-2	C12
3011-3	C12
3011-4	C12
3012-1	D12
3012-2	D12
3012-3	D12
3012-4	C12
3013	D12
3014	D12
3015	D12
3016	D12
3017	D12
3018	D12
3019	C1
3020	C1
3021	D2
3023-1	D7
3023-2	D7
3023-3	D7
3023-4	D7
3024-1	F12
3024-2	G12
3024-3	G12
3024-4	G12
3026-1	G12
3026-2	G12
3026-3	G12
3026-4	G12
3029	D12
3030	D1
3031	D5
3033	E12
3034	B7
3038	F12
3039	H13
3040	F12
3041	F3
3042	F12
3043	F12
3044	F7
3045	F12
3046-1	F7
3046-2	F7
3046-3	F7
3046-4	G7
3047-1	G7
3047-2	G7
3047-3	G7
3047-4	G7
3048-1	G7
3048-2	G7
3048-3	G7
3048-4	G7
3050-1	G7
3050-2	G7
3050-3	G7
3050-4	G7
3051	F12
3054	G12
3056	G12
3058	G12
3061	G12
3063	G7
3064	G13
3067	B7
4000	B8
4003	D12
4004	D12
4011	E1
5000	H3
5001	H3
5002	I6
5003	I3
7000	B5
7001	C11
F001	B8
F002	B2
F003	B5
F004	B2
F005	B2
F006	B5
F007	C1
F008	C2
F009	C2
F010	C12
F011	C2
F012	C6
F013	C12
F014	C12
F015	C2
F016	C6
F017	C12
F018	C12
F019	D1
F020	D6
F021	D12
F022	D12
F023	D6
F024	D12
F025	D12
F026	D2
F027	D6
F028	D12
F029	D12
F030	D6
F031	D11
F032	D12
F033	D6
F034	D8
F035	D11
F036	D11
F037	E5
F038	E5
F039	G12
F040	G12
F041	H11
F042	H4
F043	H4
F044	I4
F045	H8
F046	G12
F047	I7
F048	D8
F049	D2
F050	B5

LECO: Be Periphery

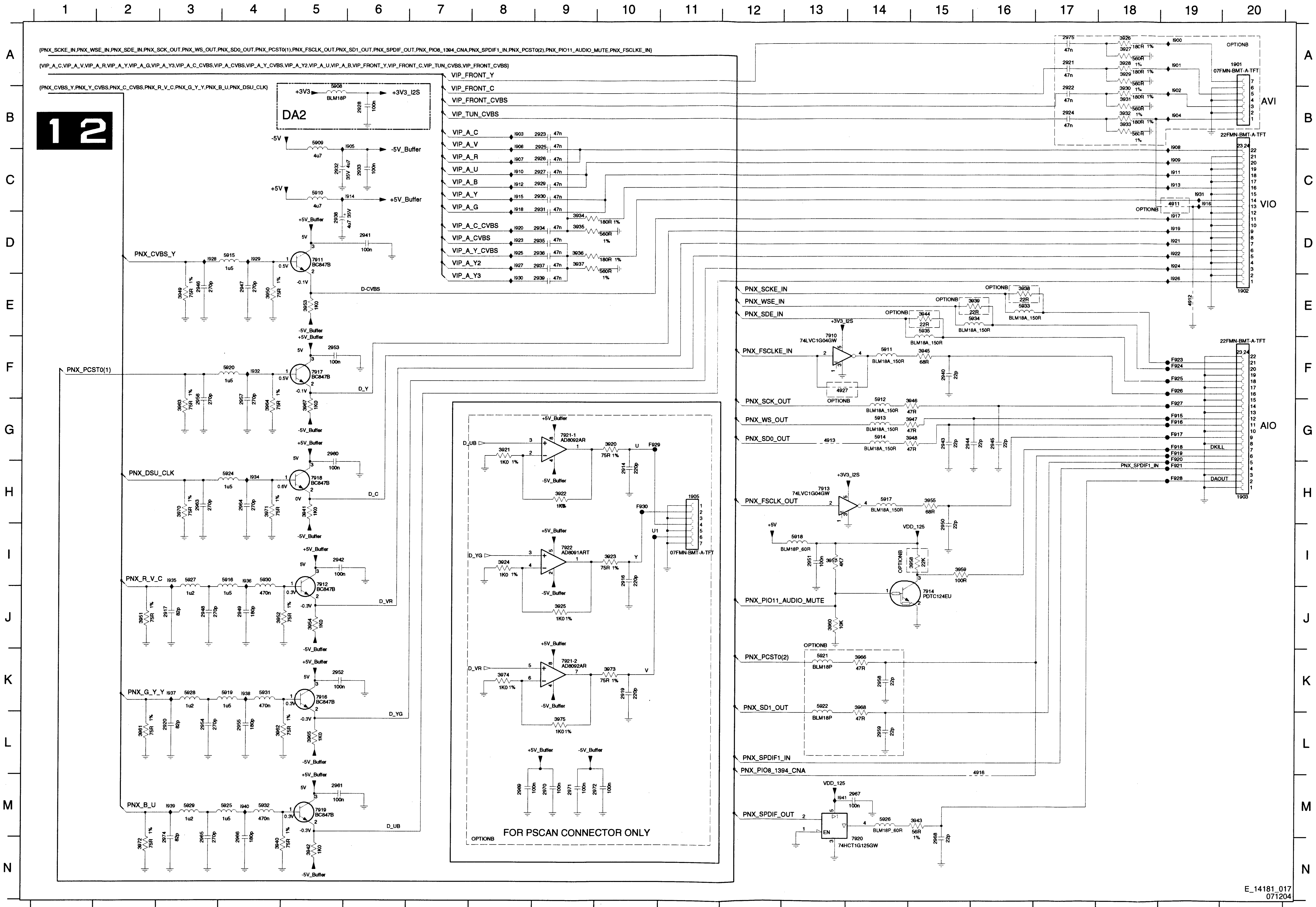

13
RESET
+3V3
7925
NCP303LSN29
INP
OUTP
CD
NC GND
RESETN
PNX_RESETN
PNX_SYS_RESETN
PNX_PIO0_BOOT0_IDE0_RESETN
PNX_PIO7_IDE1_RESETN
PNX_PIO1_BOOT1_1394_RESETN
7927-3 74LVC08AD
7927-4 74LVC08AD
7927-1 74LVC08AD
7927-2 74LVC08AD
IDE0_RESETN
1394_RESETN
SYSTEM_RESETN
OPTIONB
COMMUNICATION INTERFACE
PNX_PIO2_ORESET_ANA_LED_SPARE
PNX_UART_RXD1
PNX_UART_TXD1
PNX_PIO10_IRQ_MCU_ANA_WE
PNX_I2C_SDA(0)
PNX_I2C_SCL(0)
VIP_FB
COMM CONN
10FMN-BMT-A-TFT
1912
LeCo EJTAG DEBUG
OPTIONA
On Breakaway board
1915 SFW7R-1STE1
1916 SFW7R-1STE1
FTSH-114-01-L-DV
ROW_1 1913-1
ROW_2 1913-2
PNX_TRST
PNX_TDI
PNX_TDO_DSU_TPC0
PNX_TMS
PNX_TCK
RESETN
PNX_PCST0(0:2)
PNX_PCST0(0)
PNX_PCST0(1)
PNX_PCST0(2)
PNX_DSU_CLK
PNX_DSU_TPC1
EJTAG CONNECTOR
SERVICE INTERFACE
UART 0
+5V
PNX_UART_TXD0
PNX_UART_RXD0
7928 BC847B
7930 BC847B
PNX_PIO12_SERVICE_MODE_1394_POWERDOWN2
DBG CONN
1911
B7B-PH-SM3-TBT
BOOT
SYSTEM_RESETN
+3V3_BOOT
5943 BLM18P_60R
7929-1 74LVC125AD
7929-2 74LVC125AD
7929-3 74LVC125AD
7929-4 74LVC125AD
EN
PNX_PIO0_BOOT0_IDE0_RESETN
PNX_PIO1_BOOT1_1394_RESETN
PNX_PIO13_BOOTCLK_D_RDY_LED2
CLOCK
5940 BLM18P
7926 FXO-34FL
4M0
PNX_XTAL_IN
EDGE CONNECTOR FOR TESTING PURPOSE
1914 EDGE CONNECTOR
TOP
BOTTOM
IDE0_DD(0:15)
IDE0_RESETN
IDE0_DMARQ
IDE0_DA(1)
IDE0_DA(2)
IDE0_IORDY
IDE0_CS0
IDE0_CS1
IDE0_DA(0)
IDE0_DIOW
IDE0_DIOR
PNX_PIO4_IDE0_IRQ
IDE0_DMACK
+3V3_PS
+5V_S
+12V_P
+12V_S
E_14181_018
191104

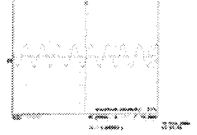
PIO13	LOW	CLOCK 4MHz
	HIGH	CLOCK 16MHz

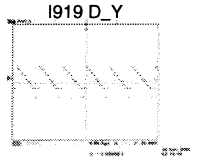
PIO1	PIO0	
LOW	LOW	INT-BOOT-FLASH 8 BIT
LOW	HIGH	INT.BOOT-FLASH 16 BIT
HIGH	LOW	I2C BOOT
HIGH	HIGH	I2C (FAST) BOOT

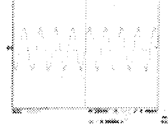
1911	G14
1912	L7
1913-1	B14
1913-2	B14
1914	E18
1915	A11
1916	B12
1920	F13
2977	B18
2978	C6
2980	I13
2981	D6
2982	E12
2983	F13
2984	B3
2985	B6
3320	A10
3321	C12
3322	F11
3323	J10
3324	K9
3325	M5
3327	C12
3328	L5
3329	A10
3330	A10
3331	A9
3332	B12
3333	B18
3334	C12
3335	C12
3336	C12
3337	C18
3338	C12
3339	C12
3340	C12
3341	D4
3342	A10
3343	J5
3345	E4
3346	L4
3347	D6
3979	K9
3980	A5
3981	J9
3982	K5
3983	K6
3984	F11
3985	E11
3986	E12
3987	F4
3989	E10
3990	H11
3991	G4
3992	G11
3993	K10
3994	G12
3995	H12
3998	J5
3999	J9
4933	K5
4934	M5
4935	B6
4936	E5
4937	F5
4938	H5
4939	I5
4940	I11
4941	J11
4942	K11
5940	A18
5943	I11
7925	B4
7926	B17
7927-1	G5
7927-2	H5
7927-3	D5
7927-4	E5
7928	F11
7929-1	J12
7929-2	K12
7929-3	L12
7929-4	M12
7930	H11
F931	J6
F932	K6
F933	L6
F934	L6
F935	L6
F936	L6
F937	L6
F938	L6
F939	L6
F940	E17
F942	F19
F943	H17
F944	H19
F945	I17
F946	I19
F947	I17
F948	A9
F949	B15
F950	C12
F951	C15
F952	C12
F953	C12
F954	C12
F955	C11
F956	C11
F957	C11
F958	C11
F959	C11
F963	C12
F964	C12
F965	C12
F966	C12
F967	I19
I960	B6
I961	B7
I962	D5
I963	D4
I964	D6
I965	E4
I966	E12
I967	F6
I968	B4
I969	E10
I970	E10
I971	F13
I972	G6
I973	G4
I974	G12
I975	G14
I978	H6
I979	I12
I980	J11
I981	K11
I982	L11
I983	E13
I984	G14
I985	G14
I986	G14
I987	H14

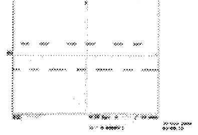
LECO: Be Audio/Video Out

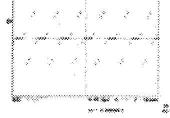

12
DA2
+3V3
5908
BLM18P
+3V3_I2S
2928
100n
-5V
5909
4u7
I905
-5V_Buffer
+5V
5910
I914
+5V_Buffer
VIP_FRONT_Y
VIP_FRONT_C
VIP_FRONT_CVBS
VIP_TUN_CVBS
VIP_A_C
VIP_A_V
VIP_A_R
VIP_A_U
VIP_A_B
VIP_A_Y
VIP_A_G
VIP_A_C_CVBS
VIP_A_CVBS
VIP_A_Y_CVBS
VIP_A_Y2
VIP_A_Y3
PNX_CVBS_Y
PNX_PCST0(1)
PNX_DSU_CLK
PNX_R_V_C
PNX_G_Y_Y
PNX_B_U
7911 BC847B
7917 BC847B
7918 BC847B
7912 BC847B
7916 BC847B
7919 BC847B
D-CVBS
D_Y
D_C
D_VR
D_YG
D_UB
7921-1 AD8092AR
7922 AD8091ART
7921-2 AD8092AR
1905
07FMN-BMT-A-TFT
F929
F930
U1
FOR PSCAN CONNECTOR ONLY
OPTIONB
PNX_SCKE_IN
PNX_WSE_IN
PNX_SDE_IN
PNX_FSCLKE_IN
7910 74LVC1G04GW
4927
PNX_SCK_OUT
PNX_WS_OUT
PNX_SD0_OUT
PNX_FSCLK_OUT
7913 74LVC1G04GW
PNX_PIO11_AUDIO_MUTE
7914 PDTC124EU
PNX_PCST0(2)
PNX_SD1_OUT
PNX_SPDIF1_IN
PNX_PIO8_1394_CNA
4916
PNX_SPDIF_OUT
7920 74HCT1G125GW
VDD_125
AVI
1901
07FMN-BMT-A-TFT
VIO
22FMN-BMT-A-TFT
1902
AIO
1903
DKILL
DAOUT
PNX_SPDIF1_IN
E_14181_017
071204

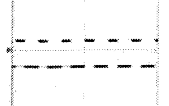

I917 D_CVBS

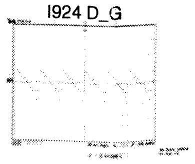

I919 D_Y

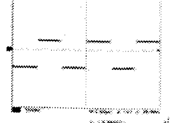

I921 D_C

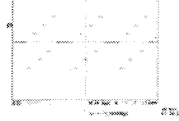

I922 D_V

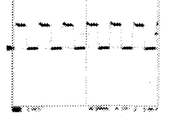

I922 D_R

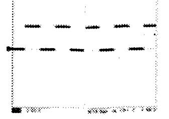

I922D_Y

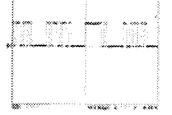

I924 D_G

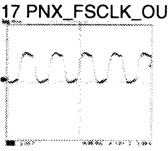

I926 D_U


I926D_B


F927 PNX_SCK_OUT

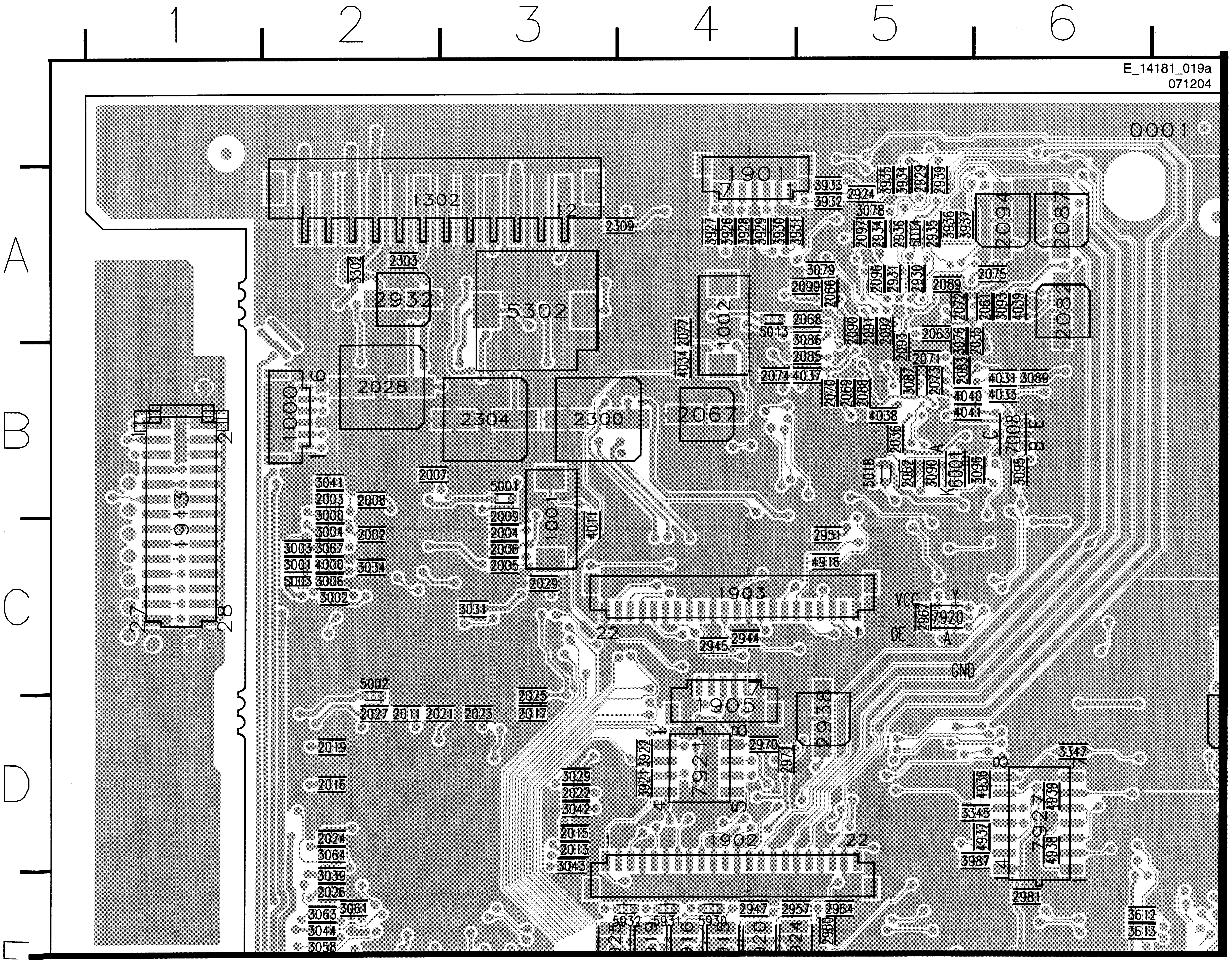

F915 PNX_WS_OUT


F916 PNX_SDO_OUT


F917 PNX_FSCLK_OUT

U1	I10
1901	A20
1902	E20
1903	H20
1905	H11
2914	H10
2916	I10
2917	J3
2919	K10
2920	L3
2921	A17
2922	B17
2923	B9
2924	B17
2925	B9
2926	C9
2927	C9
2928	B6
2929	C9
2930	C9
2931	C9
2932	C5
2933	C6
2934	D9
2935	D9
2936	D9
2937	D9
2938	D5
2939	E9
2940	F15
2941	D6
2942	I5
2943	G15
2944	G15
2945	G16
2946	E3
2947	E4
2948	J3
2949	J4
2950	I15
2951	I13
2952	K5
2953	F5
2954	L3
2955	L4
2956	G3
2957	G4
2958	K14
2959	L14
2960	G5
2961	M5
2963	H3
2964	H4
2965	N3
2966	N4
2967	M14
2968	N15
2969	M8
2970	M9
2971	M9
2972	M9
2974	N3
2975	A17
3920	G10
3921	G8
3922	H9
3923	I10
3924	I8
3925	J9
3926	A18
3927	A18
3928	A18
3929	A18
3930	B18
3931	B18
3932	B18
3933	B18
3934	D9
3935	D9
3936	D9
3937	D9
3938	E16
3939	E16
3940	N4
3941	H5
3942	N5
3943	M15
3944	E15
3945	F15
3946	G15
3947	G15
3948	G15
3949	E3
3950	E4
3951	J2
3952	J4
3953	E5
3954	J5
3955	H15
3957	I13
3958	I15
3959	I15
3960	J13
3961	L2
3962	L4
3963	G3
3964	G4
3965	L5
3966	K14
3967	G5
3968	K14
3970	H3
3971	H4
3972	N2
3973	K10
3974	K8
3975	L9
4911	C19
4912	E19
4913	G13
4916	L16
4927	F13
5908	B5
5909	B5
5910	C5
5911	F14
5912	G14
5913	G14
5914	G14
5915	D4
5916	I4
5917	H14
5918	I13
5919	K4
5920	F4
5921	K13
5922	K13
5924	H4
5925	M4
5926	M14
5927	I3
5928	K3
5929	M3
5930	I4
5931	K4
5932	M4
5933	E16
5934	E16
5935	E15
7910	F13
7911	D5
7912	J5
7913	H13
7914	J15
7916	K5
7917	F5
7918	H5
7919	M5
7920	N14
7921-1	G9
7921-2	K9
7922	I9
F915	G19
F916	G19
F917	G19
F918	G19
F919	G19
F920	G19
F921	H19
F923	F19
F924	F19
F925	F19
F926	F19
F927	G19
F928	H19
F929	G10
F930	H10
I900	A19
I901	A19
I902	B19
I903	B8
I904	B19
I905	B6
I906	B8
I907	C8
I908	B19
I909	C19
I910	C8
I911	C19
I912	C8
I913	C19
I914	C6
I915	C8
I916	C19
I917	D19
I918	C8
I919	D19
I920	D8
I921	D19
I922	D19
I923	D8
I924	D19
I925	D8
I926	E19
I927	D8
I928	D3
I929	D4
I930	E8
I931	C19
I932	F4
I934	H4
I935	I3
I936	I4
I937	K3
I938	K4
I939	M3
I940	M4
I941	M13

Layout: LECO Top View Part 1


1
2
3
4
5
6
A
B
C
D
E
E_14181_019a
071204
0001
1302
1901
1913
1000
1002
1001
1903
1905
1902
2028
2304
2300
2067
2932
5302
2094
2087
2082
7008
7920
7921
7927
6001
2938
2309
2303
3302
3933
3932
2924
3078
3079
2099
2066
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Layout: LECO Top Overview

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1001	C3	1901	A4	1920	G1	2009	B3	2017	D3	2025	D3	2062	B5	2072	A5	2086	B5	2096	A5	2211	F10	2304	B3	2323	A7	2422	B12	2502	F8	2520	E7	2528	F8
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1100	E10	1903	C4	2003	B2	2011	D2	2019	D2	2027	D2	2066	A5	2074	B4	2089	A5	2099	A5	2216	F11	2314	A7	2325	B7	2439	G12	2514	D7	2522	F7	2530	F8
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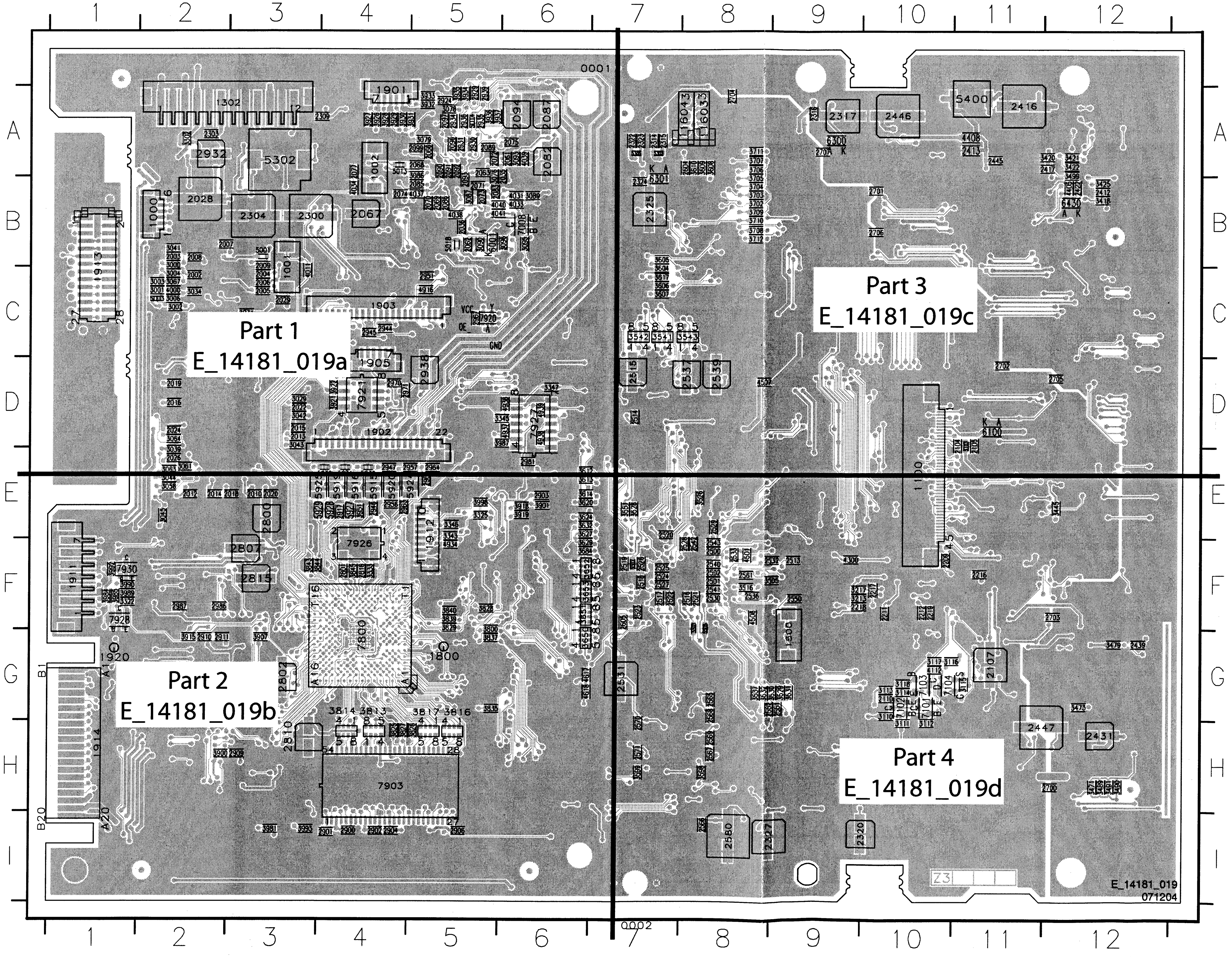
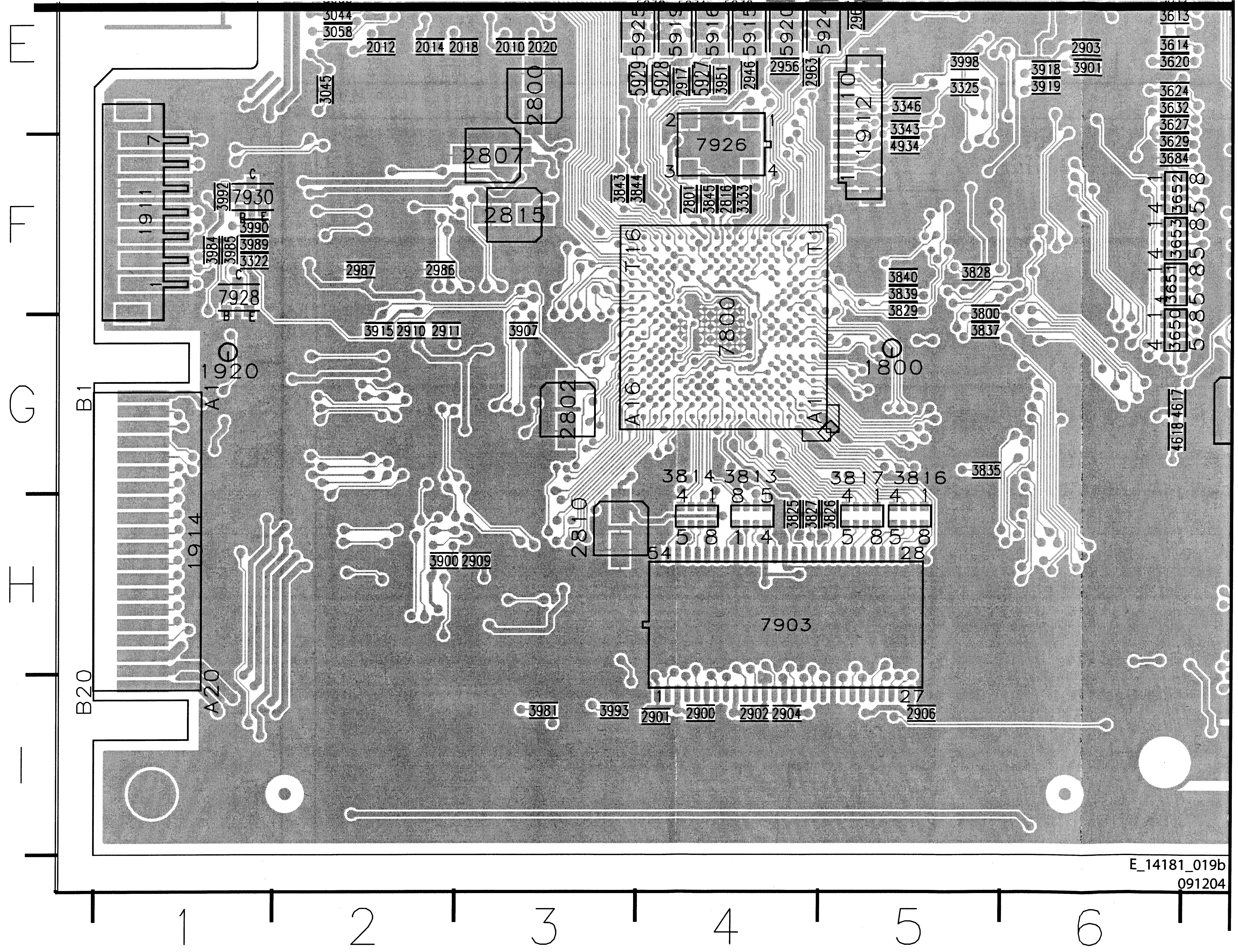


Layout: LECO Top View Part 2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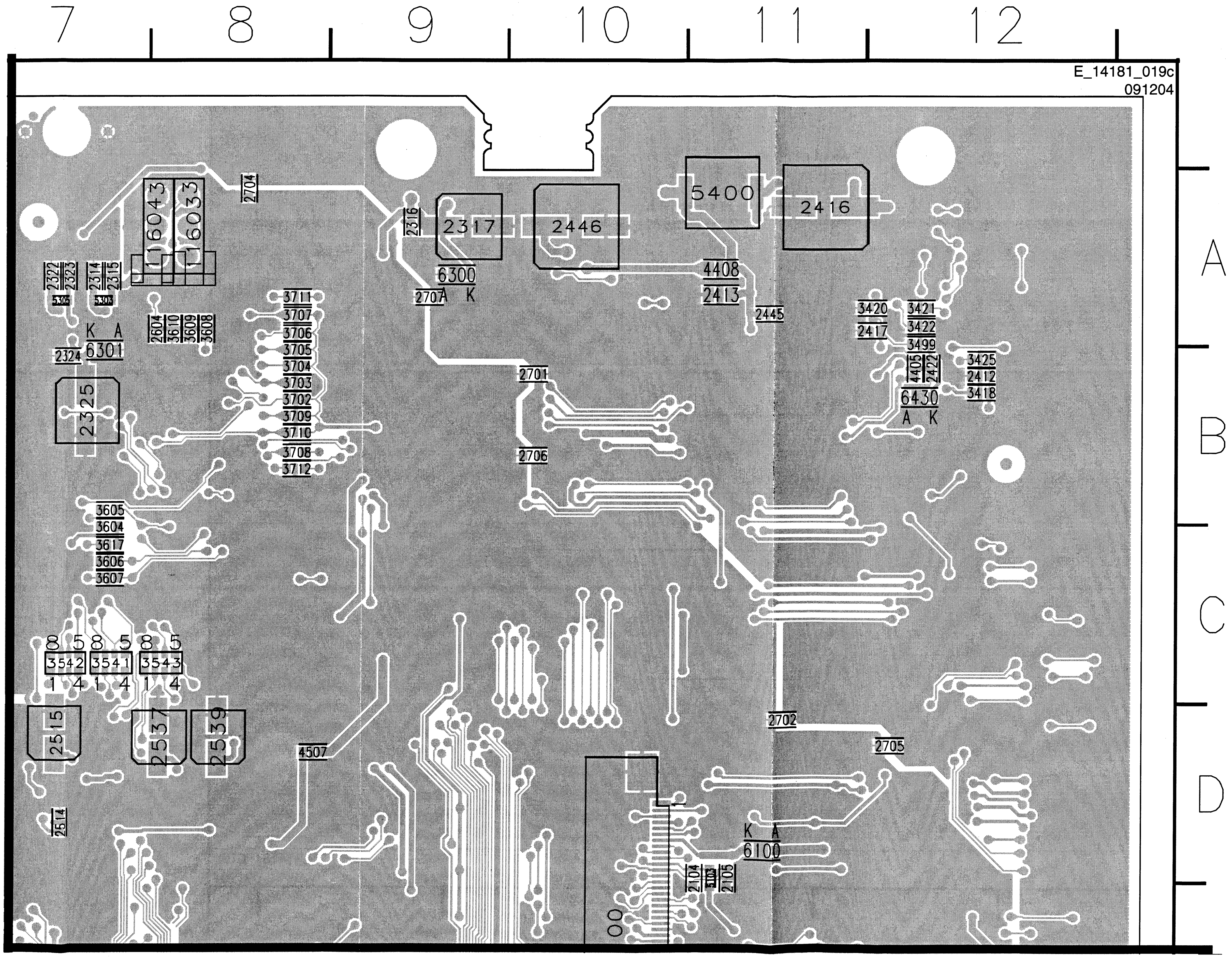
Layout: LECO Top View Part 3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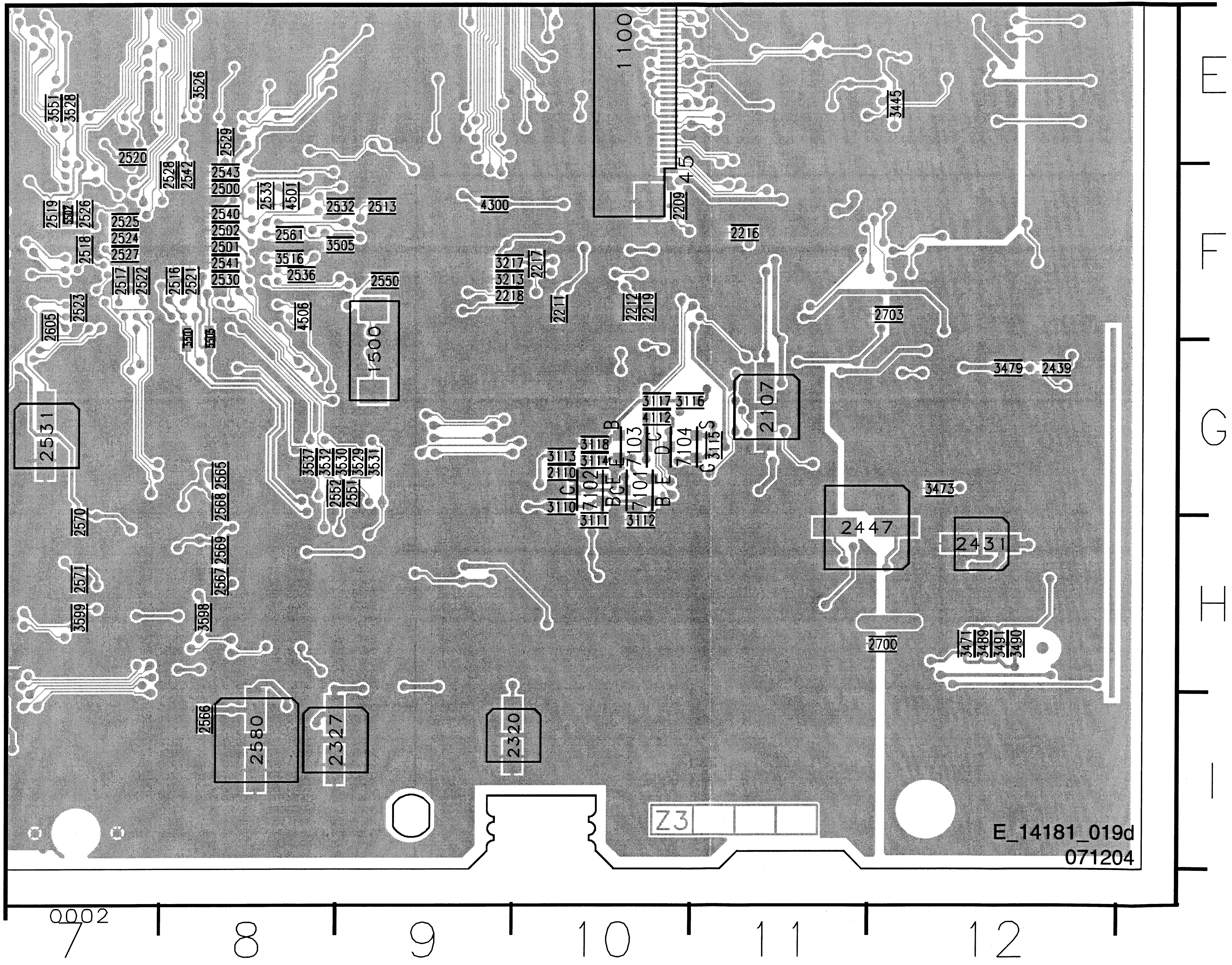
Layout: LECO Top View Part4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Layout: LECO Bottom View

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1303	A11
1304	A10
1305	A6
1306	A6
1400	A4
1401	A1
1700	C5
1702	C1
1703	A5
1915	D7
1916	D12
2000	B11
2001	B11
2030	B10
2031	B10
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2065	A8
2076	A7
2078	A9
2079	B9
2080	B6
2081	A7
2084	A7
2088	A7
2095	A7
2100	E3
2101	D3
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2103	F2
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2109	D2
2210	F4
2213	F4
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2228	F4
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2302	A11
2305	A10
2306	A10
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2308	A10
2310	A10
2318	H3
2319	H3
2321	H3
2326	I5
2328	I4
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2406	H2
2407	C1
2411	A2
2414	B1
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2421	H2
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2441	E1
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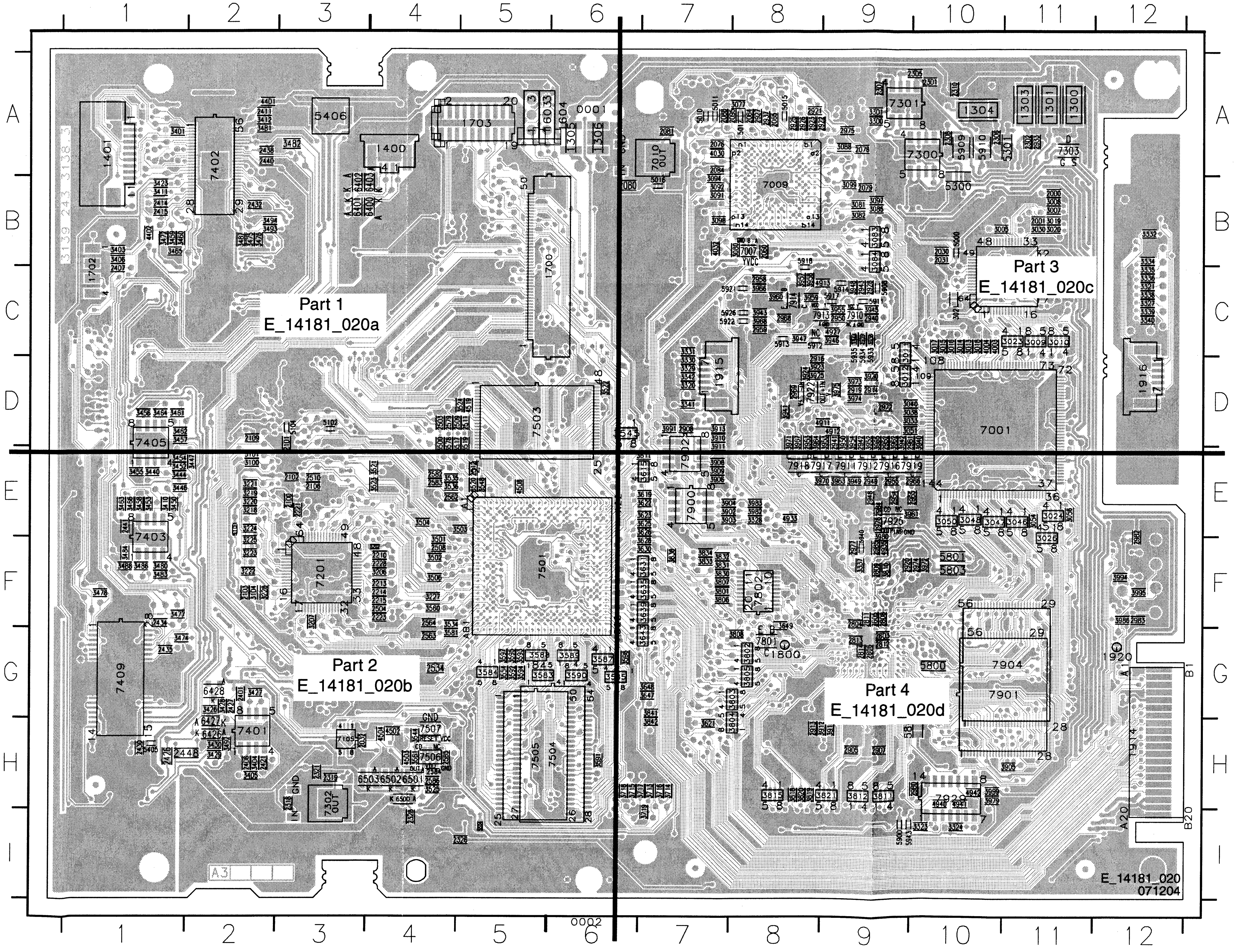
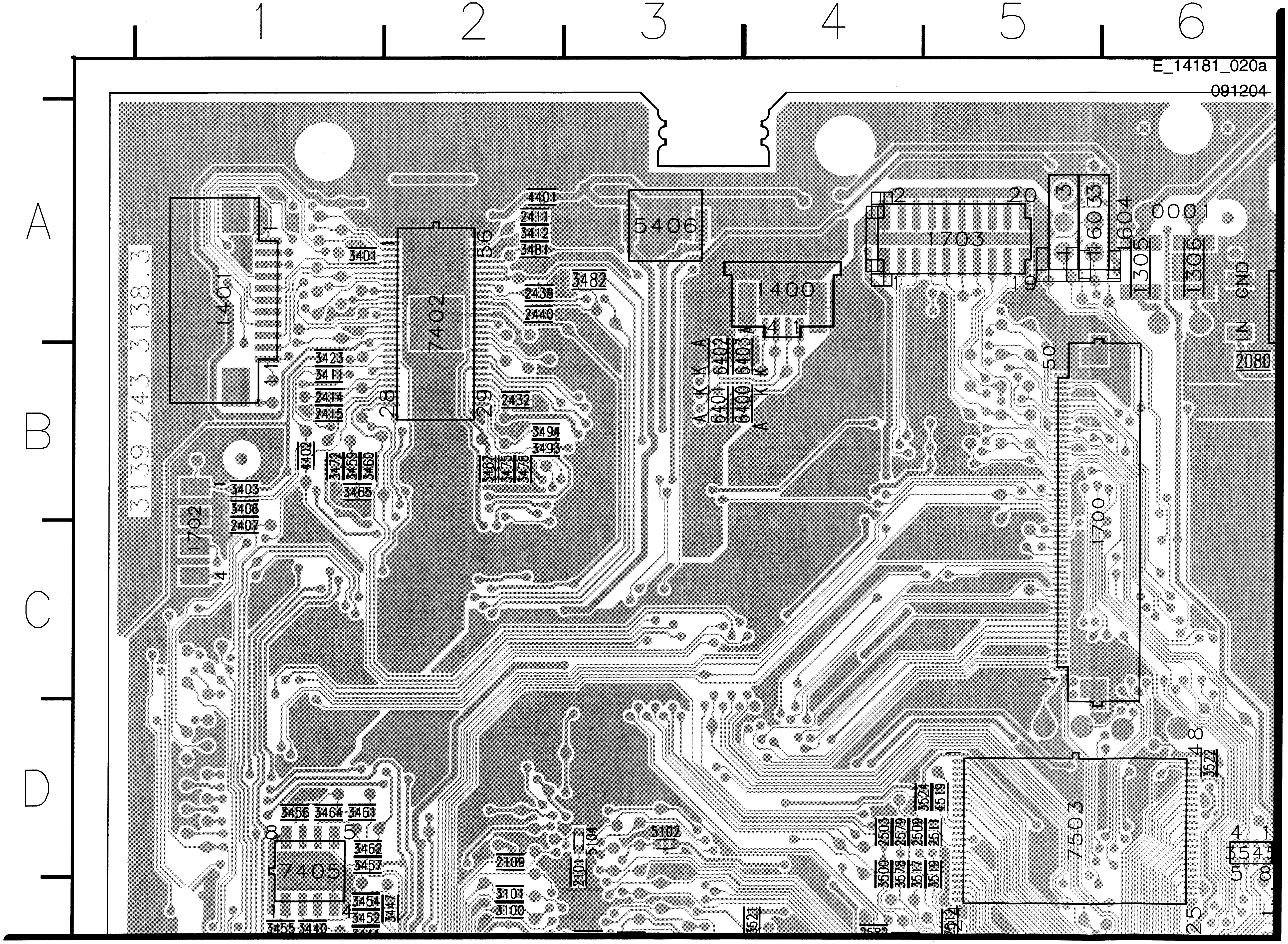
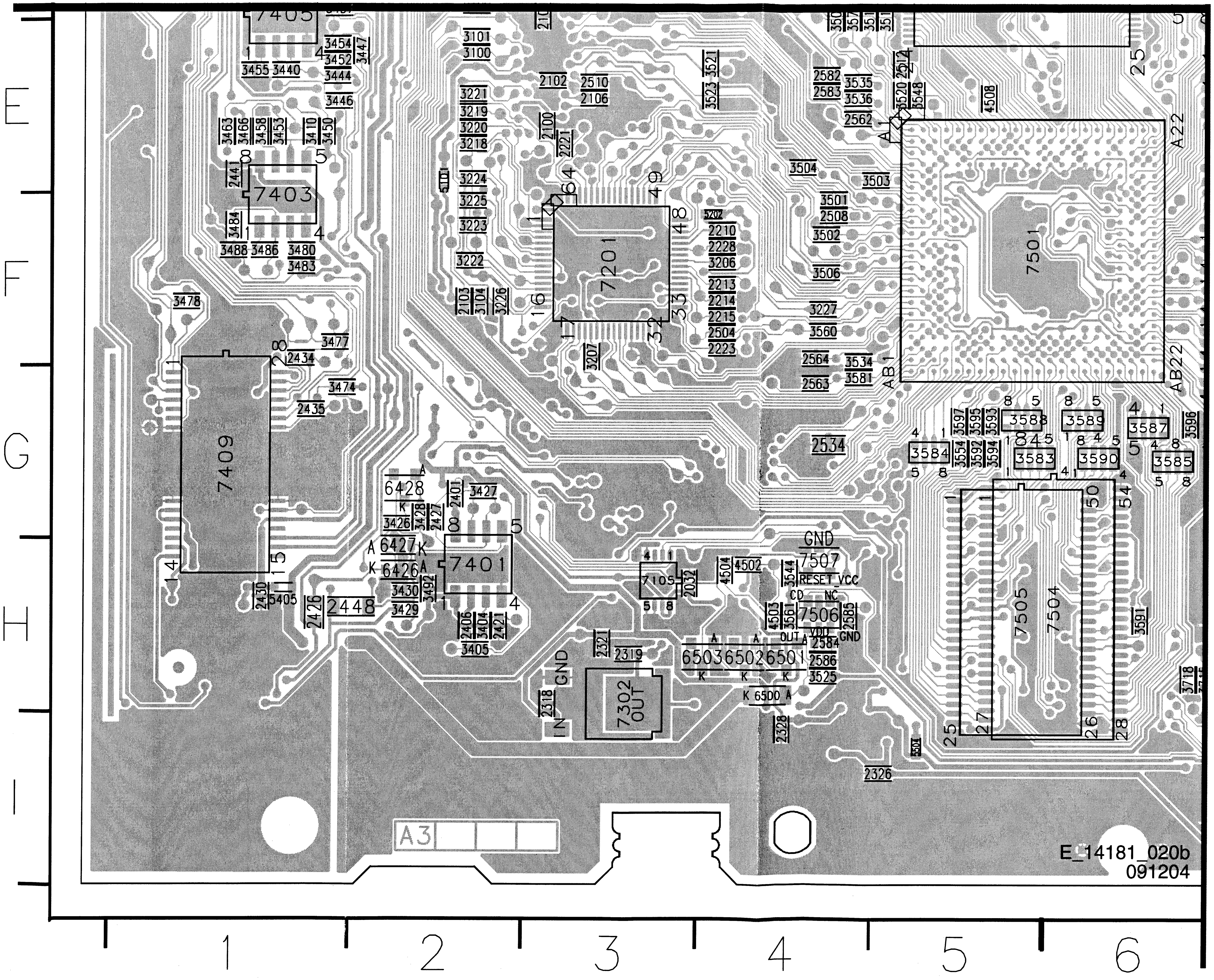
6401	B3
6402	B3
6403	B3
6426	H2
6427	H2
6428	G2
6500	H4
6501	H4
6502	H4
6503	H4
7000	C11
7001	D10
7007	B8
7009	B8
7010	A7
7105	H3
7201	F3
7300	A10
7301	A9
7302	H3
7303	A11
7401	H2
7402	A2
7403	F1
7405	D1
7409	G1
7501	F5
7503	D5
7504	H6
7505	H5
7506	H4
7507	H4
7801	G8
7802	F8
7900	E7
7901	G11
7902	E7
7904	G11
7910	C9
7911	E9
7912	E9
7913	C8
7914	C8
7916	E9
7917	E8
7918	E8
7919	E10
7922	D8
7925	E9
7929	H10



Layout: LECO Bottom View Part 1


1
2
3
4
5
6
A
B
C
D
E_14181_020a
091204
3139 243 3138.3
1401
7402
56
28
29
3401
4401
2411
3412
3481
2438
2440
3482
5406
1400
1703
2
20
19
3
1604
6033
0001
1305
1306
GND
N
2080
6402
6403
6401
6400
A
K
3423
3411
2414
2415
2432
3494
3493
4402
3472
3459
3460
3465
3487
3475
3476
1702
3403
3406
2407
1700
50
48
25
3522
7503
3524
4519
2503
2579
2509
2511
3500
3578
3517
3519
3545
3456
3464
3461
7405
8
5
3462
3457
3454
3452
3447
3455
3440
2109
3101
3100
2101
5104
5102
3521
2582
2514

Layout: LECO Bottom View Part 2


E
F
G
H
I
1
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3
4
5
6
7405
3454
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3446
3463
3466
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3453
3410
3450
2441
7403
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3486
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3483
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3477
2434
3474
2435
7409
2430
5405
2426
2448
6428
3426
3428
2427
2401
3427
6427
6426
7401
3430
3429
3492
2406
3404
2421
3405
3101
3100
3221
3219
3220
3218
3224
3225
3223
3222
2103
3104
3226
2102
2510
2106
2100
2221
7201
3207
3202
2210
2228
3206
2213
2214
2215
2504
2223
3523
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2583
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3536
2562
3520
3548
2514
4508
3504
3503
3501
2508
3502
3506
3227
3560
2564
2563
3534
3581
7501
A1
A22
AB1
AB22
3597
3595
3593
3588
3589
3587
3596
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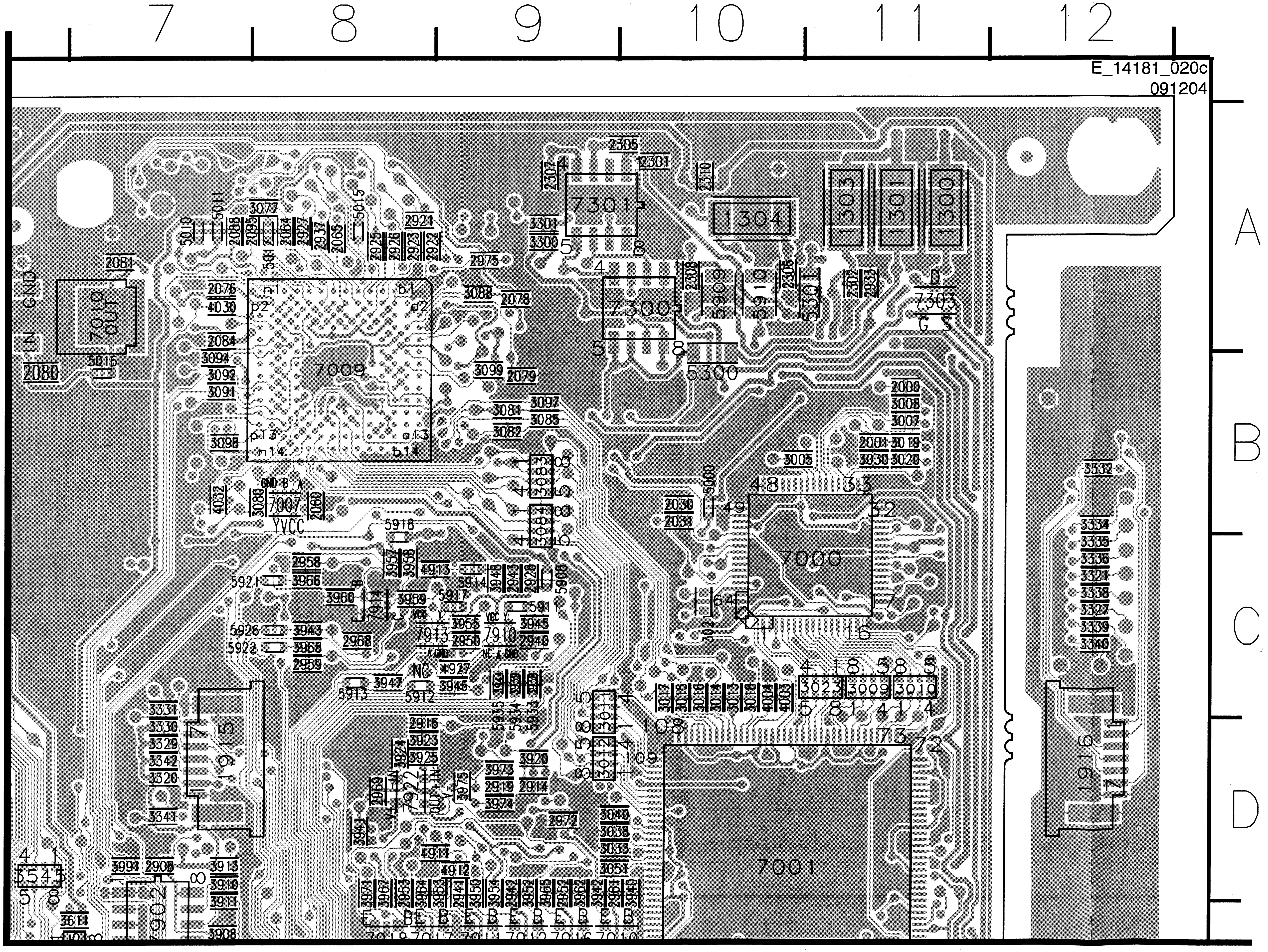
3554
3592
3594
3583
3590
3585
2534
7505
7504
3591
3718
7105
2032
4504
4502
3544
GND
7507
RESET
VCC
CD
NC
7506
4503
3561
2585
OUT
VDD
2584
2586
3525
6503
6502
6501
6500
2321
2319
2318
7302
OUT
IN
2328
2326
A3
E_14181_020b
091204

Layout: LECO Bottom View Part 3


7
8
9
10
11
12
A
B
C
D
E_14181_020c
091204
7009
7000
7001
7300
7301
7303
1300
1301
1303
1304
1915
1916
7010 OUT
GND
IN
2080
2081
5016
5010
5011
2088
2095
5017
3077
2064
2927
2937
2065
5015
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2922
2921
2975
3088
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2076
4030
2084
3094
3092
3091
3098
3099
2079
3081
3082
3097
3085
3083
3084
2305
2301
2307
2310
3301
3300
2308
5909
5910
2306
5301
2302
2933
5300
2000
3008
3007
2001
3019
3030
3020
3005
3332
3334
3335
3336
3321
3338
3327
3339
3340
4032
3080
7007
2060
YVCC
5918
2958
3966
5921
3957
3958
4913
5914
3948
2943
2928
5908
3960
7914
3959
5917
5911
7913
3955
2950
7910
3945
2940
5926
3943
5922
3968
2959
2968
NC
4927
3946
3947
5913
5912
2030
2031
5000
3023
3009
3010
3017
3015
3016
3014
3013
3018
4004
4003
3011
3012
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3329
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3991
2908
7902
3913
3910
3911
3908
3611
3971
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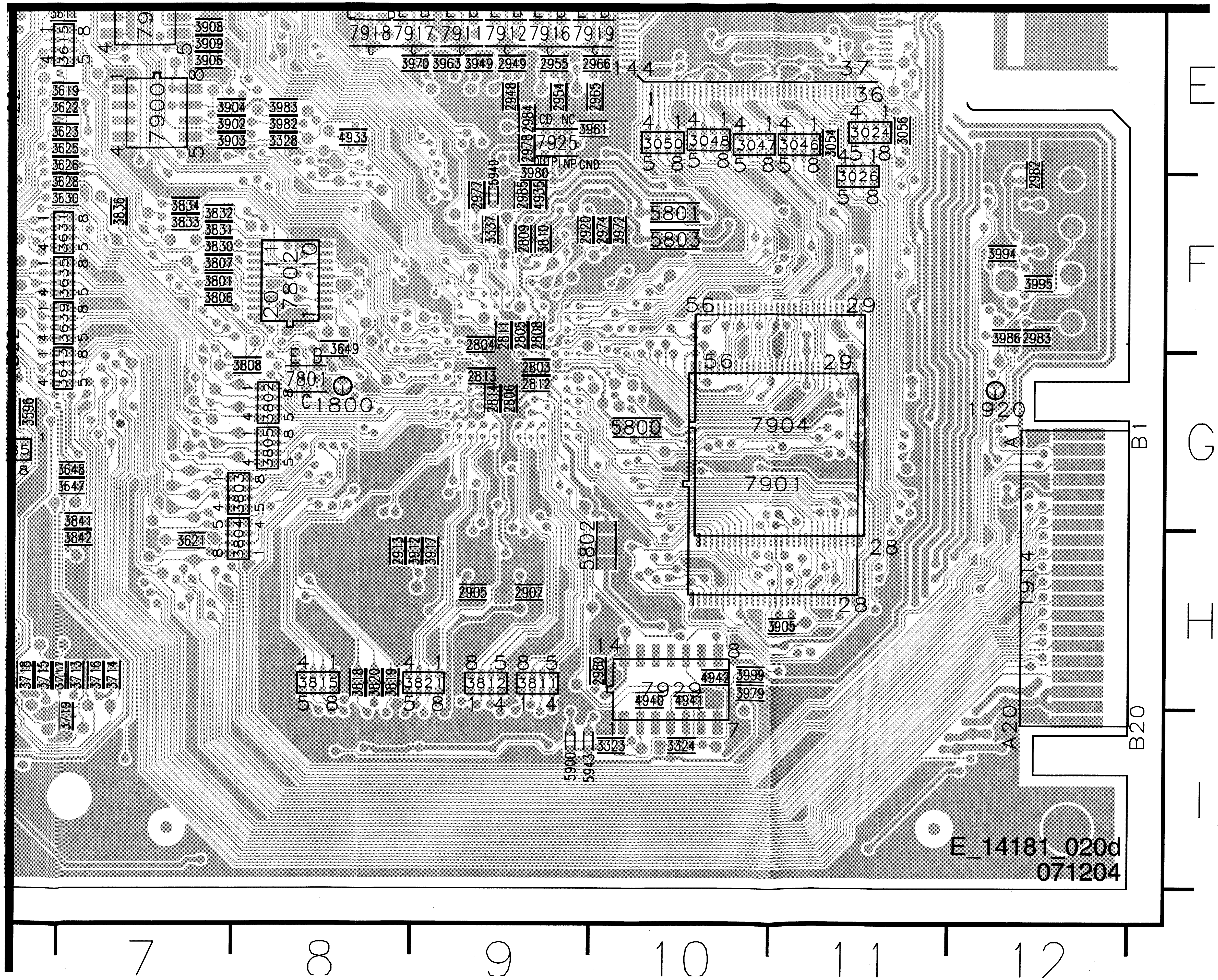
7011
7012
7016
7010

Layout: LECO Bottom View Part 4


3615
3908
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144
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3328
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2954
2965
2984
2978
CD
NC
7925
3961
INP
GND
3980
5940
2977
2985
4935
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2974
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3994
3995
3631
3635
3639
3643
56
29
3986
2983
3808
3649
7801
1800
2804
2811
2805
2808
2813
2803
2812
2814
2806
1920
3802
3805
3803
3804
5800
7904
7901
3596
3648
3647
3841
3842
3621
5802
2913
3912
3917
2905
2907
28
1914
3905
A1
B1
A20
B20
3718
3715
3717
3713
3716
3714
3719
3815
3818
3820
3819
3821
3812
3811
2980
7929
4942
3999
3979
4940
4941
3323
3324
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E_14181_020d
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8. Alignments

8.1 Reprogramming Procedure of NVM on the FEBE board

The NVM, item 7905 (7900 for LECO), on the FEBE board contains the slash information of the set
The slash version is stored at the end of the production line of the set.
In case of failure, the NVM must be replaced by an empty device. By way of commands via the Diagnostic Software or via ComPair, the factory settings must be restored in the NVM.

8.1.1 Slash Version

The slash version is stored with command 1217 followed by the slash version as parameter.
The slash versions used in DVDR610, DVDR615 and DVDR616 are the following:

- DVDR610/00/02/19/33: 11001
- DVDR610/05: 11002
- DVDR615/00/02/19/33: 11003
- DVDR615/05: 11004
- DVDR616/00/02/19/33: 11003
- DVDR616/05: 11004

Example:
DD:>1217 11003

8.2 Rework Procedure IEEE Unique Number

8.2.1 Scope:

The procedure describes how to upgrade sets with a unique number after repair. This unique number is stored in the NVRAM (item 7001 [7900 for LECO]) of the FEBE board at the end of the production line.
This procedure is only valid or necessary when:

- The FEBE board is replaced
- NVRAM on the FEBE board is replaced
- NVRAM is cleared

In all other cases the repaired set retains its unique number.
The procedure defines several means to re-assure the unique number depending on the possibilities of repair or the state the faulty set is in.

8.2.2 Handling:

State of original (defective) board:

1. The FEBE board starts up in Diagnostics Mode: follow procedure A to retrieve the valid unique number
2. The FEBE board does NOT start up in Diagnostics Mode: follow procedure B.

8.2.3 Procedure A

1. Connect defective digital board to PC via serial cable (3122 785 90017)
2. start up hyper terminal or any other serial terminal via the correct settings (DSW command mode interface)
3. read out existing unique number via 1208
   example:
   DS:> 1208 120800: DvldNumber is: 0x0C22384E5A
   Test OK @
4. note read out
5. program new digital board via nucleus 1207
   example:
   DS:> 1207 1234567890 120700: Test OK @

The set has now the original unique number

8.2.4 Procedure B

1. Note the serial number of the set example:
   VN050136130156
   - VN = production centre (VN....Szekesfehervar). According to UAW-500: V=22 and N=14
   - 05 = change code (this is not used for this calculation)
   - 01 = YEAR
   - 36 = Production WEEK
   - 130156 = Lot and SERIAL number
2. Calculate the unique number: this number always exists out of 10 hexadecimal numbers.
3. First 5 numbers: First we calculate a decimal number according to the formula below:35828*YEAR + 676* WEEK + 26*A + H + 8788 The figures are fixed, YEAR + WEEK + factory code (A + H) are variable Example: 35828*01+676*36+26*1+8+8788 = 68986 (decimal) Then we translate the decimal number to a hexadecimal number. example: 68986 (decimal)= 10D7A (hex)
4. Last 5 numbers: The last 5 numbers exist out of the Lot and SERIAL number.
   We have to translate the decimal number to the next 5 hexadecimal numbers: Example: 130156 (decimal) = 1FC6C (hex)
5. Program new digital board via nucleus 1207. Therefore we use the 10 hexadecimal numbers we calculated above: example:
   DS:>1207 10D7A1FC6C
   120700: Test OK @

The set has now its original unique number

8.3 Alignments after replacing the Boot EEPROM 7904 (7900 for LECO) on the FEBE Board

The NVM, item 7904 (7900 for LECO), on the FEBE Board contains the "Diversity String" that tells the software during startup which hardware version is present.
The setting is stored in the NVM during the production of the FEBE Board.
In case of a fault the NVM must be replaced by a programmed device containing the boot script.
Via the Diagnostic Software the Diversity String is stored with command 1226, followed by the Diversity String as parameter.

The diversity strings used in DVDR610, DVDR615 and DVDR616 are the following:"

FEBE Board Type:	String
E1_AV3_4	444248495AB8200145315F4156335F34350 40300000101020001000020040000
E2_AV3_4	444248496CB8200145325F4156335F34360 40300000000020001000020040000
OL22FEBE	4442484960A440016F6C32326665626593 1105000000000200010000200400004456 4452323030312E30303101030008000100 0000000201000000000000000000

Example:
DS:> 1226 444248495AB8200145315F4156335F34350
40300000101020001000020040000
122600
Test OK @

E1_AV3_4 FEBE Board (for DVDR615/00/02/05/19/33 and DVDR616/00/02/05).
E2_AV3_4 FEBE Board (for DVDR610/00/02/05/19/33).

With command 1228 the settings can be displayed.

9. Circuit-, IC descriptions and list of abbreviations

9.1 MOBO (Analog) Board

9.1.1 General

The pcba consists of the following parts:
- Control unit Slave µP
- Power supply unit
- Frontend (Audio & Video)
- Input/Output switching
- Audio ADC & DAC processing
- Analog Follow-Me circuit
- IR Blaster (for EPG sets only)

9.1.2 Control unit Slave µP

The core element of the MOBO analog board is the slave µP TMP87CM74AF [7107].
It runs on a 5V supply and is responsible for the following functions:
- Interface with the Chrysalis chip on the FEBE Digital backend
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infra-red receiver
- Activation and control of the display
- Heater voltage generation
- Fan control
- IR Blaster (for EPG sets only)

It runs on a high clock frequency of 8MHz with resonator [1101] and a low clock frequency of 32.768kHz with resonator [1102].

9.1.3 Interface to the Chrysalis chip

The communication to the Chrysalis chip on the FEBE Digital backend is done via I^{2}C interface, where the TMP87CM74AF acts in slave-mode.

9.1.4 Evaluation of the keyboard matrix

A resistor network on the Keyboard is used to generate a specific direct voltage value (KEY1- & KEY2-line), depending on the pressed key. Via the resistors 3157 and 3159 on the analog/digital (A/D) ports, [7107] pin 32 and 32 the evaluation is done.

9.1.5 IR receiver and signal evaluation

The IR receiver [7200] on the Keyboard contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received infra red transmission to electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7200], a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IF remote control command, can be measured. This pulse sequence is fed into the controller for further processing via pin 22 [7107].

9.1.6 Vacuum Fluorescence Display

The VFD BJ900GNK [1100] is fully controlled by the microcontroller. The microcontroller also includes the driving stages. Only two additional drivers [7110] and [7112] are necessary for the grids 8 and 9 because of their large size.

9.1.7 VFD Heater Voltage Generator

The circuit around [7102], [7103] and [7104] is used to generate a proper AC-voltage for the filament of the VFD. For this the microcontroller generates an appropriate rectangular signal with 50% duty-cycle and a frequency of 30kHz at pin 19. [5101] and [2112] are acting as resonance circuit. Via zener-diode [6102] and resistors [3111], [3113] and [3116] the two heater pins of the VFD (FIL1 and FIL2) are clamped so that the grids and segments can be fully switched off.

9.1.8 Fan Control

To avoid unwanted temperatures inside the set (especially the Laser on the OPU of the drive is very sensitive) a fan is located at the rear of the FEBE module. The speed control is dependent on the ambient temperature. A NTC resistor [3211] located on the Keyboard measures the temperature. The change in temperature is translated into dc levels and send to pin 28 of slave µP [7107]. High / low signals is then sends out via pin 5 and 6 of slave µP [7107] to control transistors [7106] and [7108] which regulates the fan motor to 3 different speeds

9.1.9 Power Supply Unit

Functional principle:
This power supply works in the way of a flyback converter. In the mains input part [1931 to 2315], the mains voltage is rectified and buffered in the capacitor [2315]. From this direct voltage at [2315] energy is transferred into the transformer [5300, pins 7-5] during the conductive phase of the switching transistor [7307] and is stored there as magnetic energy. This energy is passed to the secondary outputs of the power supply in the blocking phase of the switching transistor [7307]. With the switch-on time of the switching transistor [7307], the energy transferred in every cycle is regulated in such a way that the output voltages remain constant regardless of changes in the load or mains voltage. The power transistor is driven by the integrated circuit [7311].

Mains input part:
The mains input part extends from the mains socket [1931] to the capacitor [2315]. The diodes [6302, 6303, 6305 and 6307] rectify the AC supply voltage, which is then buffered by the capacitor [2315]. The common mode coil [5302] and capacitor [2311] work as a filter to block interference arising in the power supply from the mains. Components [1302], [3316] protect the power supply against short-term over voltages in the mains, e.g. caused by indirect lightning.

Start-up with Mains-on:
After connecting the power cord to the mains, the capacitor [2331] is loaded via a current source between pin 8 and pin 1 in the IC [7311]. Once the voltage on [2331] and therefore the supply voltage V_{CC} of the IC [7311] has reached approx. 11V, the IC starts up and provides pulses at its output pin 5. These pulses are used to drive the gate of the power transistor [7307]. The frequency of these pulses is depending on load and mains voltage. The current consumption of the IC is approx. 5 mA at V_{CC} in normal mode.
If V_{CC} drops to below approx. 9V (e.g. with power limitation) or if V_{CC} exceeds approximately 16V (e.g. interruption of the control loop), the output of the IC [7311, pin 5] is blocked and a new start-up cycle begins.
(See also Overload, Power Limitation and Burst Mode section)

Normal operation:
With the power supply in normal mode, the periodic sequences in the circuit are divided primarily into the conductive and blocking phase of the switching transistor [7307]. During the **conductive phase** of the switching transistor [7307], current flows from the rectified mains voltage at capacitor [2315] through the primary coil of the transformer [5300, pins 7-5], the transistor [7307] and resistors [3330, 3331] to ground. The

positive voltage on pin 7 of the transformer [5300] can be assumed as constant for a switching cycle. The current in the primary coil of the transformer [5300] increases linearly. A magnetic field representing a certain value of the primary current is formed inside the transformer. In this phase, the voltages on the secondary coils are polarized such that the diodes [6300, 6301, 6304, 6306, 6309, 6311, 6315 and 6318] block. From the controller [7319] a current is supplied into the CTRL input on the IC [pin 3, 7311] via optocoupler [7316]. Once the switch on time of the switching transistor [7307] - that corresponds to the current supplied into the CTRL input - has been reached, the switching transistor [7307] is switched off. When the switching transistor has been switched off, the **blocking phase** begins. No more energy will be transferred into the transformer. The inductivity of the transformer will still attempt to keep the current flowing at a constant level (U=L*di/dt). Switching off transistor [7307] interrupts the primary current circuit. The polarity of the voltages on the transformer is reversed, which means that the diodes [6300, 6301, 6304, 6306, 6309, 6311, 6315 and 6318] become conductive and current flows into the capacitors [2302, 2309, 2316, 2321, 2324 and 2328] and the load. This current is also ramp-shaped (di/dt negative, therefore decreasing).
The **feedback control** for the switched-mode power supply is done by changing the conductive phase of the switching transistor so that either more or less energy is transferred from the rectified mains voltage at [2315] into the transformer. The regulation information is provided by voltage reference [7319]. This element compares the 5V-output voltage via voltage divider [3359, 3362, 3363] with an internal 2.5V reference voltage. The output voltage of [7319] passes via an optocoupler [7316] for insulation of primary and secondary parts as a current value into pin 3 on the IC [7311]. The switch-on time of the transistor [7307] is inversely proportional to the value of this current.

Overload, power limitation, burst mode:
With increasing load on one or more of the power supply outputs, the switch-on time for the power transistor [7307] increases, and thus also the peak value of the delta-shaped current through this power transistor. The equivalent voltage of this current profile is passed from resistors [3330] and [3331] via [3334] to pin 5 of the IC [7311]. If the voltage on pin 2 reaches approx. 0.4V in one switching cycle, the conductive phase of the switching transistor is ended immediately. The check is done in each individual switching cycle. This process ensures that no more than approx. 50W can be taken out from the mains (= **power limitation**).
If the power supply reaches the power limit, the output voltages and the supply voltage V_{CC} on pin 1 of the IC [7311] will be reduced following further loading. If V_{CC} is less than approx. 9V at any point during this process, the output of the IC [7311, pin 6] is blocked. All output voltages and V_{CC} decrease and a new start-up cycle begins. If the overload status or short-circuit remains, the power limitation will be activated immediately and the voltages will again decrease, followed by another start-up cycle (**Burst Mode**). The amount of power taken up from the mains in burst mode is low.

Standby modes:
In the AV-Standby operating mode of the set, the DD_ON control line is low switching off the +5VE and +12VE supply [connector 1932] to the FEBE Frontend and DVD drive. This reduces the amount of power taken from the mains.
In Low Power Standby mode, additional STBY control line is high switching off the 12V, 5V, 5N and 3V3SW supply. In this mode all functions are switch off and the slave µP (in idle mode) and real time clock (32.768kHz) is running. This reduces power consumption to less than 3W. In some program mode the slave µP provides a wakeup service (STBY-line switches to low), then the Chrysalis main controller starts up and asks for the wakeup reason.

9.1.10 Tuner Frontend

This unit support Broadcast System PAL: BG, DK, I and SECAM: L, L'.
It has a RF IN for antenna connection and RF OUT which provides a RF loop through during Standby mode for connection to the TV.
The frontend is controlled by the I^2C (SCL_5V- and SDA_5V-) lines coming from the slave µP.
Complete video processing is done in this unit and the video output (CVBS) is out from pin 17 via transistor 7000 as VFV-line to the Video I/O and Follow Me circuitry.
The audio-IF component SIF1 is taken out from pin 7 for demodulation in the sound processor [7600].

Audio demodulator
The sound demodulation is done by the MSP3415 [7600], which is also fully controlled via I^2C-bus by the slave µP (determination of bandwidth, amplitude, standard, ...). The audio signals are available at pin 26 and pin 27 of [7600] and fed as AFER- & AFEL-line to the audio-I/O for further processing.

9.1.11 Audio routing

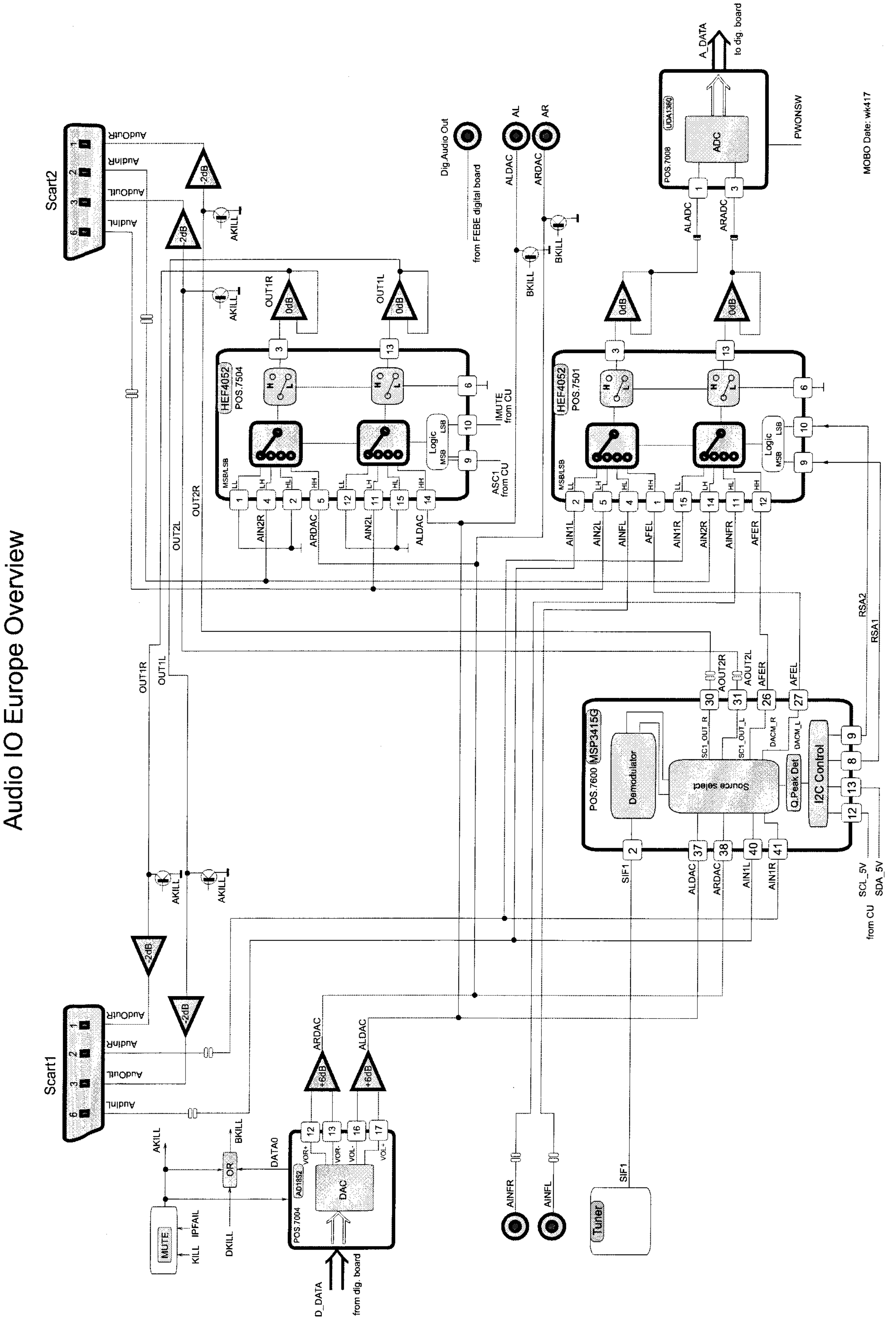

Audio IO Europe Overview
Scart2
Scart1
AudOutR
AudInR
AudOutL
AudInL
-2dB
AKILL
BKILL
OUT1R
OUT1L
OUT2R
OUT2L
0dB
HEF4052
POS.7504
POS.7501
MSB/LSB
LL
LH
HL
HH
Logic
MSB
LSB
IMUTE from CU
ASC1 from CU
AIN2R
ARDAC
AIN2L
ALDAC
AIN1L
AINFL
AFEL
AIN1R
AINFR
AFER
RSA2
RSA1
Dig.Audio Out
from FEBE digital board
AL
AR
POS.7008
UDA1360
ADC
A_DATA
to dig. board
PWONSW
ALADC
ARADC
MOBO Date: wk417
POS.7600
MSP3415G
Demodulator
Source select
Q.Peak Det
I2C Control
SC1_OUT_R
SC1_OUT_L
DACM_R
DACM_L
AOUT2R
AOUT2L
SIF1
SCL_5V
SDA_5V
from CU
Tuner
POS 7004
AD1852
DAC
+6dB
VOR+
VOR-
VOL-
VOL+
DATA0
OR
MUTE
KILL
IPFAIL
DKILL
D_DATA
from dig. board

Figure 9-1 MOBO Audio IO Eur

The processing of audio is always done in stereo (e.g. separate left- and right-channel) and the complete switching is realized by using HEF4052, which is a dual four-to-one multiplexer and MSP3415G, multi-sound processor. In principle there are three independent selectors:

a) Scart 1-Output-Path:
Pos [7504] is used to select either Scart 2-Input (AIN2L/AIN2R) or the signal directly from the audio DAC [7004] (ALDAC/ARDAC) as the output source for Scart 1 (AOUT1L/AOUT1R). The control is done by means of the lines ASC1S coming from slave µP [7107].

b) Scart 2-Output-Path:
The MSP [7600] is used to select either Scart 1-Input (AIN1L/AIN1R), signals from the DAC [7004] (ALDAC/ARDAC) or Tuner frontend as the output source for Scart 2 (AOUT2L/AOUT2R).

c) Record-Path:
Pos [7501] selects either signals from Scart 1 (AIN1L/AIN1R) or Scart 2 (AIN2L/AIN2R) or Cinch-Front (AINFL/AINFR) or the MSP [7600] (AFEL/AFER) and routes to the audio ADC [7008] (ALADC/ARADC) for record purposes. The switch is controlled via RSA1 and RSA2 signals. These signals come from the MSP [7600], which acts as a port expander of the slave µP.
The two selectors [7501] & [7504] has a separate Op-Amp on the output for level-adaptation-, performance- and line-driving-reasons: [7500-1 & -2] for record, [7503-1 & -2] for Scart 1-Output respectively. Every audio output line on the two Scart connectors and rear Cinch sockets can be killed (muted) by the AKILL-line [7505], [7507], [7602] &[7603] and the BKILL-line [7802], [7804].
Additionally to analog audio the set is also equipped with a digital output via cinch plug [1955]. The signal is generated on the FEBE Digital backend and routed via audio interface cable and connector [1900] to the MOBO analog board. Here the DAOUT-line first passes a 6-fold inverter [7551] being used as a driver and for performance reasons (noise reduction, jitter, ...). Afterwards a transformer [5551] is necessary to achieve the correct level and also to have a floating output with isolated ground before the signal is fed via [3559 & 3563] to cinch plug [1955]. The capacitor [2553] performs an AC-coupling between connector- and set-ground.

9.1.12 Audio ADC/DAC

The conversion of analog audio signals from the record-selector [7501] in the audio I/O (ALADC & ARADC) is done via UDA1361TS [7008]. This IC can process input signals up to $2V_{rms}$ by using external resistors [3034], [3036] in series to the input pins. All required clock signals are generated on the FEBE Digital backend and only the audio data (A_DAT-line) are routed from MOBO analog board to FEBE Digital backend for further processing.
The transformation of digital audio back into the analog domain is done by AD1852 [7004]. All necessary clock signals are coming from the FEBE digital backend and digital audio data (D_DATA0-line) are converted into analog signals, which are available at pin 12 & 13 (right channel) and pin 16 & 17 (left channel) of [7004]. Afterwards an Op-Amp. [7005] (line driver & level adaptation) and a low-pass-filter to increase signal performance (noise, distortions,...). is passed. Then both signals (ALDAC & ARDAC) are directly routed to the rear cinch output and also used in the audio-I/O for further processing.
The DAC has also a mute possibility, which can be activated by setting pin 8 to high via [7006]. This mute is controlled either by the FEBE digital backend (D_IKLL-line), IMUTE-signal from the slave µP or the IPFAIL-signal from power-supply-unit.
In addition to that the cinch outputs is killed (muted) in case of digital silence (D_DATA0-line zero) by the circuit around [7045] and [7002] via the BKILL-line.

9.1.13 Video-routing

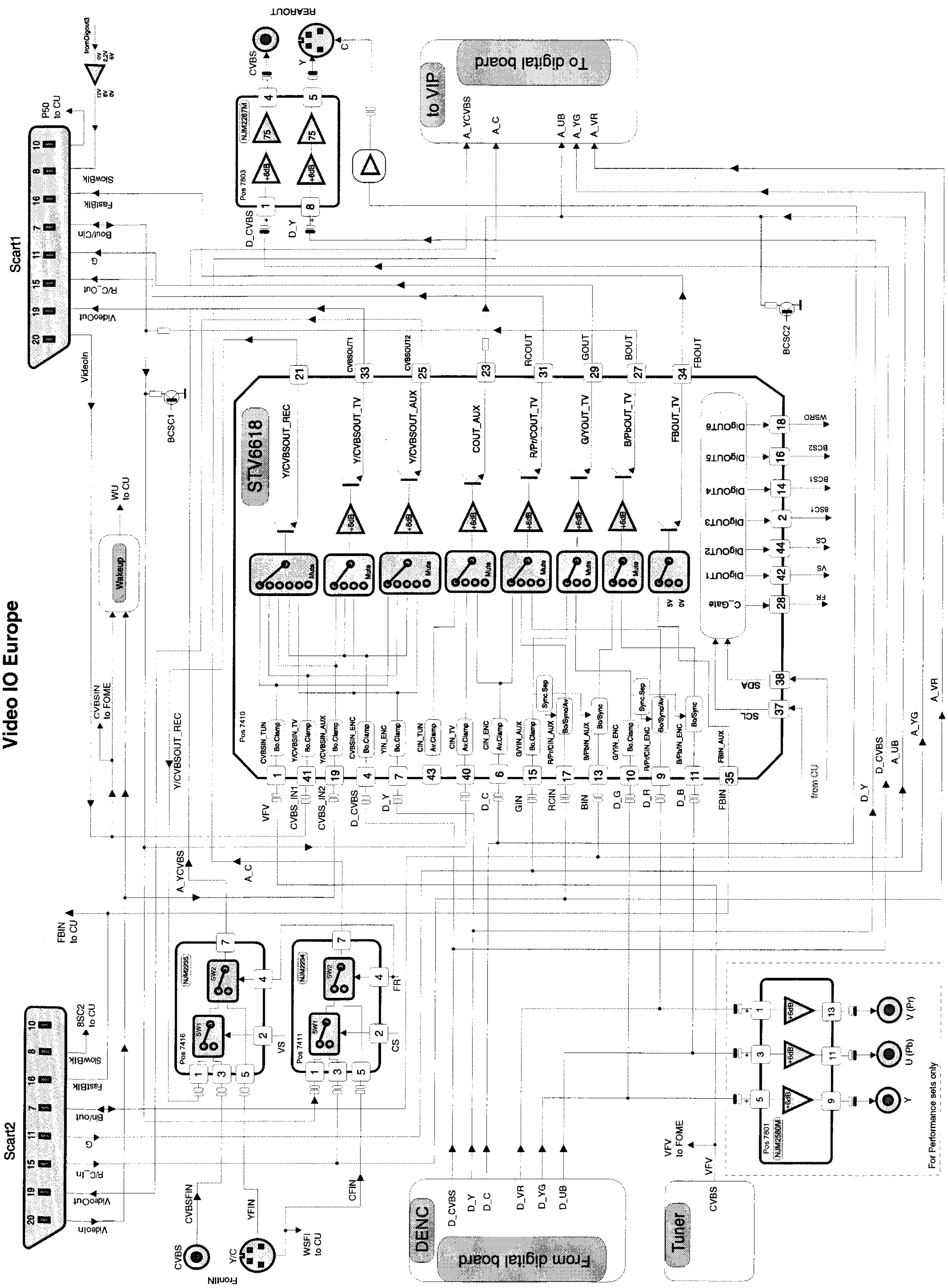

Video IO Europe
Scart1
Scart2
STV6618
Pos 7410
To digital board
to VIP
From digital board
DENC
Tuner
REAROUT
FrontIN
NJM2267M
Pos 7803
NJM2235
Pos 7416
NJM2234
Pos 7411
NJM2560M
Pos 7801
For Performance sets only
Wakeup
BCSC1
BCSC2
P50 to CU
WU to CU
FBIN to CU
8SC2 to CU
WSFI to CU
VFV to FOME
CVBSIN to FOME
Y/CVBSOUT_REC
A_YCVBS
A_C
A_UB
A_YG
A_VR
D_CVBS
D_Y
D_C
D_VR
D_YG
D_UB
CVBS
Y/C
CVBSFIN
YFIN
CFIN
VFV
CVBS_IN1
CVBS_IN2
GIN
RCIN
BIN
D_G
D_R
D_B
FBIN
CVBSOUT1
CVBSOUT2
RCOUT
GOUT
BOUT
FBOUT
Y/CVBSOUT_TV
Y/CVBSOUT_AUX
COUT_AUX
R/Pr/COUT_TV
G/YOUT_TV
B/PbOUT_TV
FBOUT_TV
DigOUT1
DigOUT2
DigOUT3
DigOUT4
DigOUT5
DigOUT6
C_Gate
SDA
SCL
from CU
WSRO
BCS2
BCS1
8SC1
CS
VS
FR
SlowBlk
FastBlk
Bout/Cin
Bin/out
G
R/C_Out
R/C_In
VideoOut
VideoIn
fromDigout3
+6dB
75
Mute
Bo.Clamp
Av.Clamp
Sync.Sep
Bo/Sync
Bo/Sync/Av
SW1
SW2
V (Pr)
U (Pb)
Y

Figure 9-2 MOBO Video IO Eu

9.2.3 Frontend part

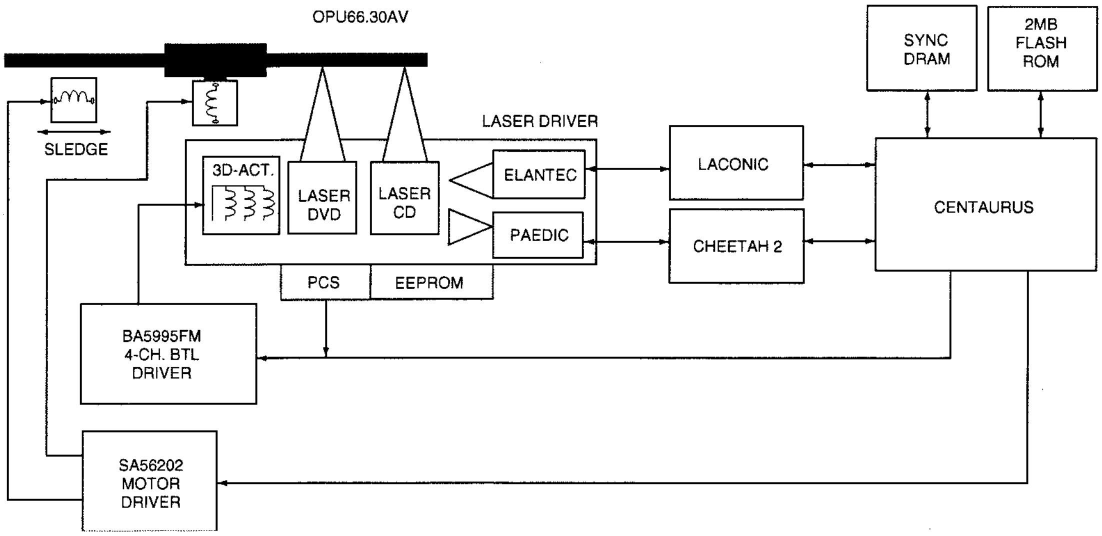


Figure 9-3 Servo Block

This section describes briefly the functional behavior of the engine. It performs all basic servo and data processing function:

- it reads data from the disc
- it writes data to the disc - it controls all other functions like tray control, start/stop the disc, tracking, jumping, and communication to the host.
- encodes and multiplexes analogue video and digital uncompressed audio (I^2C) into a MPEG2 stream
- decodes the MPEG2 stream into analogue and digital audio and into analogue video

Centaurus 1.5 (PNX7850E)

Centaurus Basic Functions Block Diagram

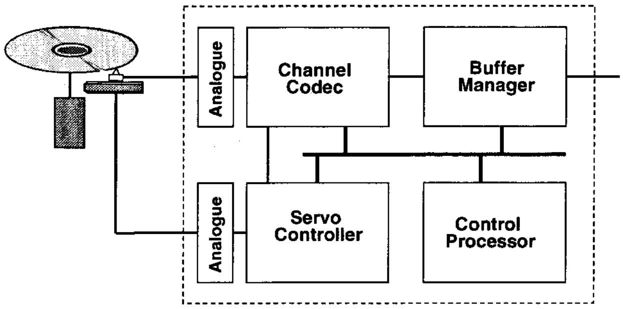


Figure 9-4 Centaurus

The Centaurus [7500] is a highly integrated IC that controls all the functions of the drive. It interfaces via the IDE bus to the MPEG backend and incorporates the following functions.

- CD/DVD channel decoder/encoder
- CD/DVD data block decoder/encoder
- Buffer Manager
- Digital Servo processor using digital signal processor
- Drive system microprocessor based on MIPS core

The MIPS microcontroller uses Flash ROM for the firmware and SRAM to execute the program. SDRAM is provided for the encoding/decoding function block of centaurus [7500]. 2 Mbytes of data buffer size is available inside the IC for data storage.

Cheetah 2 (TZA1047)

The Cheetah2, [7201] is an analogue pre-processing for the diode signals coming from the OPU. It contains an amplifier with programmable gain that amplifies the RF signal to adapt the output for the different reflectivity of the various discs. The tracking signals are filtered and normalized. In addition the IC contains a timing circuit for the sample and holding circuits and for switching the various blocks between read and write. Supporting functions such as laser control and offset control are incorporated. Communication to and from the IC is based on a fast two-wire serial bus that works according to the I^2C interface protocol.

Laconic (TZA1042)

The main function of the Laconic, [7300] is to control the laser power. The IC forms a closed control loop in combination with the Elantec located on the OPU. It compensates aging and temperature of the laser. Furthermore it forms a fingerprint correction loop. It also acts as bridge between I^2C and serial bus of the Elantec laser driver on the CPU.

Optical Pick-up Unit

The OPU66 is a dual laser Optical Pick-up Unit for the DVD+RW/+R. It consists of a 3-D actuator for focusing, radial tracking and tilt correction.

- 650nm laser for DVD
- 780nm laser for CD

On the interconnecting flex several electrical components are mounted.

- Elantec: programmable laser diode power driver

- Paedic: integrated photo detector with programmable gain pre-amplifier
- Eeprom: containing a number of values representing adjustments belonging to the OPU

The laser control and diode signal processor ICs together with an Eeprom are mounted on the OPU flex.

The laser control IC generates the DVD laser read and writing signals needed for reading DVD discs and writing DVD+RW/+R discs (write strategies of DVD+RW/+R discs).

The diode signal processor is an analogue pre-processor adapted for the CD and CD-R/RW read function.

The Eeprom contains information about writing current, writing strategies and other parameters belonging to the OPU.

Motor and Servo drivers

The disc, tray and sledge motors are driven by a one-chip motor driver SA56202 [7402] while the 3-D actuator is driven & control by a 4-channe BTL driver BA5995FM [7409] and some low power Ops amplifier LM358D [7401], [7403] and [7405].

The complete Video-I/O-switching is basically realized by the matrix switch STV6618 [7410], which is controlled via I^2C-bus by the slave µP. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6 dB-amplification and a 75 Ohms driver-stage inside. This IC includes also several digital outputs, which are used for switching purposes on the analog board. The record selector inside the switch selects between the CVBS from Tuner frontend (VFV), the input from Scart 1 (YCVBSIN1) or the signal from Scart 2 (YCVBSIN2). Afterwards the signal passes another switch [7416] in which a selection between signals from the front or the preselected ones are done.
Likewise a second switch [7411] selects between Scart 1 (CIN) and Scart 2 (RCIN) and front (CFIN). The output signals of [7416] A_YCVBS- and [7411] A_C-lines are fed to the VIP on FEBE Digital backend for further processing.
The R/G/B-inputs and the Fast-Blanking-line from Scart 2 are directly routed to the FEBE Digital backend. These signals are also available on the corresponding input-pins of the STV6618 to enable a loop-through in AV-Standby. In this mode the set has to behave like a cable between the two Scart-connectors.
AV-Standby is activated either by a high level on pin 8 of Scart 2 (active device is present) or by the WU-line (wake up). This signal is generated out of the circuit around [7401], [7402] & [7404] and will become high if there is a signal on pin 20 of Scart 1- or Scart 2. The detection of the input level on pin 8 of Scart 2 (8SC2) is done via an analog input of the slave µP (less than 2V means inactive; 4,5V to 7V determines a source with 16:9 picture-ratio and greater than 9,5V is an active 4:3 source).
All signals from the FEBE Digital backend (D_VR, D_YG, D_UB, D_C, D_Y and D_CVBS) are routed to the proper inputs of the STV6618 for amplification and driving purpose before they can be seen on the appropriate Scart outputs.
Parallel to this the D_CVBS- and the D_Y-line are passing a 6 dB-amplifier and driver-IC [7803] and are then routed to the CVBS-Cinch and Y/C-out rear. The chroma signal for this Y/C out is coming from the STV6618.
The detection of the picture ratio information on the Y/C-input front is made by measuring the DC-level on the Chroma signal via analog input of the slave µP (WSFI-line). In case the level is higher than 3,5V the input signal is a 16:9 source. If the level is lower than 2,4V the picture ratio is 4:3.
Likewise for the D_VR-, D_YG- and D_UB- lines are passing a 6dB-amplifier and driver-IC [7801] and routed as component video YUV (For Performance set only).
The control of the switching voltage (Pin 8 of Scart 1) is done via 3-level-pin (pin 2) of the STV6618 [7408] and the transistors [7405], [7407] & [7409]. A low on pin 2 of [7408] causes around 11V on pin 8-Scart 1 (e.g. source with 4:3 picture-ratio active). Medium level (2,5V) on pin 2 of the STV6618 generates medium level (approx. 6V) on pin 8-Scart 1 (e.g. active source with 16:9) and a high on pin 2 of the STV6618 pushes pin 8-Scart 1 to low (e.g. inactive).

9.1.14 Analog Follow-Me

This circuit compares the video signal from the Tuner frontend (VFV) of the recorder with that one of the connected TV-set (CVBSIN). The TV set delivers the signal via Scart-cable. A comparator [7951] and several additional parts [7953], [7954], ... are used to compare the two video signals. In case of both input signals are equal the output-line of this circuit (FOME) is set to low. Detection is made via an input port of the slave µP.

9.2 VAU8041 (FEBE / AV3.5) Module

9.2.1 General

The Video Recorder Drive VAU8041 module known as FEBE 1.0 with AV3.5 drive is actually the Video Recorder Drive VAD8041 module with and extended board. The new FEBE board contains both the frontend Servo and backend Digital portion. Being physically on the same board the IDE connector is no longer required.
The recorder engine performs all basic servo tasks - reading and writing data on the disc and controls all functions like tray control, start/stop the disc, tracking, jumping and communicating to the host.
Mechanically, the module consists of a motorized tray loader that contains the dual laser optical pickup unit and a board that contains all the electronics needed to control the drive and interfacing to the MPEG encoder/decoder backend Digital portion
The backend Digital portion encodes and multiplexes analogue video and digital uncompressed audio (I^2S) into an MPEG2 stream. This MPEG2 stream is formatted, to be recorded by the DVD+RW/+R engine. In playback, it decodes the MPEG2 stream into analogue and digital audio and into analogue video.
There is a temperature sensor included in the drive that prevents malfunction or destruction of the drive in case the temperature inside the drive gets too high.

9.2.2 Power Supply

The +3V3, +5V, -5V and +12V come from the PSU of the MOBO analog board via connector [1905] while the +1V8 core voltage is generated on the board by a low voltage buck controller [7929]. It provides the control for DC-DC power solution producing a +1.8V output power over a wide current range. The NCP1570-based solution is powered from +12V with the output derived from the +3V3 supply. It contains all required circuitry for a synchronous NFET [7927-1] and [7928-2] buck regulator.

9.2.4 Backend Digital part

Record Mode

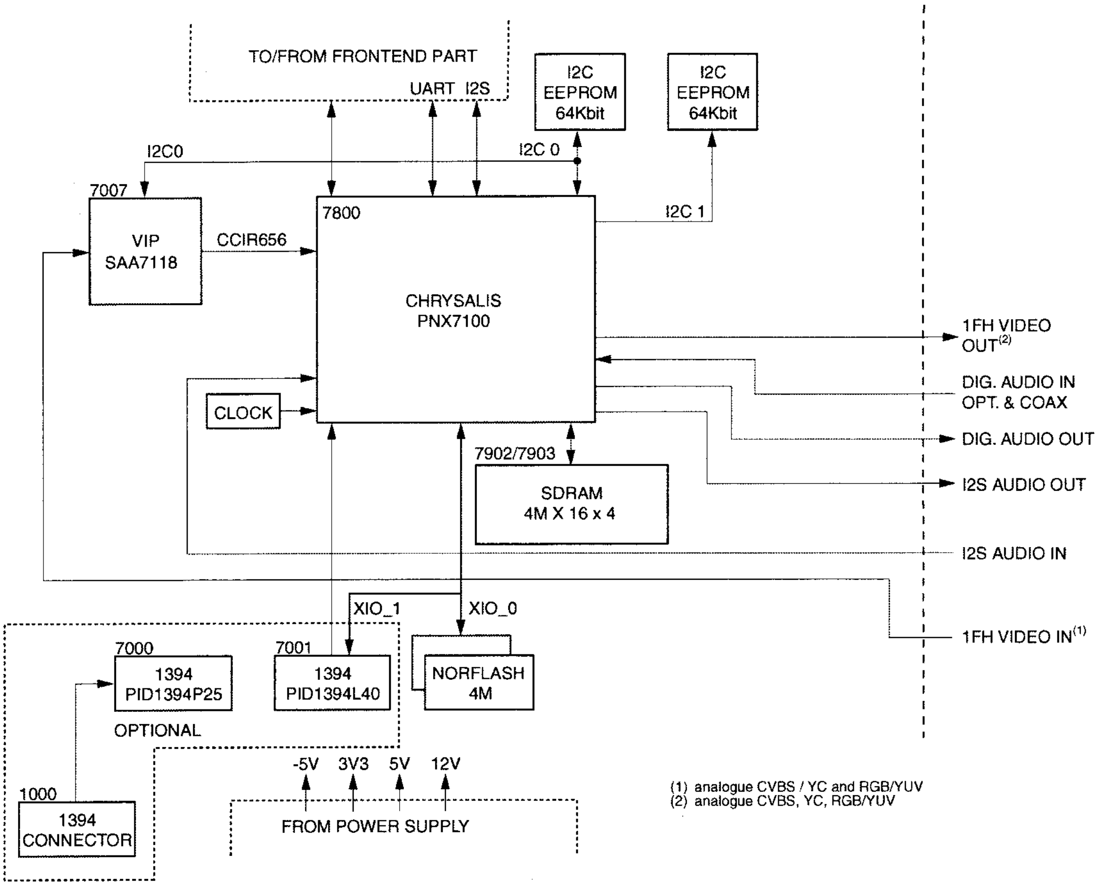

TO/FROM FRONTEND PART
UART
I2S
I2C EEPROM 64Kbit
I2C EEPROM 64Kbit
I2C0
I2C 0
I2C 1
7007
VIP SAA7118
CCIR656
7800
CHRYSALIS PNX7100
CLOCK
7902/7903
SDRAM 4M X 16 x 4
1FH VIDEO OUT(2)
DIG. AUDIO IN OPT. & COAX
DIG. AUDIO OUT
I2S AUDIO OUT
I2S AUDIO IN
1FH VIDEO IN(1)
XIO_1
XIO_0
7000
1394 PID1394P25
7001
1394 PID1394L40
NORFLASH 4M
OPTIONAL
1000
1394 CONNECTOR
-5V 3V3 5V 12V
FROM POWER SUPPLY
(1) analogue CVBS / YC and RGB/YUV
(2) analogue CVBS, YC, RGB/YUV

Figure 9-5 Chrysalis Block

Video Part

The analogue video input signals CVBS, YC and YUV/RGB (RGB for Euro and YUV for USA) from the MOBO analog board are routed from connector [1901] to IC [7007] SAA7118 , Video Input Processor.

The digital video input signals are routed from the DV-in connector [1000] via ICs [7000], 1394 PHY and [7001] 1394 LINK to Chrysalis PNX7100 [7800].

The multi-standard Video Input Processor VIP, [7007] encodes the analogue video to digital stream (CCIR656 format). It provides filtering of the analogue signals and separation of luminance and chrominance by a comb filter. The output stream, named ITU_IN(7:0), is then routed to the Chrysalis [7800]. This IC encodes and decodes the digital video stream into/from MPEG2 format.

Audio Part

I^2S audio is sent from the MOBO analog board to the Chrysalis [7800] via connector [1902]. The Chrysalis [7800] compresses the I^2S audio data into an MPEG1-L2/AC3 audio stream.

Front-end I^2S

Chrysalis [7800] interfaces directly with the Centaurus [7500] and buffers the in- and out-going data streams.

In the Chrysalis [7800], the video MPEG2 stream and the audio AC3 stream are multiplexed into an I^2S stream. The serial data are sent to the Centaurus [7500] for recording.

Playback Mode

During playback, the serial data from the Centaurus [7500] is going directly to the Chrysalis [7800] via the serial front-end I^2S interface. The Chrysalis [7800] is an MPEG CoDec and has the following outputs:

- To the MOBO analog board: analogue video RGB, YC, CVBS on connector [1901].
- I^2S audio (PCM format) on connector [1902].
- SPDIF audio (digital audio output) on connector [1902].
- Communication gateway (RS232) on connector [1907].

Clock Distribution

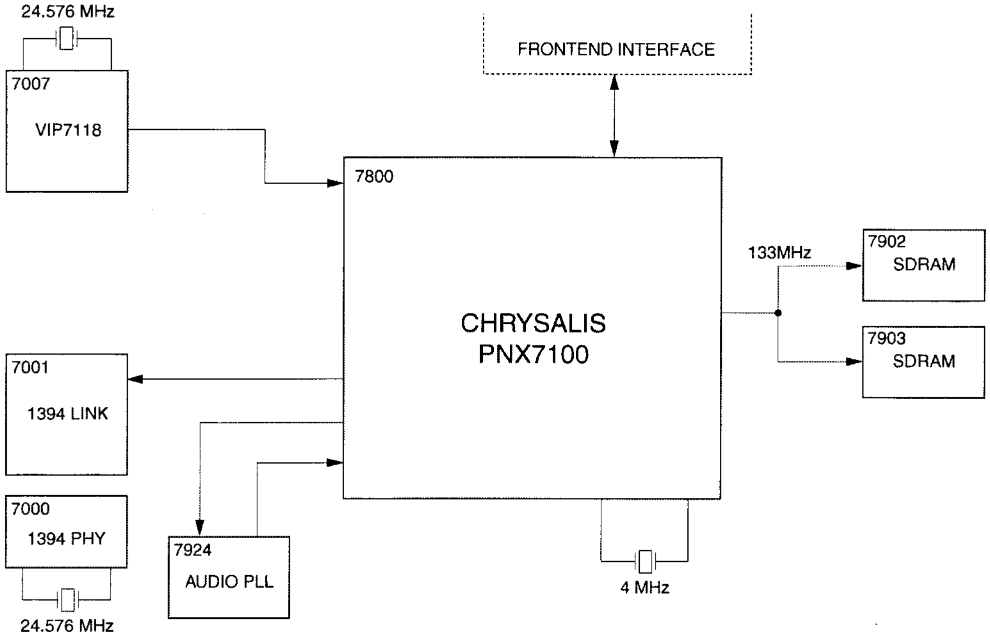

24.576 MHz
7007
VIP7118
FRONTEND INTERFACE
7800
CHRYSALIS
PNX7100
133MHz
7902
SDRAM
7903
SDRAM
7001
1394 LINK
7000
1394 PHY
24.576 MHz
7924
AUDIO PLL
4 MHz

Figure 9-6 Chrysalis Clock

The Chrysalis [7800] has a complex clock system, which is needed to support the processes running at different frequencies such as video decoding, audio decoding or peripheral I/O devices etc. To ensure a synchronous initialization of all the registers and state machines, all the PLLs are switched to their default frequency and the reset sequence is run at 4MHz. Then when the booting control unit is correctly initialized and once it has captured all the booting parameters, it sets the PLLs to its functional frequency to allow the modules to run at their nominal frequencies. Thanks to a clock blocking mechanism, the frequency switching is glitch free.

System clocks:

- PNX7100 [7800], pins AF9 and AF10 : 4MHz provided by the crystal oscillator [7804]
- SAA7118 [7007], pins A3 and B4 : 24.576 MHz provided by crystal [1002]
- SDRAM [7902] and [7903], pin 38 : 133MHz provided by PNX7100
- 1394-LINK [7001], pin 88 : 49.152MHz provided by 1394-PHY
- 1394-PHY [7000], pin 59 and 60 : 24.576MHz provided by crystal [1001]

Memory

Several memories are used on the Chrysalis [7800]:

- EEPROM [7904] : this memory contains all the necessary boot parameters of the board
- EEPROM [7905] : this memory contains all the necessary parameters for the application
- FLASH [7900] : this memory contains the application, diagnosis and service software

Reset

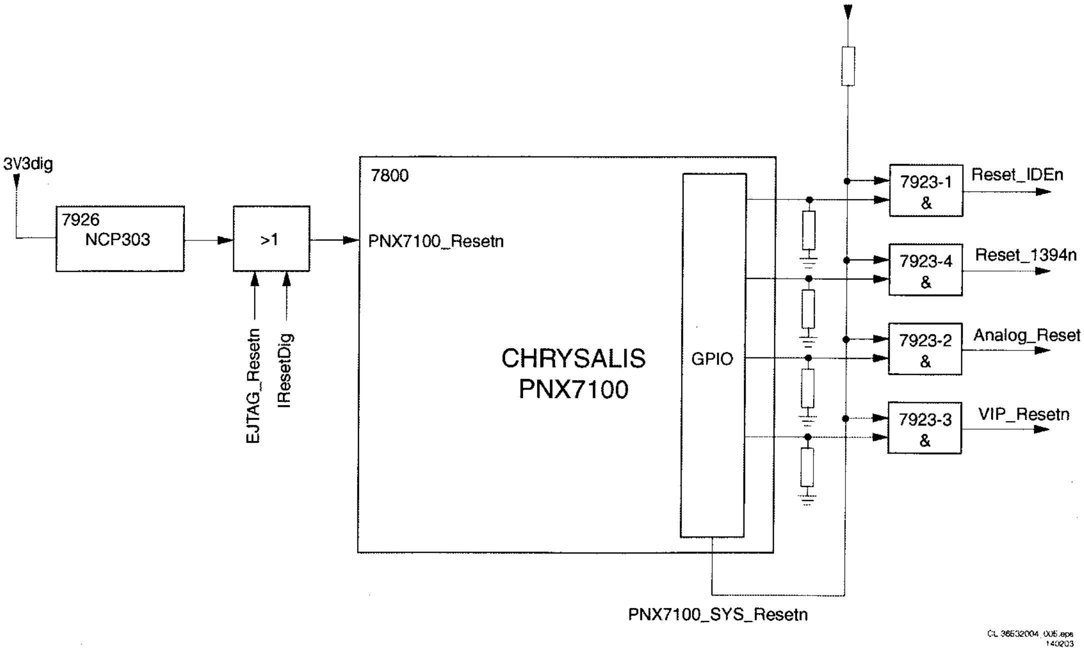

3V3dig
3V3dig
7926
NCP303
>1
EJTAG_Resetn
IResetDig
7800
PNX7100_Resetn
CHRYSALIS
PNX7100
GPIO
7923-1
&
Reset_IDEn
7923-4
&
Reset_1394n
7923-2
&
Analog_Reset
7923-3
&
VIP_Resetn
PNX7100_SYS_Resetn
CL 36532004_006.eps
140203

Figure 9-7 Chrysalis reset

The voltage detector NCP303LSN290 [7926] provides the reset signal PNX7100_RESETn (active: low) with the correct timing behavior. This circuitry functions as a Power-On Reset (POR) module, which detects the minimum functional voltage that is needed by the device. It also detects any voltages drop. When the power voltage is outside the nominal range, a reset signal is generated by the POR module and fed to the reset module which controls the individual reset of the different peripherals and processing units.
There are two control lines which can overrule this reset signal:

- IRESET_DIG (controlled by the slave µP on the MOBO Analog board)
- EJTAG_RESETn (only for production)

They can pull the output of the NCP303LSN29 [7926] down via a shottky diode.
So when the output signal PNX7100_RESETn is low, the board will reset. When this signal is high, the board is up and running. The PNX7100_SYS_RESETn is a general enabling signal for the different reset lines. All other reset lines are directly driven from Chrysalis [7800] port pins (eg. MPIO13_IDE1_RESETn). All reset lines are logically connected via 74LVC08AD [7923] AND-gates. If both reset signals are low, all other external devices are initialized.

I^2C Bus
The Chrysalis [7800] is the master of all the I^2C bus (during reset, external I^2C masters are allowed). The following ICs are controlled by the I^2C bus:

- [7904] Boot Eeprom
- [7905] NVRAMs
- [7007] VIP

9.2.5 I/O Connectors

Audio IO Connector [1902]
The Audio In/Out (AIO) connector is used to interchange digital audio signals between MOBO Analog and FEBE Backend Digital portion.

Video IO Connector [1901]
The Video In/Out (VIO) connector is used to interchange analogue video signals between MOBO Analog and FEBE Backend Digital portion.

9.2.6 Service UART Interface

Transistor 7950, BC847BS is used to make a level conversion from microprocessor (LVTTL) to +/-5V (compatible with most RS232 interfaces) and vice versa. The control line MPIO19_CTL_SERVICE is used to activate service and diagnostic SW at start up procedure. The connectivity is provided via an external service tool.

9.3 Lecolite U4.01L Module

9.3.1 General

Leco U4.0L module is a DVD recorder module that houses a recorder drive VAU 8041 to a simpler Frontend- Backend Board (Leco). Being physically on the same board the IDE connector is no longer required.
The recorder engine performs all basic servo tasks - reading and writing data on the disc and controls all functions like tray control, start/stop the disc, tracking, jumping and communicating to the host.
Mechanically, the module consists of a motorized tray loader that contains the dual laser optical pickup unit and a board that contains all the electronics needed to control the drive and interfacing to the MPEG encoder/decoder backend Digital portion
The backend Digital portion encodes and multiplexes analogue video and digital uncompressed audio (I^2S) into an MPEG2 stream. This MPEG2 stream is formatted, to be recorded by the DVD+RW/+R engine. In playback, it decodes the MPEG2 stream into analogue and digital audio and into analogue video. There is a temperature sensor included in the drive that prevents malfunction or destruction of the drive in case the temperature inside the drive gets too high.

9.3.2 Power Supply

The +3V3, +5V, -5V and +12V come from the PSU of the MOBO analog board via connector [1302] while the +1V2 core voltage is generated on the board by a low voltage buck controller [7301]. The NCP1571-based solution is powered from +12V with the output derived from the +3V3 supply. It contains all required circuitry for a synchronous NFET [7300-1] and [7300-2] buck regulator.

9.3.3 Frontend part

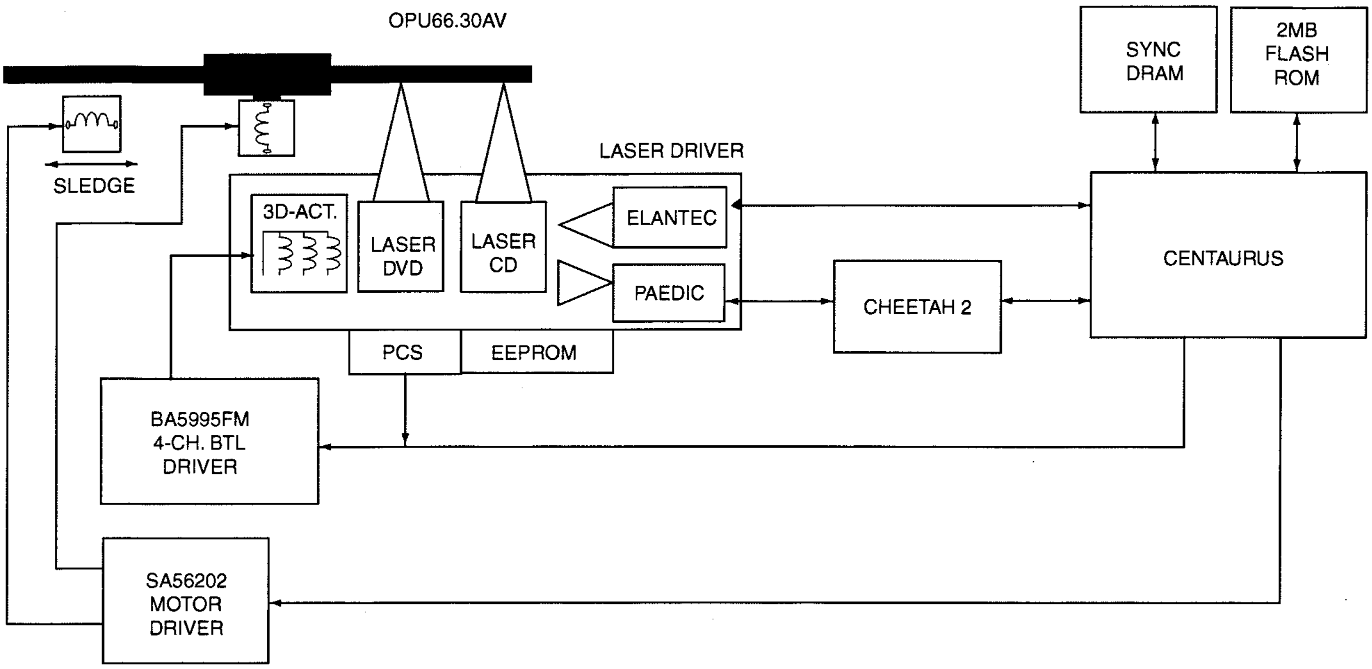


Figure 9-8 Lecolite Servo Block

This section describes briefly the functional behavior of the engine. It performs all basic servo and data processing function:

- it reads data from the disc
- it writes data to the disc - it controls all other functions like tray control, start/stop the disc, tracking, jumping, and communication to the host.
- encodes and multiplexes analogue video and digital uncompressed audio (I^2C) into a MPEG2 stream
- decodes the MPEG2 stream into analogue and digital audio and into analogue video

Centaurus 2 (PNX7860E)

Centaurus Basic Functions Block Diagram

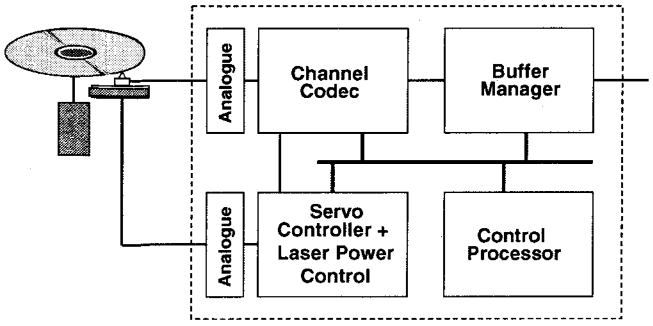


Figure 9-9 Centaurus

The Centaurus [7501] is a highly integrated IC that controls all the functions of the drive. It interfaces via the IDE bus to the MPEG backend and incorporates the following functions.

- CD/DVD channel decoder/encoder
- CD/DVD data block decoder/encoder
- Buffer Manager
- Digital Servo processor using digital signal processor
- Drive system microprocessor based on MIPS core
- Laser Power Control

The MIPS microcontroller uses Flash ROM for the firmware and SRAM to execute the program. SDRAM is provided for the encoding/decoding function block of centaurus [7501]. 2 Mbytes of data buffer size is available inside the IC for data storage.

Cheetah 2 (TZA1047)

The Cheetah2, [7201] is an analogue pre-processing for the diode signals coming from the OPU. It contains an amplifier with programmable gain that amplifies the RF signal to adapt the output for the different reflectivity of the various discs. The tracking signals are filtered and normalized. In addition the IC contains a timing circuit for the sample and holding circuits and for switching the various blocks between read and write. Supporting functions such as laser control and offset control are incorporated. Communication to and from the IC is based on a fast two-wire serial bus that works according to the I^2C interface protocol.

Optical Pick-up Unit

The OPU66 is a dual laser Optical Pick-up Unit for the DVD+RW/+R. It consists of a 3-D actuator for focusing, radial tracking and tilt correction.

- 650nm laser for DVD
- 780nm laser for CD

On the interconnecting flex several electrical components are mounted.

- Elantec: programmable laser diode power driver and write strategy IC
- Paedic: integrated photo detector with programmable gain pre-amplifier
- Eeprom: containing a number of values representing adjustments belonging to the OPU

The laser control and diode signal processor ICs together with an Eeprom are mounted on the OPU flex.
The laser control IC generates the DVD laser read and writing signals needed for reading DVD discs and writing DVD+RW/+R discs (write strategies of DVD+RW/+R discs).
The diode signal processor is an analogue pre-processor adapted for the CD and CD-R/RW read function.
The Eeprom contains information about writing current, writing strategies and other parameters belonging to the OPU.

Motor and Servo drivers

The disc, tray and sledge motors are driven by a one-chip motor driver SA56202 [7402] while the 3-D actuator is driven &

control by a 4-channe BTL driver BA5995FM [7409] and some low power Ops amplifier LM358D [7401], [7403] and [7405].

9.3.4 Backend Digital part

General
The LECO IC is bascially the Chrysalis but it supports only one IDE Bus resulting in a smaller footprint.

Record Mode

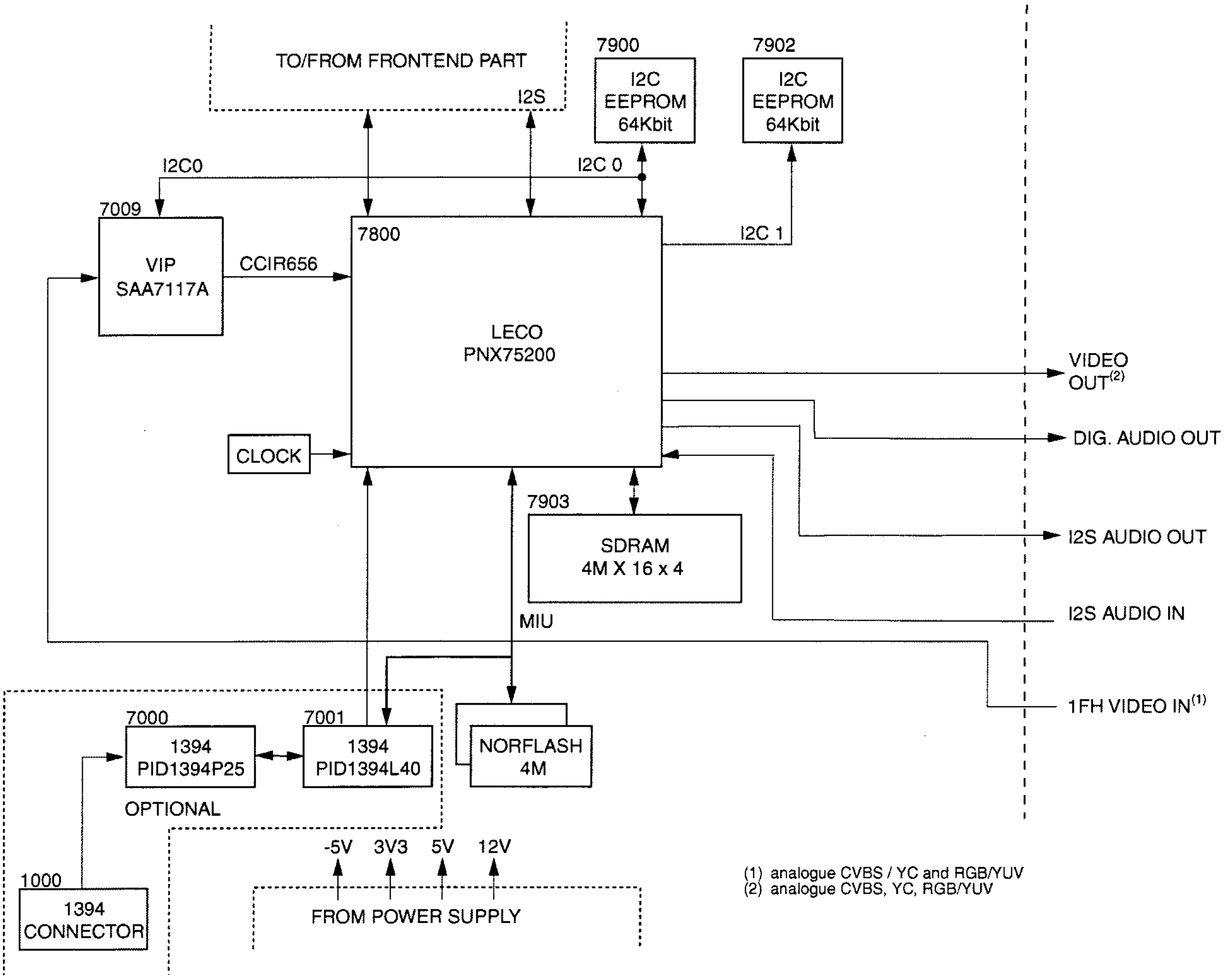

TO/FROM FRONTEND PART
I2S
7900
I2C EEPROM 64Kbit
7902
I2C EEPROM 64Kbit
I2C0
I2C 0
7009
VIP SAA7117A
CCIR656
7800
LECO PNX75200
I2C 1
CLOCK
7903
SDRAM 4M X 16 x 4
MIU
VIDEO OUT(2)
DIG. AUDIO OUT
I2S AUDIO OUT
I2S AUDIO IN
1FH VIDEO IN(1)
7000
1394 PID1394P25
7001
1394 PID1394L40
NORFLASH 4M
OPTIONAL
1000
1394 CONNECTOR
-5V 3V3 5V 12V
FROM POWER SUPPLY
(1) analogue CVBS / YC and RGB/YUV
(2) analogue CVBS, YC, RGB/YUV

Figure 9-10 Lecolite Block

Video Part
The analogue video input signals CVBS, YC and YUV/RGB (RGB for Euro and YUV for USA) from the MOBO analog board are routed from connector [1902] to IC [7009] SAA7117A , Video Input Processor.
The digital video input signals are routed from the DV-in connector [1000] via ICs [7000], 1394 PHY and [7001] 1394 LINK to Leco PNX7520 [7800].
The multi-standard Video Input Processor VIP, [7009] encodes the analogue video to digital stream (CCIR656 format). It provides filtering of the analogue signals and separation of luminance and chrominance by a comb filter. The ourput stream), is then routed to the Leco IC [7800]. This IC encodes and decodes the digital video stream into/from MPEG2 format.

Audio Part
I^2S audio is sent from the MOBO analog board to the Leco IC [7800] via connector [1903]. The Leco IC [7800] compresses the I^2S audio data into an Dolby Digital audio stream.

Front-end I^2S
Leco IC [7800] interfaces directly with the Centaurus [7500] and buffers the in- and out-going data streams.

In the Leco IC [7800], the video MPEG2 stream and the audio AC3 stream are multiplexed into an I^2S stream. The serial data are sent to the Centaurus [7500] for recording.

Playback Mode
During playback, the serial data from the Centaurus [7500] is going directly to the Leco IC [7800] via the serial front-end I^2S interface. The Leco IC [7800] outputs the followings:

- analogue video RGB, YC, CVBS on connector [1902].
- I^2S audio (PCM format) on connector [1903].
- SPDIF audio (digital audio output) on connector [1900].

Clock Distribution

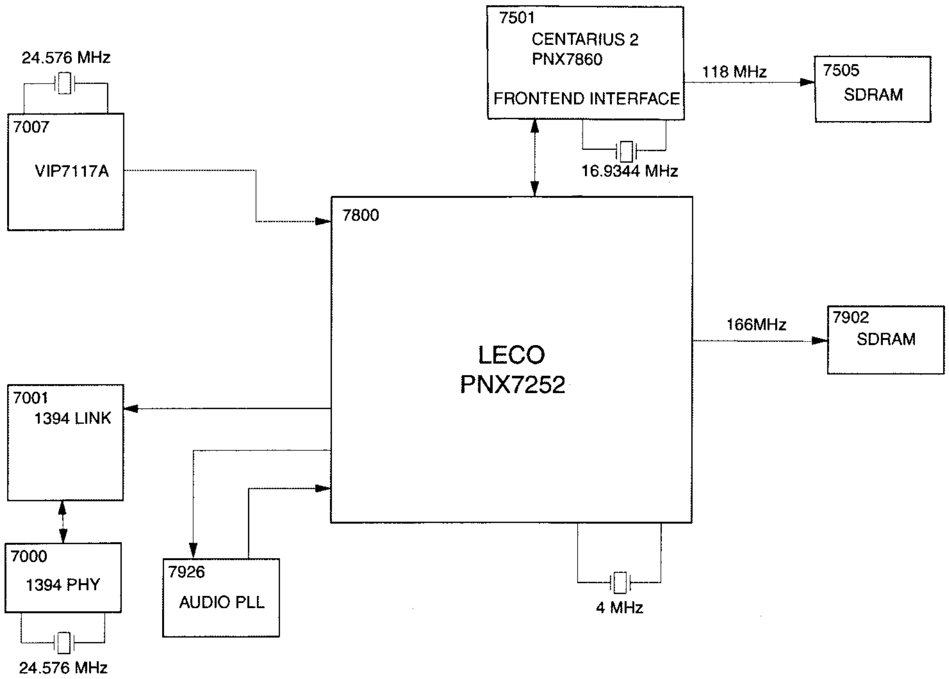

24.576 MHz
7007
VIP7117A
7501
CENTARIUS 2
PNX7860
FRONTEND INTERFACE
118 MHz
7505
SDRAM
16.9344 MHz
7800
LECO
PNX7252
166MHz
7902
SDRAM
7001
1394 LINK
7000
1394 PHY
24.576 MHz
7926
AUDIO PLL
4 MHz

Figure 9-11 Lecolite Clock

System clocks:

- PNX7252 [7800], pins T8 and N10 : 4MHz provided by the crystal oscillator [7926]
- SAA7117A [7009], pins A3 and B4 : 24.576 MHz provided by crystal [1002]
- SDRAM and [7903], pin 38 : 133MHz provided by PNX7252
- 1394-LINK [7001], pin 88 : 49: 152MHz provided by 1394-PHY
- 1394-PHY [7000], pin 59 and 60 : 24.576MHz provided by crystal [1001]
- SDRAM [7505], pin 35: 118MHz provided by Centaurus [7501]
- Centaurus [7501], pinV1/V2: 16.9344MHz provided by crystal

Memory

Several memories are used on the Leco IC [7800]:

- EEPROM [7902] : this memory contains all the necessary boot parameters of the board
- EEPROM [7900] : this memory contains all the necessary parameters for the application
- FLASH [7904] : this memory contains the application, diagnosis and service software

Reset

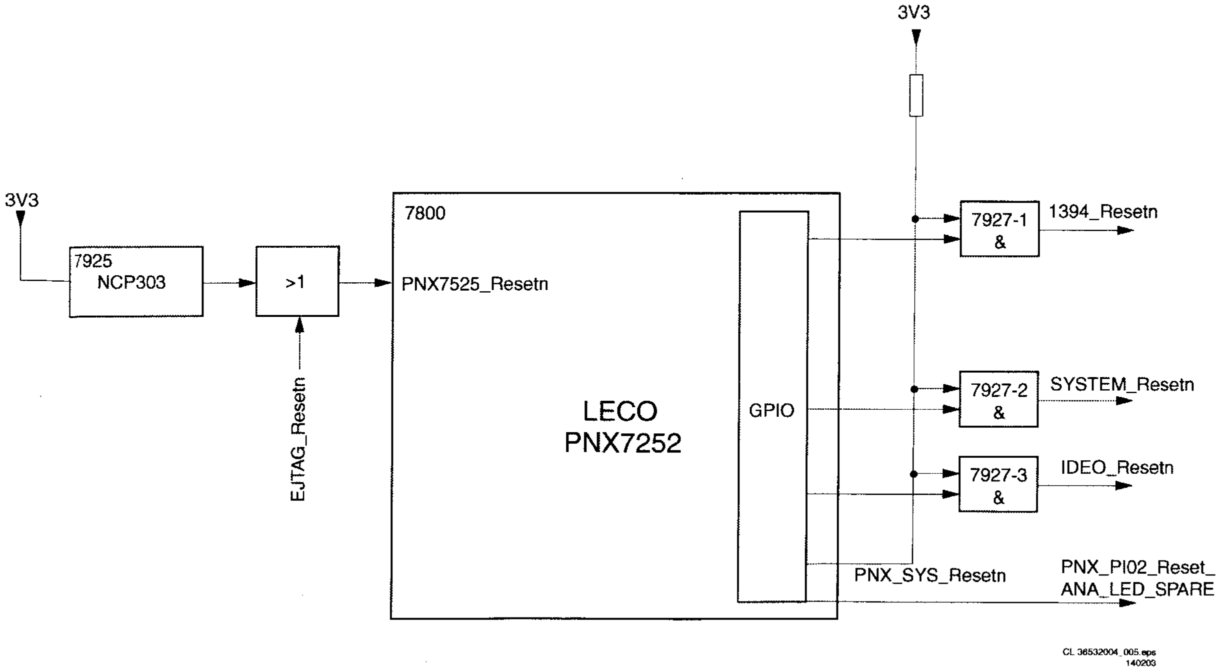

3V3
3V3
7925
NCP303
>1
EJTAG_Resetn
7800
PNX7525_Resetn
LECO
PNX7252
GPIO
7927-1
&
1394_Resetn
7927-2
&
SYSTEM_Resetn
7927-3
&
IDEO_Resetn
PNX_SYS_Resetn
PNX_PI02_Reset_
ANA_LED_SPARE
CL 36532004_005.eps
140203

Figure 9-12 Lecolite Reset

Upon power up, rest IC NCP303LSN290 [7925] provides a reset pulse to Leco IC PNX7252. This pulse is also generated whenever power supply dips below 2.9V for a certain amount of time. Leco can also be reset by via EJTAG for SW development purpose. After reset is released, the Leco IC will operate 4 other reset lines. 1394_RESETN resets the 1394 physiacl and link ICs. SYSTEM_RESETN, resets the flash and enable the VIP. IDEO_RESETN will reset the Centaurus 2 IC. The final line, PNX_P102_ORESET_ANA_LED_SPARE resets the ASP found on the MOBO board.

I^2C Bus

The Leco [7800] is the master of all the I^2C bus (during reset, external I^2C masters are allowed). The following ICs are controlled by the I^2C bus:

- [7902] Boot Eeprom
- [7900] NVRAMs
- [7009] VIP

and on the MOBO board

- [1700] Tuner
- [7410] Video Switch
- [7600] MSP

Audio IO Connector [1903]

The Audio In/Out (AIO) connector is used to interchange digital audio signals between MOBO Analog and FEBE Backend.

Video IO Connector [1902]

The Video In/Out (VIO) connector is used to interchange analogue video signals between MOBO Analog and FEBE Backend portion.

COMM Connector [1912]

This connector carries the I2C bus and reset line to the MOBO amongst other signal.

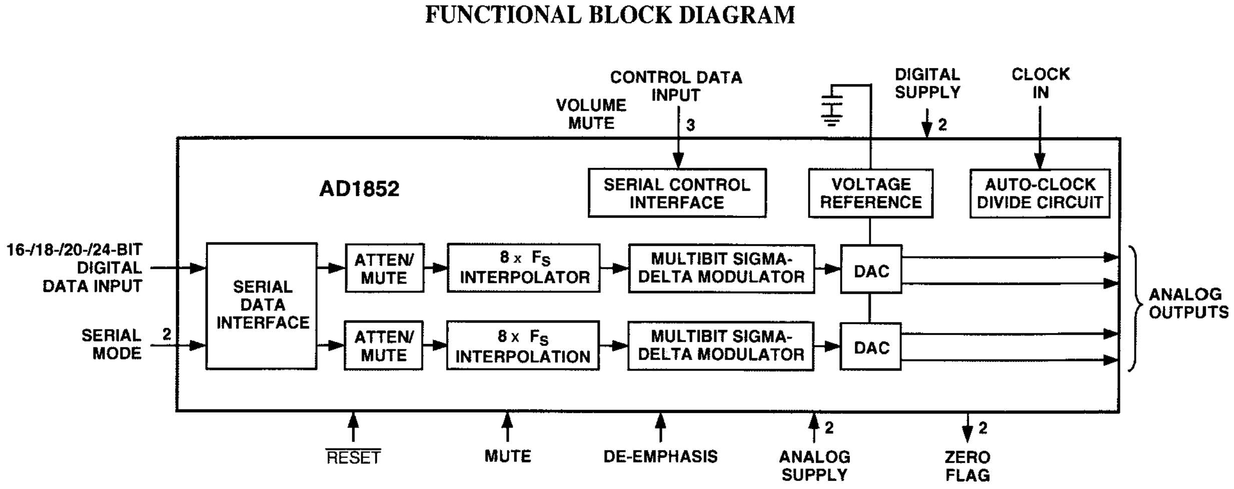
9.3.5 Service UART Interface

Transistors 7928,7930 and 7950 are used to make a level conversion between LVTTL and 5V (compatible with most RS232 interfaces) and vice versa. The control line PNX_PIOR_SERVICE_MODE_1394_ POWERDOWN2 is used to activate service and diagnostic SW at start up. The connectivity is provided via an external service tool.

9.4 IC Descriptions

9.4.1 MOBO Board

IC7004: AD1852 MOBO Board, Digital to Analoque Converter


FUNCTIONAL BLOCK DIAGRAM
CONTROL DATA INPUT
VOLUME MUTE
3
DIGITAL SUPPLY
2
CLOCK IN
AD1852
SERIAL CONTROL INTERFACE
VOLTAGE REFERENCE
AUTO-CLOCK DIVIDE CIRCUIT
16-/18-/20-/24-BIT DIGITAL DATA INPUT
SERIAL MODE
2
SERIAL DATA INTERFACE
ATTEN/ MUTE
8 x FS INTERPOLATOR
MULTIBIT SIGMA-DELTA MODULATOR
DAC
ATTEN/ MUTE
8 x FS INTERPOLATION
MULTIBIT SIGMA-DELTA MODULATOR
DAC
ANALOG OUTPUTS
RESET
MUTE
DE-EMPHASIS
2
ANALOG SUPPLY
2
ZERO FLAG

*Patents Pending

Figure 9-13

PIN FUNCTION DESCRIPTIONS

Pin	Input /Output	Pin Name	Description
1	I	DGND	Digital Ground.
2	I	MCLK	Master Clock Input. Connect to an external clock source at either 256 F_S, 384 F_S, 512 F_S, 768 F_S, or 1024 F_S.
3	I	CLATCH	Latch Input for Control Data. This input is rising-edge sensitive.
4	I	CCLK	Control Clock Input for Control Data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated.
5	I	CDATA	Serial Control Input, MSB first, containing 16 bits of unsigned data per channel. Used for specifying channel-specific attenuation and mute.
6		NC	No Connect.
7	I	192/48	Selects 48 kHz (LO) or 192 kHz Sample Frequency.
8	O	ZEROR	Right Channel Zero Flag Output. This pin goes HI when Right Channel has no signal input for more than 1024 LR Clock Cycles.
9	I	DEEMP	De-Emphasis. Digital de-emphasis is enabled when this input signal is HI. This is used to impose a 50 µs/15 µs response characteristic on the output audio spectrum at an assumed 44.1 kHz sample rate. Curves for 32 kHz and 48 kHz sample rates may be selected via SPI control register.
10	I	96/48	Selects 48 kHz (LO) or 96 kHz Sample Frequency.
11, 15	I	AGND	Analog Ground.
12	O	OUTR+	Right Channel Positive Line Level Analog Output.
13	O	OUTRD	Right Channel Negative Line Level Analog Output.
14	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 µF and 0.1 µF capacitors to the AGND.
16	O	OUTLD	Left Channel Negative Line Level Analog Output.
17	O	OUTL+	Left Channel Positive Line Level Analog Output.
18	I	AVDD	Analog Power Supply. Connect to Analog 5 V Supply.
19		FILTB	Filter Capacitor Connection. Connect 10 µF capacitor to AGND (Pin 15).
20	I	IDPM1	Input Serial Data Port Mode Control One. With IDPM0, defines 1 of 4 serial modes.
21	I	IDPM0	Input Serial Data Port Mode Control Zero. With IDPM1, defines 1 of 4 serial modes.
22	O	ZEROL	Left Channel Zero Flag Output. This pin goes HI when Left Channel has no signal input for more than 1024 LR Clock Cycles.
23	I	MUTE	Mute. Assert HI to mute both stereo analog outputs. Deassert LO for normal operation.
24	I	RESET	Reset. The AD1852 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect HI for normal operation.
25	I	L/RCLK	Left/Right Clock Input for Input Data. Must run continuously.
26	I	BCLK	Bit Clock Input for Input Data. Need not run continuously; may be gated or used in a burst fashion.
27	I	SDATA	Serial Input, MSB first, containing two channels of 16, 18, 20, and 24 bits of twos complement data per channel.
28	I	DVDD	Digital Power Supply Connect to digital 5 V supply.

Figure 9-14

IC7008: UDA1361TS MOBO Board, Analoque to Digital Converter

BLOCK DIAGRAM

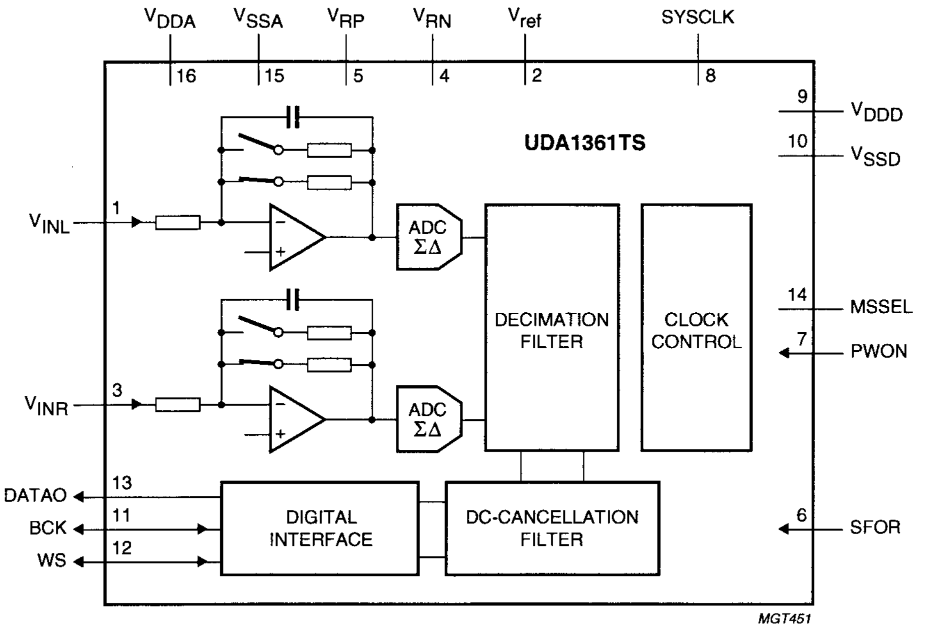

VDDA
VSSA
VRP
VRN
Vref
SYSCLK
16
15
5
4
2
8
9
VDDD
10
VSSD
UDA1361TS
VINL
1
ADC ΣΔ
DECIMATION FILTER
CLOCK CONTROL
14
MSSEL
7
PWON
VINR
3
ADC ΣΔ
DATAO
13
BCK
11
WS
12
DIGITAL INTERFACE
DC-CANCELLATION FILTER
6
SFOR
MGT451

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{INL}	1	left channel input
V_{ref}	2	reference voltage
V_{INR}	3	right channel input
V_{RN}	4	negative reference voltage
V_{RP}	5	positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock 256, 384, 512 or 768f_s
V_{DDD}	9	digital supply voltage
V_{SSD}	10	digital ground
BCK	11	bit clock input/output
WS	12	word select input/output
DATAO	13	data output
MSSEL	14	master/slave select
V_{SSA}	15	analog ground
V_{DDA}	16	analog supply voltage

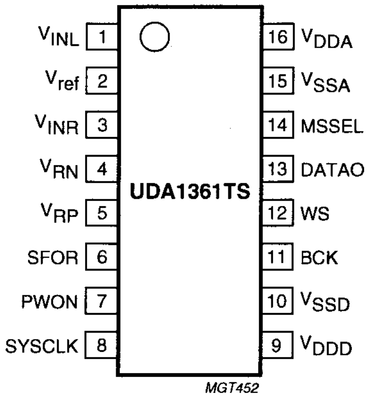
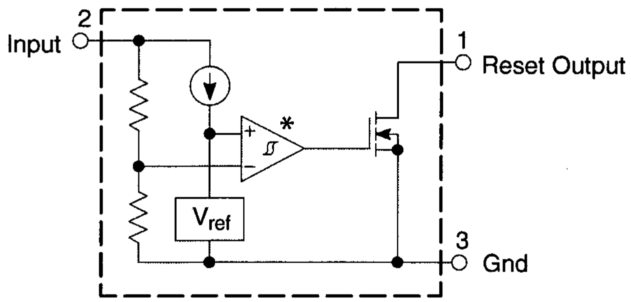

VINL 1
Vref 2
VINR 3
VRN 4
VRP 5
SFOR 6
PWON 7
SYSCLK 8
UDA1361TS
16 VDDA
15 VSSA
14 MSSEL
13 DATAO
12 WS
11 BCK
10 VSSD
9 VDDD
MGT452

Fig.2 Pin configuration.

IC7100 NCP301LSNxx MOBO Board, Reset Circuit

NCP301xSNxxT1
Open Drain Output Configuration


2
Input
1
Reset Output
*
Vref
3
Gnd

* The representative block diagrams depict active low reset output ‘L’ suffix devices. The comparator inputs are interchanged for the active high output ‘H’ suffix devices.

This device contains 25 active transistors.

Figure 1. Representative Block Diagrams

Figure 9-16

IC7107 TMP87CM74AF MOBO Board, Microprocessor

Block Diagram

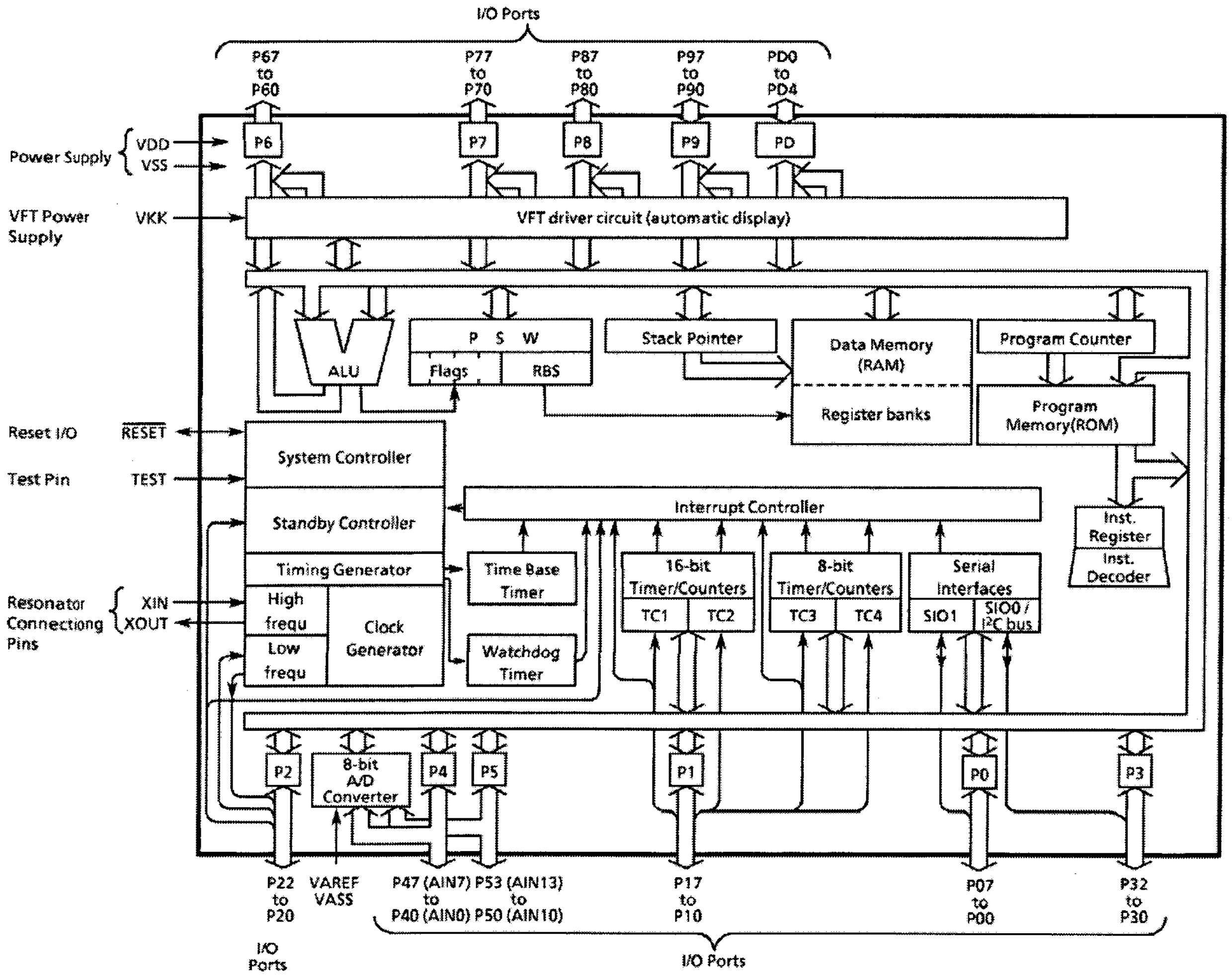

I/O Ports
P67 to P60
P77 to P70
P87 to P80
P97 to P90
PD0 to PD4
Power Supply
VDD
VSS
P6
P7
P8
P9
PD
VFT Power Supply
VKK
VFT driver circuit (automatic display)
ALU
P S W
Flags
RBS
Stack Pointer
Data Memory (RAM)
Register banks
Program Counter
Program Memory(ROM)
Reset I/O
RESET
Test Pin
TEST
System Controller
Standby Controller
Interrupt Controller
Inst. Register
Inst. Decoder
Timing Generator
Time Base Timer
16-bit Timer/Counters
TC1
TC2
8-bit Timer/Counters
TC3
TC4
Serial Interfaces
SIO1
SIO0 / I²C bus
Resonator Connectiong Pins
XIN
XOUT
High frequ
Low frequ
Clock Generator
Watchdog Timer
P2
8-bit A/D Converter
P4
P5
P1
P0
P3
P22 to P20
VAREF VASS
P47 (AIN7) to P40 (AIN0)
P53 (AIN13) to P50 (AIN10)
P17 to P10
P07 to P00
P32 to P30
I/O Ports
I/O Ports

Figure 9-17

Pin Function

Pin Name	Input / Output	Function	
P07 to P03	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as a SIO input/output, an External interrupt input, a timer/counter input, the latch must be set to "0". When used as a PPG output or divider output, the latch must be set to "1".	
P02 (SO1)	I/O (Output)		SIO1 serial data Output
P01 (SI1)	I/O (Input)		SIO1 serial data Input
P00 ($\overline{SCK1}$)	I/O (I/O)		SIO1 serial clock input/output
P17 (INT4/TC3)	I/O (Input)		External interrupt input 4 or Timer/Counter 3 input
P16 (INT2)			External interrupt input 2
P15 (INT3/TC1)			External interrupt input 3 or Timer/Counter 1 input
P14 (TC4/$\overline{PDO}$/$\overline{PWM}$)	I/O (I/O)		Timer counter 4 input or 8-bit programmable divider output or 8-bit PWM output
P13 ($\overline{DVO}$)	I/O (Output)		Divider output
P12 (TC2/$\overline{PPG}$)	I/O (I/O)		Timer counter 2 input or Programmable pulse generator output
P11 (INT1)	I/O (Input)		External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as input port, or external interrupt input, STOP mode release signal input, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$/$\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P32 ($\overline{SCK0}$)	I/O (I/O)	3-bit programmable input/output ports (Sink open drain). Each bit of these ports can be individually configured as an input or an output under software control. When used as a I^{2}C input/output, the latch must be set to "1".	SIO0 serial clock input/output
P31 (SDA/SO0)	I/O (I/O/Output)		I^{2}Cbus serial data input/output or SIO0 serial data output
P30 (SCL/SI0)	I/O (I/O/Input)		I^{2}Cbus serial clock input/output or SIO0 serial data Input
P47 (AIN7) to P40 (AIN0)	I/O (Input)	8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as a analog input, the P4CR must be set to "0".	A/D converter analog inputs
P53 (AIN13) to P50 (AIN10)	I/O (Input)	4-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as a analog input, the P5CR must be set to "0".	A/D converter analog inputs
P67 (V7) to P60 (V0)	I/O (Output)	Four 8-bit high brackdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	VFT driver outputs
P77 (V15) to P70 (V8)			
P87 (V23) to P80 (V16)			
P97 (V31) to P90 (V24)			
PD4 (V36) toPD0 (V32)	I/O (Output)	5-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	

Figure 9-18

Pin Name	Input / Output	Function
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.
$\overline{\text{RESET}}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset outputted.
TEST	Input	Test pin for out-going test. Be tied to low.
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)
VKK		VFT driver power supply
VAREF, VASS		Analog reference voltage inputs (High, Low)

Figure 9-19

IC7311 TEA 1507 MOBO Board, Power Supply Control

BLOCK DIAGRAM

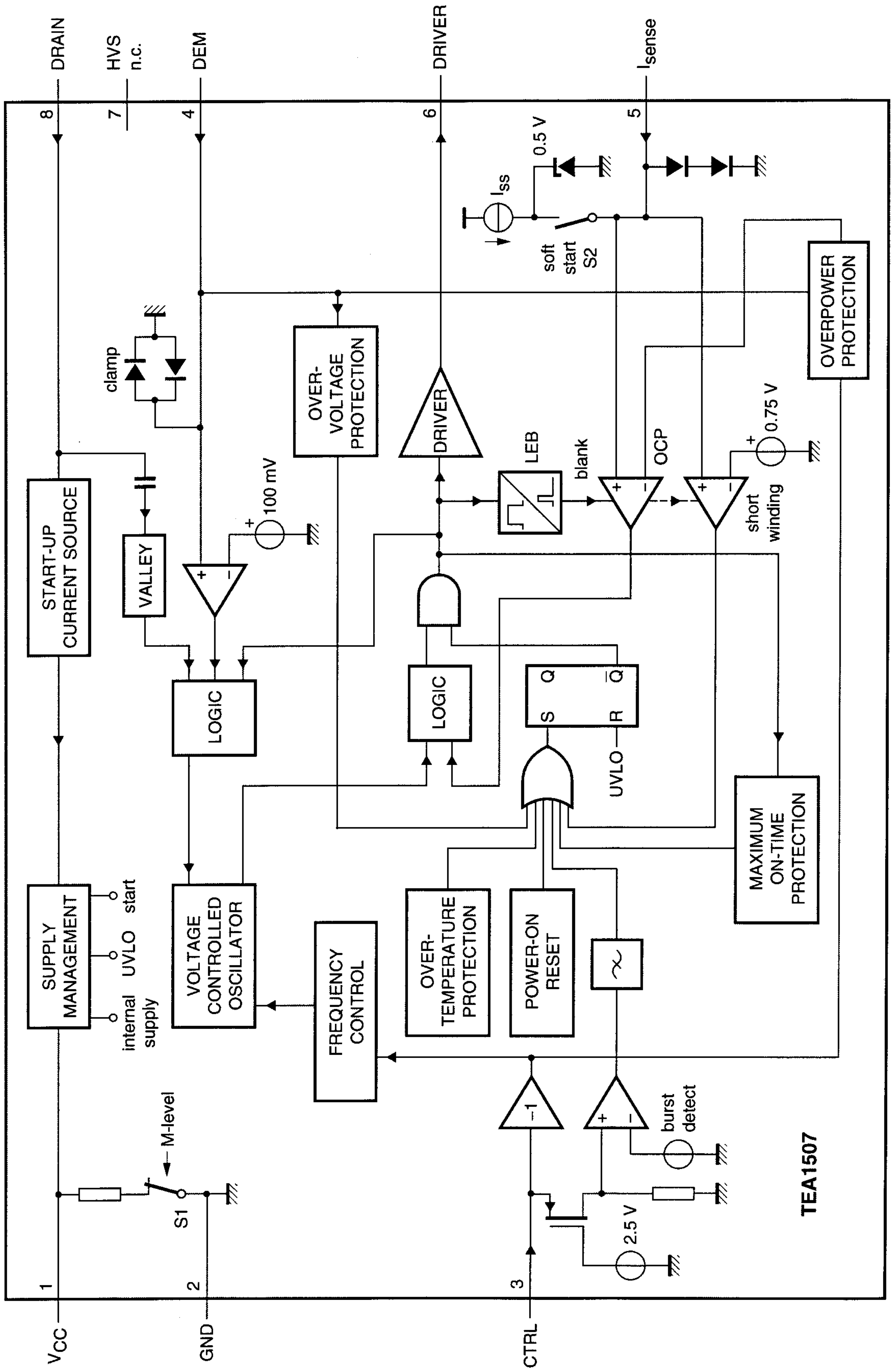

DRAIN
HVS
n.c.
DEM
DRIVER
I_{sense}
8
7
4
6
5
MGU230
0.5 V
I_{ss}
soft start S2
clamp
OVER-VOLTAGE PROTECTION
DRIVER
OVERPOWER PROTECTION
0.75 V
LEB
blank
OCP
short winding
100 mV
START-UP CURRENT SOURCE
VALLEY
LOGIC
LOGIC
S
Q
R
$\bar{Q}$
UVLO
MAXIMUM ON-TIME PROTECTION
SUPPLY MANAGEMENT
start
UVLO
internal supply
VOLTAGE CONTROLLED OSCILLATOR
FREQUENCY CONTROL
OVER-TEMPERATURE PROTECTION
POWER-ON RESET
M-level
S1
−1
burst detect
2.5 V
TEA1507
1
2
3
V_{CC}
GND
CTRL

Fig.2 Block diagram.

Figure 9-20

IC7410: STV6618 MOBO Board, Video Switch Matrix

1.2 Pin Description

Pin No.	Symbol	Description
1	Y/CVBSIN_TUN	Y/CVBS Input from Tuner
2	DIGOUT3	Digital Output Pin 3
3	GND1	Ground Supply 1 for Video Inputs
4	CVBSIN_ENC	CVBS Input from Encoder
5	DECV	Video decoupling capacitor
6	CIN_ENC	Chroma Input from Encoder
7	YIN_ENC	Y Input from Encoder
8	V_{CC}	+5 V Power Supply for Video Inputs
9	R/PR/CIN_ENC	Red or Pr or Chroma Input from Encoder
10	G/YIN_ENC	Green or Y Input from Encoder
11	B/PBIN_ENC	Blue or Pb Input from Encoder
12	GND2	Ground Supply 2 for Video Inputs
13	B/PBIN_AUX	Blue or Pb Input from Auxiliary (SCART2 or external Cinch)
14	DIGOUT4	Digital Output Pin 4
15	G/YIN_AUX	Green or Y Input from Auxiliary (SCART2 or external Cinch)
16	DIGOUT5	Digital Output Pin 5
17	R/PR/CIN_AUX	Red or Pr or Chroma input from Auxiliary (SCART2 or external Cinch)
18	DIGOUT6	Digital Output Pin 6
19	Y/CVBSIN_AUX	Y/CVBS Input from Auxiliary (SCART2 or external Cinch)
20	VCCB_REC	Video Output Recorder Buffer Supply Pin
21	Y/CVBSOUT_REC	Y/CVBS Output to Recorder
22	GNDB_REC	Ground Supply for Recorder Buffer
23	COUT_AUX	Chroma Output to Auxiliary (SCART2 or external Cinch)
24	VCCB1	Video Output Buffer Supply Pin
25	Y/CVBSOUT_AUX	Y/CVBS Output to Auxiliary (SCART2 or external Cinch)
26	GNDB	Ground Supply for Video Buffer
27	B/PBOUT_TV	Blue or Pb Output to TV (SCART1 or external Cinch)
28	C_GATE	External Transistor Command for Bidirectinnal B/C SCART I/O
29	G/YOUT_TV	Green or Y Output to TV (SCART1 or external Cinch)
30	VCCB2	Video Buffer
31	R/PR/COUT_TV	Red or Pr or Chroma Output to TV (SCART1 or external Cinch)
32	VCCB3	Video Output Buffer Supply Pin
33	Y/CVBSOUT_TV	Y/CVBS Output to TV (SCART1 or external Cinch)
34	FBOUT_TV	Fast Blanking Output to TV (SCART1)
35	FBIN_AUX	Fast Blanking Input from Auxiliary (SCART2)

Figure 9-21

Pin No.	Symbol	Description
36	VDD	+5 V Digital Power Supply
37	SCL	I²C Bus Clock
38	SDA	I²C Bus Data
39	GNDD	Digital Ground Supply
40	CIN_TV	Chroma Input from TV (SCART1 or external Cinch)
41	Y/CVBSIN_TV	Y/CVBS Input from TV (SCART1 or external Cinch)
42	DIGOUT1	Digital Output Pin 1
43	CIN_TUN	Chroma Input from Tuner
44	DIGOUT2	Digital Output Pin 2

Figure 2: STV6618 Input/Output Diagram

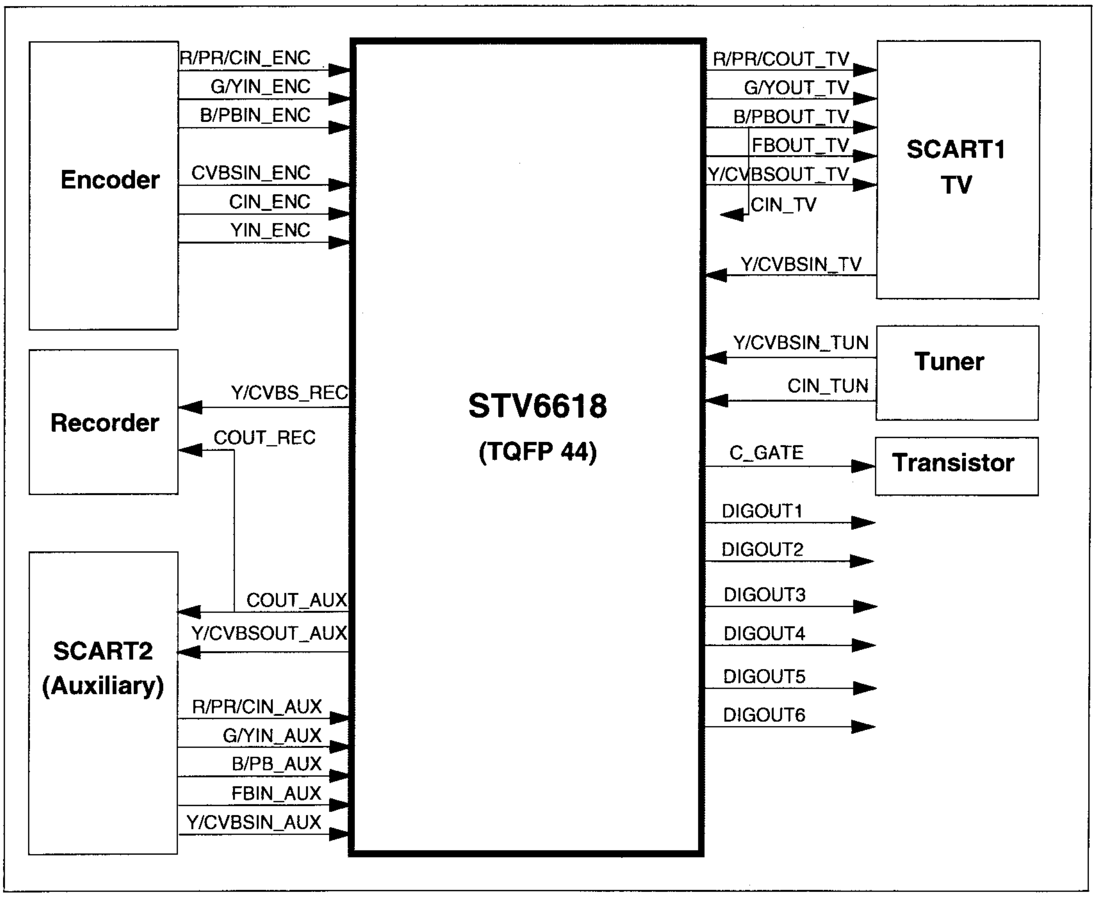

Encoder
R/PR/CIN_ENC
G/YIN_ENC
B/PBIN_ENC
CVBSIN_ENC
CIN_ENC
YIN_ENC
Recorder
Y/CVBS_REC
COUT_REC
SCART2 (Auxiliary)
COUT_AUX
Y/CVBSOUT_AUX
R/PR/CIN_AUX
G/YIN_AUX
B/PB_AUX
FBIN_AUX
Y/CVBSIN_AUX
STV6618
(TQFP 44)
R/PR/COUT_TV
G/YOUT_TV
B/PBOUT_TV
FBOUT_TV
Y/CVBSOUT_TV
CIN_TV
Y/CVBSIN_TV
SCART1 TV
Y/CVBSIN_TUN
CIN_TUN
Tuner
C_GATE
Transistor
DIGOUT1
DIGOUT2
DIGOUT3
DIGOUT4
DIGOUT5
DIGOUT6

Figure 9-22

Figure 3: STV6618 Block Diagram

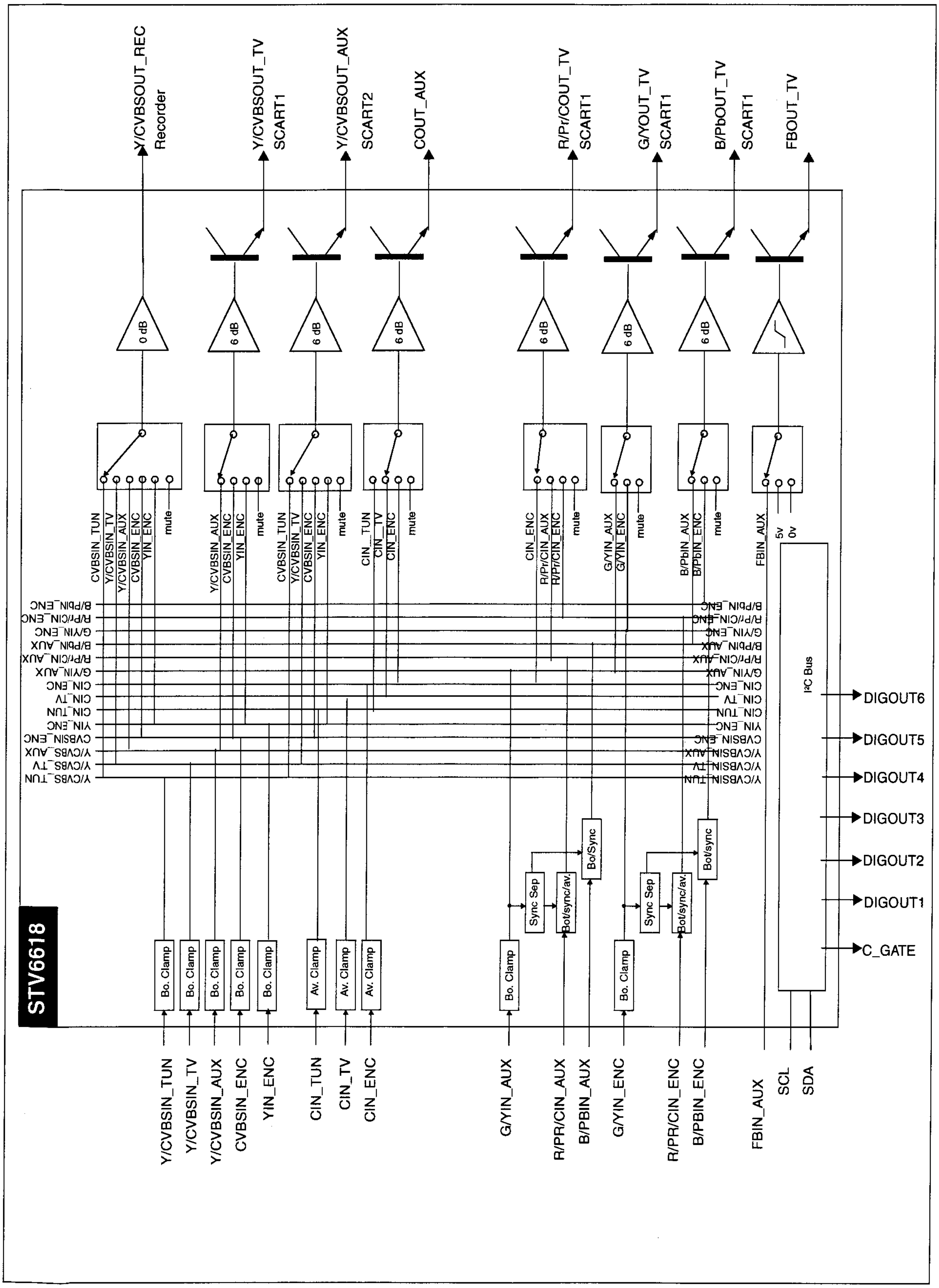

Y/CVBSOUT_REC
Recorder
Y/CVBSOUT_TV
SCART1
Y/CVBSOUT_AUX
SCART2
COUT_AUX
R/Pr/COUT_TV
SCART1
G/YOUT_TV
SCART1
B/PbOUT_TV
SCART1
FBOUT_TV
0 dB
6 dB
CVBSIN_TUN
Y/CVBSIN_TV
Y/CVBSIN_AUX
CVBSIN_ENC
YIN_ENC
CIN_TUN
CIN_TV
CIN_ENC
R/Pr/CIN_AUX
R/Pr/CIN_ENC
G/YIN_AUX
G/YIN_ENC
B/PbIN_AUX
B/PbIN_ENC
FBIN_AUX
5v
0v
mute
I²C Bus
DIGOUT6
DIGOUT5
DIGOUT4
DIGOUT3
DIGOUT2
DIGOUT1
C_GATE
Bo. Clamp
Av. Clamp
Sync Sep
Bot/sync/av.
Bo/Sync
Bot/sync
STV6618
Y/CVBSIN_TUN
Y/CVBSIN_TV
Y/CVBSIN_AUX
CVBSIN_ENC
YIN_ENC
CIN_TUN
CIN_TV
CIN_ENC
G/YIN_AUX
R/PR/CIN_AUX
B/PBIN_AUX
G/YIN_ENC
R/PR/CIN_ENC
B/PBIN_ENC
FBIN_AUX
SCL
SDA

Figure 9-23

IC7411: NJM2234 MOBO Board, 3-Input Video Switch

■ BLOCK DIAGRAM

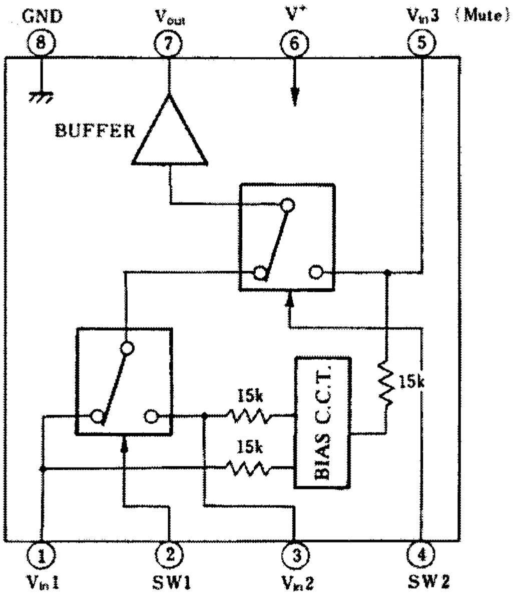

GND
8
V_{out}
7
V^+
6
$V_{in}3$ (Mute)
5
BUFFER
15k
15k
15k
BIAS C.C.T.
1
$V_{in}1$
2
SW1
3
$V_{in}2$
4
SW2

Figure 9-24

INPUT CONTROL SIGNAL – OUTPUT SIGNAL

SW 1	SW 2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

Figure 9-25

IC7416: NJM2235 MOBO Board, 3-Input Video Switch

BLOCK DIAGRAM

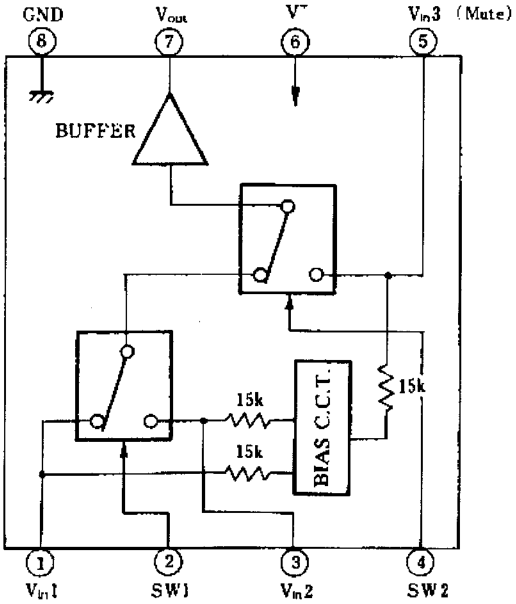

GND
8
V_{out}
7
V^-
6
$V_{in}3$ (Mute)
5
BUFFER
15k
15k
15k
BIAS C.C.T.
1
$V_{in}1$
2
SW1
3
$V_{in}2$
4
SW2

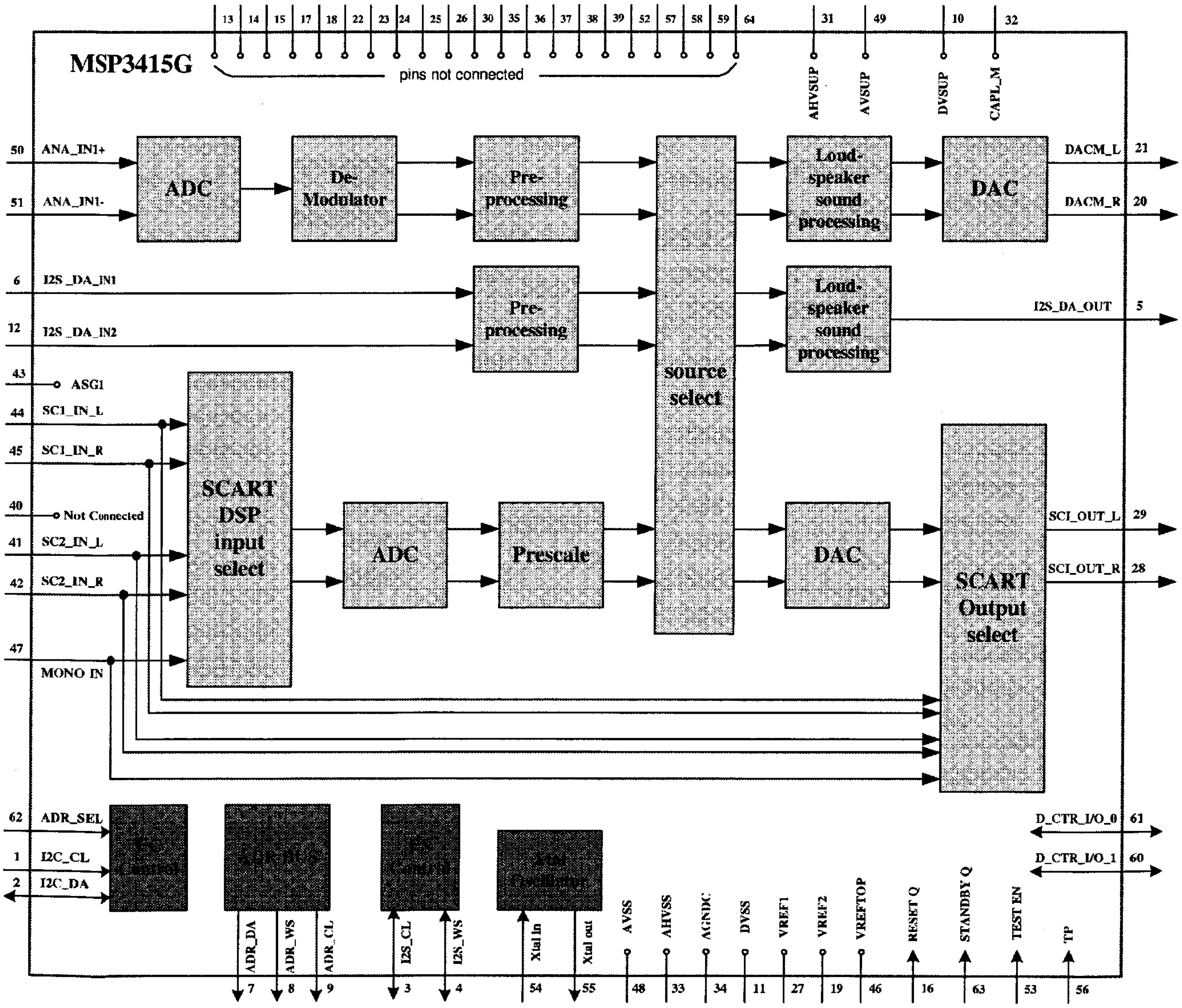
Figure 9-26

INPUT CONTROL SIGNAL – OUTPUT SIGNAL

SW1	SW2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

Figure 9-27

IC7600: MSP3415G MOBO Board, Multi Sound Processor



MSP3415G
13
14
15
17
18
22
23
24
25
26
30
35
36
37
38
39
52
57
58
59
64
pins not connected
31
49
10
32
AHVSUP
AVSUP
DVSUP
CAPL_M
50
ANA_IN1+
51
ANA_IN1-
ADC
De-Modulator
Pre-processing
source select
Loud-speaker sound processing
DAC
DACM_L
21
DACM_R
20
6
I2S_DA_IN1
12
I2S_DA_IN2
Pre-processing
Loud-speaker sound processing
I2S_DA_OUT
5
43
ASG1
44
SC1_IN_L
45
SC1_IN_R
40
Not Connected
41
SC2_IN_L
42
SC2_IN_R
47
MONO IN
SCART DSP input select
ADC
Prescale
DAC
SCART Output select
SC1_OUT_L
29
SC1_OUT_R
28
62
ADR_SEL
1
I2C_CL
2
I2C_DA
I²C Control
ADR-BUS
I²S Control
Xtal Oscillator
D_CTR_I/O_0
61
D_CTR_I/O_1
60
ADR_DA
ADR_WS
ADR_CL
I2S_CL
I2S_WS
Xtal In
Xtal out
AVSS
AHVSS
AGNDC
DVSS
VREF1
VREF2
VREFTOP
RESET Q
STANDBY Q
TEST EN
TP
7
8
9
3
4
54
55
48
33
34
11
27
19
46
16
63
53
56

Figure 9-28

IC7803: NJM2267 MOBO Board, Dual 6dB Video Amplifier

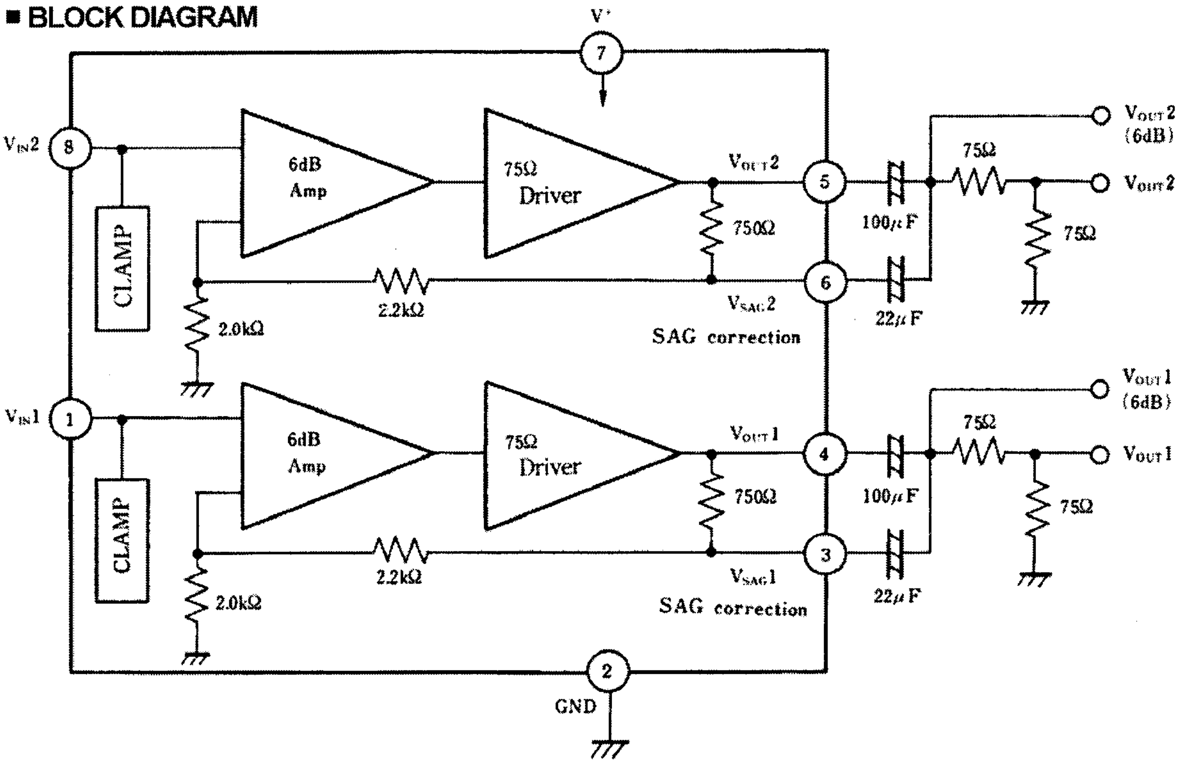

■ BLOCK DIAGRAM
V+
7
V_IN2
8
CLAMP
6dB Amp
75Ω Driver
V_OUT2
5
750Ω
6
2.2kΩ
2.0kΩ
V_SAG2
SAG correction
100μF
22μF
75Ω
V_OUT2 (6dB)
V_OUT2
75Ω
V_IN1
1
CLAMP
6dB Amp
75Ω Driver
V_OUT1
4
750Ω
3
2.2kΩ
2.0kΩ
V_SAG1
SAG correction
100μF
22μF
75Ω
V_OUT1 (6dB)
V_OUT1
75Ω
2
GND

Figure 9-29

9.4.2 FEBE Board

IC7008 / 7603 / 7607 / 7608, LD1117 FEBE Board, Voltage Regulator

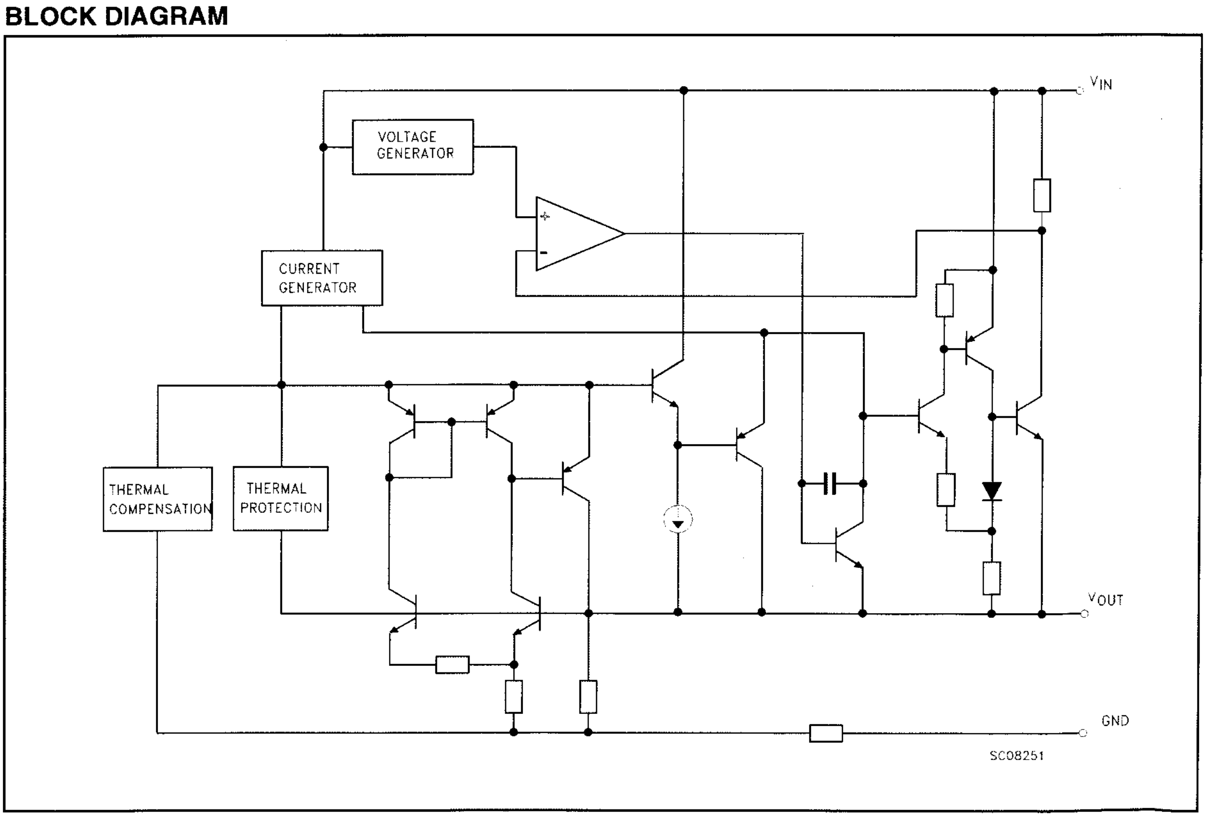

BLOCK DIAGRAM
VIN
VOLTAGE GENERATOR
+
-
CURRENT GENERATOR
THERMAL COMPENSATION
THERMAL PROTECTION
VOUT
GND
SC08251

Figure 9-30

IC7201, TZA1047: FEBE Baord, Analoque Processor

Block diagram

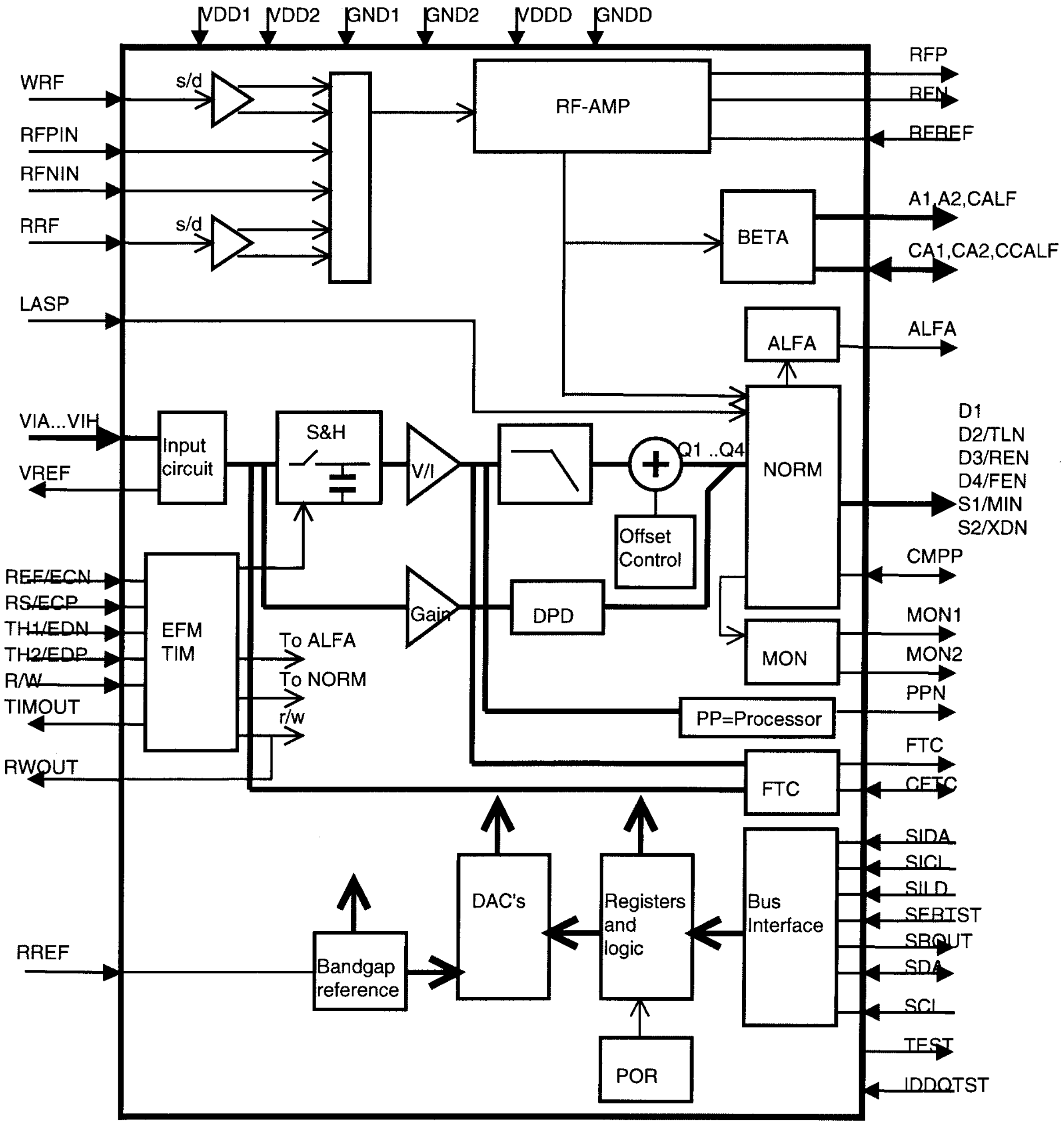

VDD1
VDD2
GND1
GND2
VDDD
GNDD
WRF
s/d
RFPIN
RFNIN
RRF
s/d
RF-AMP
RFP
RFN
RFREF
BETA
A1,A2,CALF
CA1,CA2,CCALF
LASP
ALFA
ALFA
VIA...VIH
VREF
Input circuit
S&H
V/I
Q1 ..Q4
Offset Control
NORM
D1
D2/TLN
D3/REN
D4/FEN
S1/MIN
S2/XDN
CMPP
REF/ECN
RS/ECP
TH1/EDN
TH2/EDP
R/W
TIMOUT
EFM TIM
Gain
DPD
To ALFA
To NORM
r/w
MON
MON1
MON2
PPN
PP=Processor
RWOUT
FTC
FTC
CFTC
SIDA
SICL
SILD
SEBIST
SBOUT
SDA
SCL
TEST
IDDQTST
DAC's
Registers and logic
Bus Interface
RREF
Bandgap reference
POR

Fig 1. TZA1047 Block Diagram

Figure 9-31

Pin description

Table 1: Pin description

Symbol	Pin	Description
VIH	1	Satellite segment H input
GND1	2	Ground
VIC	3	Central segment C input
VIB	4	Central segment B input
GND1	5	Ground
RFNIN	6	Inverse differential RF input / Single-ended RF read input
RFPIN	7	Differential RF input/ Single-ended RF write input
VDD1	8	Positive supply
VID	9	Central segment D input
VIA	10	Central segment A input
VDD1	11	Positive supply
VIE	12	Satellite segment E input
VIG	13	Satellite segment G input
RWOUT	14	R/W signal output
SDA	15	Data input/output I^2C
SCL	16	Clock input I^2C
SILD	17	Strobe line of serial bus interface
SIDA	18	Data line of serial bus interface
SICL	19	Clock line of serial bus interface
TIMOUT	20	EFMTIM test output
R/W	21	External Read/Write signal input
VDDD	22	Positive supply digital part
VSSD	23	digital ground
REF/ECN	24	Reference input for timing signals in EFMTIM bypass mode[1]/ Inverse EFM clock input[2]
RS/ECP	25	RF sampling signal[1]/ EFM clock input[2]
TH1/EDN	26	Segment sampling timing signal[1]/ Inverse EFM data input[2]
TH2/EDP	27	Segment sampling timing signal[1]/ EFM data input[2]
SERTST	28	Enable test mode (Tie to GND or leave open for normal operation)
VDD2	29	Positive supply voltage

Figure 9-32

Table 1: **Pin description** *(Continued)*

Symbol	Pin	Description
GND2	30	Supply ground
RFP	31	RF output voltage, positive
RFN	32	RF output voltage, negative
RFREF	33	Reference voltage for differential RF output common mode level
PPN	34	Output PP voltage
CFTC	35	FTC high pass filter capacitor
FTC	36	FTC output
GND1	37	Supply ground
CA1	38	Beta circuit external capacitor
CA2	39	Beta circuit external capacitor
CCALF	40	Beta circuit external capacitor
RREF	41	Reference resistor to ground
GND1	42	Supply ground
CMPP	43	MPP external capacitor
VDD1	44	Positive supply
MON1	45	Monitor output voltage
MON2	46	Monitor output voltage
S2/XDN	47	Servo output current
S1/MIRN	48	Servo output current
D4/FEN	49	Servo output current
D3/REN	50	Servo output current
D2/TLN	51	Servo output current
D1	52	Servo output current
IDDQTST	53	Select zero dissipation mode (tie to GND for normal operation)
CALF	54	RF average level signal
A2	55	RF bottom level signal
A1	56	RF top level signal
SROUT	57	shift register output for register test mode
ALFA	58	alfa output current
LASP	59	laser power setpoint signal
TEST	60	Test output
RRF	61	Single ended RF read input voltage

Figure 9-33

Table 1: **Pin description** *(Continued)*

Symbol	Pin	Description
WRF	62	Single ended RF write input voltage
VREF	63	PDIC reference voltage output
VIF	64	Satellite segment F input

[1] Only in EFM bypass mode

[2] EFM clock and data when not in EFM bypass mode.

Figure 9-34

IC7300, TZA1042: FEBE Baord, Laser Power Controller

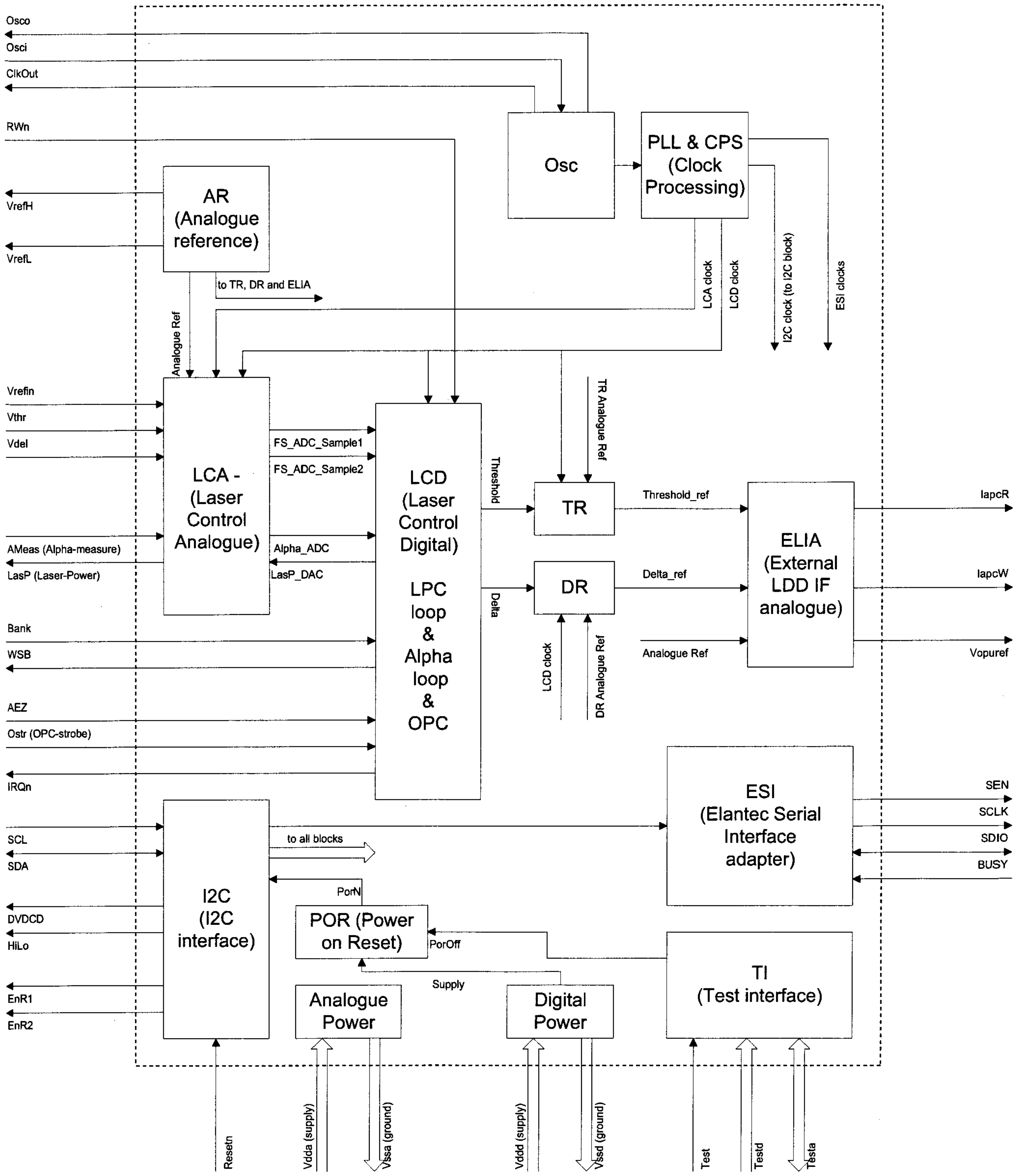

Osco
Osci
ClkOut
RWn
Osc
PLL & CPS (Clock Processing)
AR (Analogue reference)
VrefH
VrefL
to TR, DR and ELIA
LCA clock
LCD clock
I2C clock (to I2C block)
ESI clocks
Analogue Ref
Vrefin
Vthr
Vdel
FS_ADC_Sample1
FS_ADC_Sample2
LCA - (Laser Control Analogue)
LCD (Laser Control Digital)
LPC loop & Alpha loop & OPC
TR Analogue Ref
Threshold
TR
Threshold_ref
ELIA (External LDD IF analogue)
IapcR
AMeas (Alpha-measure)
LasP (Laser-Power)
Alpha_ADC
LasP_DAC
Delta
DR
Delta_ref
IapcW
Analogue Ref
Vopuref
LCD clock
DR Analogue Ref
Bank
WSB
AEZ
Ostr (OPC-strobe)
IRQn
ESI (Elantec Serial Interface adapter)
SEN
SCLK
SDIO
BUSY
SCL
SDA
to all blocks
PorN
I2C (I2C interface)
POR (Power on Reset)
PorOff
DVDCD
HiLo
Supply
EnR1
EnR2
Analogue Power
Digital Power
TI (Test interface)
Resetn
Vdda (supply)
Vssa (ground)
Vddd (supply)
Vssd (ground)
Test
Testd
Testa

Figure 9-35

Pin description

Symbol	Pin	Type	Drive /Thr.	Description
AEZ	1	I hy pd	T	Alpha Error Zero/Alpha Set Zero
V_{DDD3}	2	P	-	Digital Pad Supply
V_{SSD3}	3	P	-	Digital Pad Supply
CLOCKOUT	4	T	M	Buffered Oscillator Output
OSCO	5	AO	A	Output of inverting Amplifier that forms oscillator
OSCI	6	AI	A	Input of inverting Amplifier that forms oscillator
TEST1D	7	I pd	T	Test pin
AMEAS	8	AI	A	Alpha Measure – value of measured disk writing quality
V_{DDA1}	9	P	-	Analogue Supply
V_{SSA1}	10	P	-	Analogue Supply
LASP	11	AO	A	Laser Power – indicates power level
VREFL	12	AO	A	Bandgap Voltage Reference ground connection
VREFH	13	AO	A	Bandgap Voltage Reference output
VDEL	14	AI	A	Voltage input for Delta "laser power"
VTHR	15	AI	A	Voltage input for Threshold "laser power"
VOPUREF	16	AO	A	Reference Voltage for OPU
VREFIN	17	AI	A	Input Reference Voltage for Vthr and Vdel
V_{DDA2}	18	P	-	Analogue Supply
V_{SSA2}	19	P	-	Analogue Supply
TEST1A	20	AB	A	Test pin
IAPCW	21	AO	A	Current Output of Delta Reference
IAPCR	22	AO	A	Current Output of Threshold Reference
TEST2A	23	AB	A	Test pin
ENR2	24	T	M	Programmable Output Flag
ENR1	25	B pd	M/T	Device Initialisation/Programmable Output Flag (must be driven to VDD during reset)
DVDCD	26	T	M	Programmable Output Flag for indicating DVD/CD mode

Figure 9-36

Pin description...*continued*

Symbol	Pin	Type	Drive /Thr.	Description
IRQN	35	OD	M	Interrupt Request Not – active low interrupt request
OSTR	36	I hy pd	T	OPC Strobe – request step in alpha setpoint / Board test input
RESETN	37	I hy pd	T	Reset Not – active low reset input
RWN	38	B	M/T	Read/Write not – indicates power setpoints/Board test IO
V_{SSD2}	39	P	-	Digital Core Supply
V_{DDD2}	40	P	-	Digital Core Supply
BANK	41	I hy pd	T	CAV setpoint switching input signal / Board test IO
TEST2D	42	I pd	T	Test pin
SDA	43	BOD	M/T	I^2C Serial Data
SCL	44	I	T	I^2C Serial Clock

[1] All supply pins must be connected to the same external power supply voltage

[2] All inputs are 5V tolerant – i.e. they will drive the supply voltage (3.0-3.6V), but will work correctly when interface to a 5V drive device

[3] The pin type definition is given below:

PinType Definition Table

Type	Definition
I	input
O	output
OD	open drain
B	bi-directional
BOD	bi-directional open drain
T	tri-state output
AI	analog input
AO	analog output
AB	analog bi-directional
P	power connection
hy	hysteresis on input
pd	hysteresis on output

Figure 9-37

IC7402, SA56202 FEBE Board, Motor Drivers

PIN CONFIGURATION

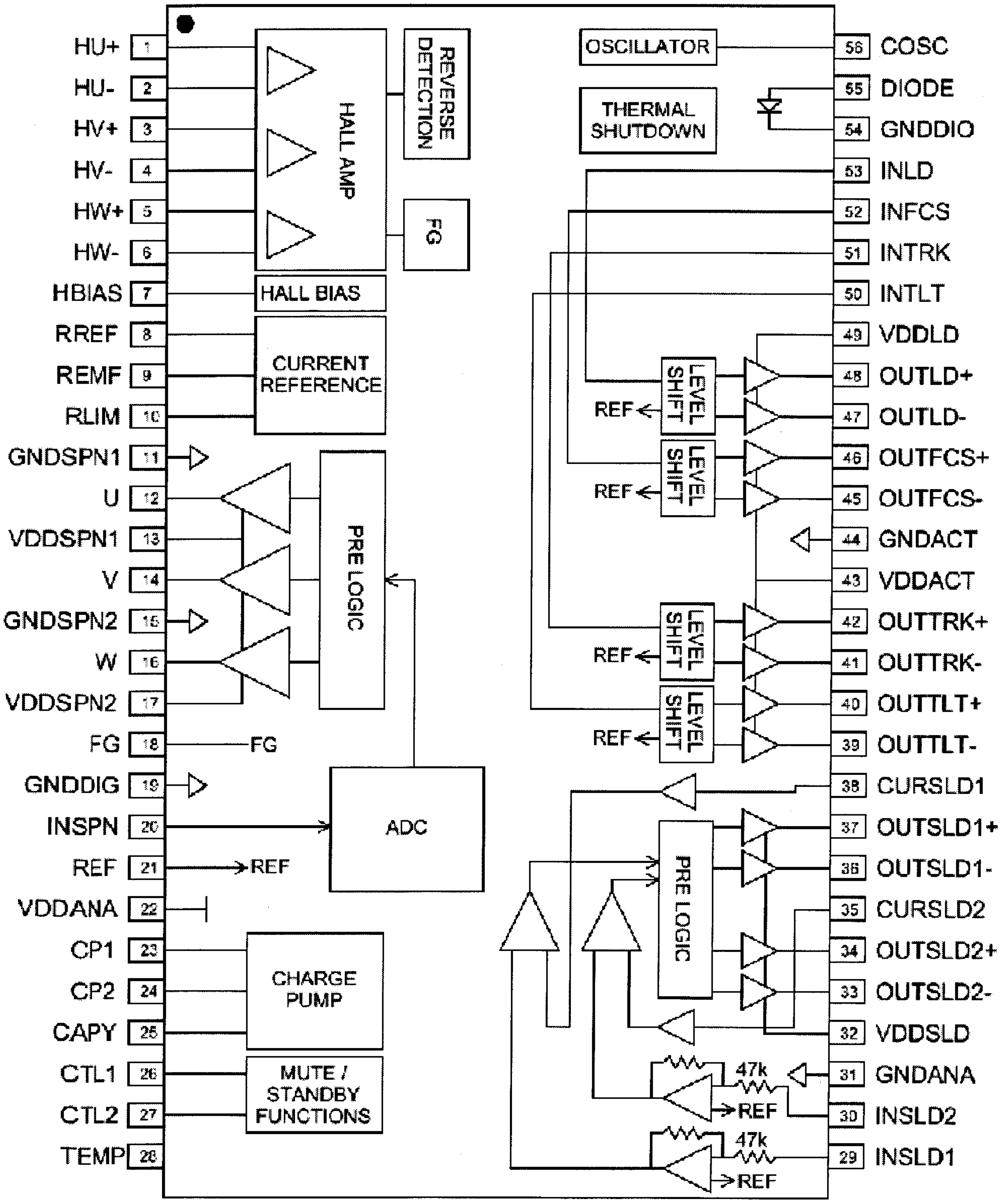

HU+ 1
HU- 2
HV+ 3
HV- 4
HW+ 5
HW- 6
HBIAS 7
RREF 8
REMF 9
RLIM 10
GNDSPN1 11
U 12
VDDSPN1 13
V 14
GNDSPN2 15
W 16
VDDSPN2 17
FG 18
GNDDIG 19
INSPN 20
REF 21
VDDANA 22
CP1 23
CP2 24
CAPY 25
CTL1 26
CTL2 27
TEMP 28
56 COSC
55 DIODE
54 GNDDIO
53 INLD
52 INFCS
51 INTRK
50 INTLT
49 VDDLD
48 OUTLD+
47 OUTLD-
46 OUTFCS+
45 OUTFCS-
44 GNDACT
43 VDDACT
42 OUTTRK+
41 OUTTRK-
40 OUTTLT+
39 OUTTLT-
38 CURSLD1
37 OUTSLD1+
36 OUTSLD1-
35 CURSLD2
34 OUTSLD2+
33 OUTSLD2-
32 VDDSLD
31 GNDANA
30 INSLD2
29 INSLD1
HALL AMP
REVERSE DETECTION
FG
HALL BIAS
CURRENT REFERENCE
PRE LOGIC
ADC
CHARGE PUMP
MUTE / STANDBY FUNCTIONS
OSCILLATOR
THERMAL SHUTDOWN
LEVEL SHIFT
LEVEL SHIFT
LEVEL SHIFT
LEVEL SHIFT
REF
REF
REF
REF
FG
REF
PRE LOGIC
47k
REF
47k
REF

Fig.2 Block diagram SA56202.

Figure 9-38

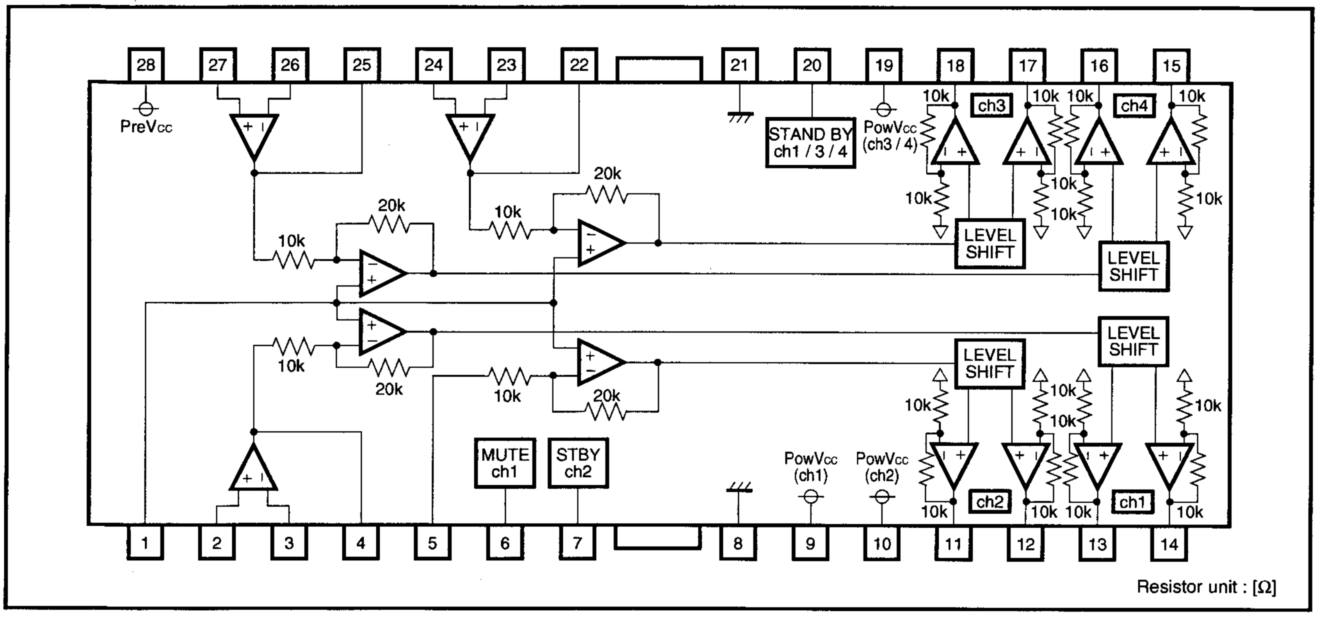
PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION	PIN	SYMBOL	DESCRIPTION
1	HU+	positive Hall input U	56	COSC	ext. capacitor for int. oscillator
2	HU-	negative Hall input U	55	DIODE	diode for temperature readout
3	HV+	positive Hall input V	54	GNDDIO	temperature diode ground
4	HV-	negative Hall input V	53	INLD	loading driver input
5	HW+	positive Hall input W	52	INFCS	focus driver input
6	HW-	negative Hall input W	51	INTRK	tracking driver input
7	HBIAS	Hall element bias	50	INTLT	tilting driver input
8	RREF	ext. res. for current reference	49	VDDLD	loading driver power supply
9	REMF	ext. res. for EMF regeneration	48	OUTLD+	loading driver positive output
10	RLIM	ext. res. for current limit	47	OUTLD-	loading driver negative output
11	GNDSPN1	spindle driver power ground 1	46	OUTFCS+	focus driver positive output
12	U	spindle driver output U	45	OUTFCS-	focus driver negative output
13	VDDSPN1	spindle driver power supply 1	44	GNDACT	actuator drivers power ground
14	V	spindle driver output V	43	VDDACT	actuator drivers power supply
15	GNDSPN2	spindle driver power ground 2	42	OUTTRK+	tracking driver pos. output
16	W	spindle driver output W	41	OUTTRK-	tracking driver neg. output
17	VDDSPN2	spindle driver power supply 2	40	OUTTLT+	tilting driver pos. output
18	FG	frequency generator output	39	OUTTLT-	tilting driver neg. output
19	GNDDIG	ground supply	38	CURSLD1	sled driver 1 current sense
20	INSPN	spindle driver input	37	OUTSLD1+	sled driver 1 positive output
21	REF	reference input voltage	36	OUTSLD1-	sled driver 1 negative output
22	VDDANA	system supply voltage	35	CURSLD2	sled driver 2 current sense
23	CP1	charge pump cap. conn. 1	34	OUTSLD2+	sled driver 2 positive output
24	CP2	charge pump cap. conn. 2	33	OUTSLD2-	sled driver 2 negative output
25	CAPY	charge pump output voltage	32	VDDSLD	sled driver power supply
26	CTL1	driver logic control input 1	31	GNDANA	ground supply
27	CTL2	driver logic control input 2	30	INSLD2	sled driver 2 input
28	TEMP	thermal warning	29	INSLD1	sled driver 1 input

Figure 9-39

IC7409 BA5995: FEBE Board, 4-channel BTL driver

●Block diagram


28
27
26
25
24
23
22
21
20
19
18
17
16
15
PreVcc
STAND BY ch1 / 3 / 4
PowVcc (ch3 / 4)
ch3
ch4
10k
20k
LEVEL SHIFT
MUTE ch1
STBY ch2
PowVcc (ch1)
PowVcc (ch2)
ch2
ch1
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Resistor unit : [Ω]

●Pin descriptions

Pin No.	Pin name	Function
1	BIAS IN	Input for bias-amplifier
2	OPIN1 (+)	Non inverting input for CH1 OP-AMP
3	OPIN1 (–)	Inverting input for CH1 OP-AMP
4	OPOUT1	Output for CH1 OP-AMP
5	IN2	Input for CH2
6	MUTE	Input for CH1 mute control
7	STBY2	Input for CH2 stand by control
8	GND	Substrate ground
9	PowVcc1	Vcc for CH1 power block
10	PowVcc2	Vcc for CH2 power block
11	Vo2 (–)	Inverted output of CH2
12	Vo2 (+)	Non inverted output of CH2
13	Vo1 (–)	Inverted output of CH1
14	Vo1 (+)	Non inverted output of CH1

Note) Symbol of + and – (output of drivers) means polarity to input pin.
(For example if voltage of pin4 high, pin14 is high.)

Pin No.	Pin name	Function
15	Vo4 (+)	Non inverted output of CH4
16	Vo4 (–)	Inverted output of CH4
17	Vo3 (+)	Non inverted output of CH3
18	Vo3 (–)	Inverted output of CH3
19	PowVcc3	Vcc for CH3/4 power block
20	STBY1	Input for CH1/3/4 stand by control
21	GND	Substrate ground
22	OPOUT3	Output for CH3 OP-AMP
23	OPIN3 (–)	Inverting input for CH3 OP-AMP
24	OPIN3 (+)	Non inverting input for CH3 OP-AMP
25	OPOUT4	Output for CH4 OP-AMP
26	OPIN4 (–)	Inverting input for CH4 OP-AMP
27	OPIN4 (+)	Non inverting input for CH4 OP-AMP
28	PreVcc	Vcc for pre block

Figure 9-40

IC7500, PNX7850: FEBE Board, Channel Codec/Buffer Manager/Servo Processor and Controller

Nexperia PNX7850 conceptual block diagram

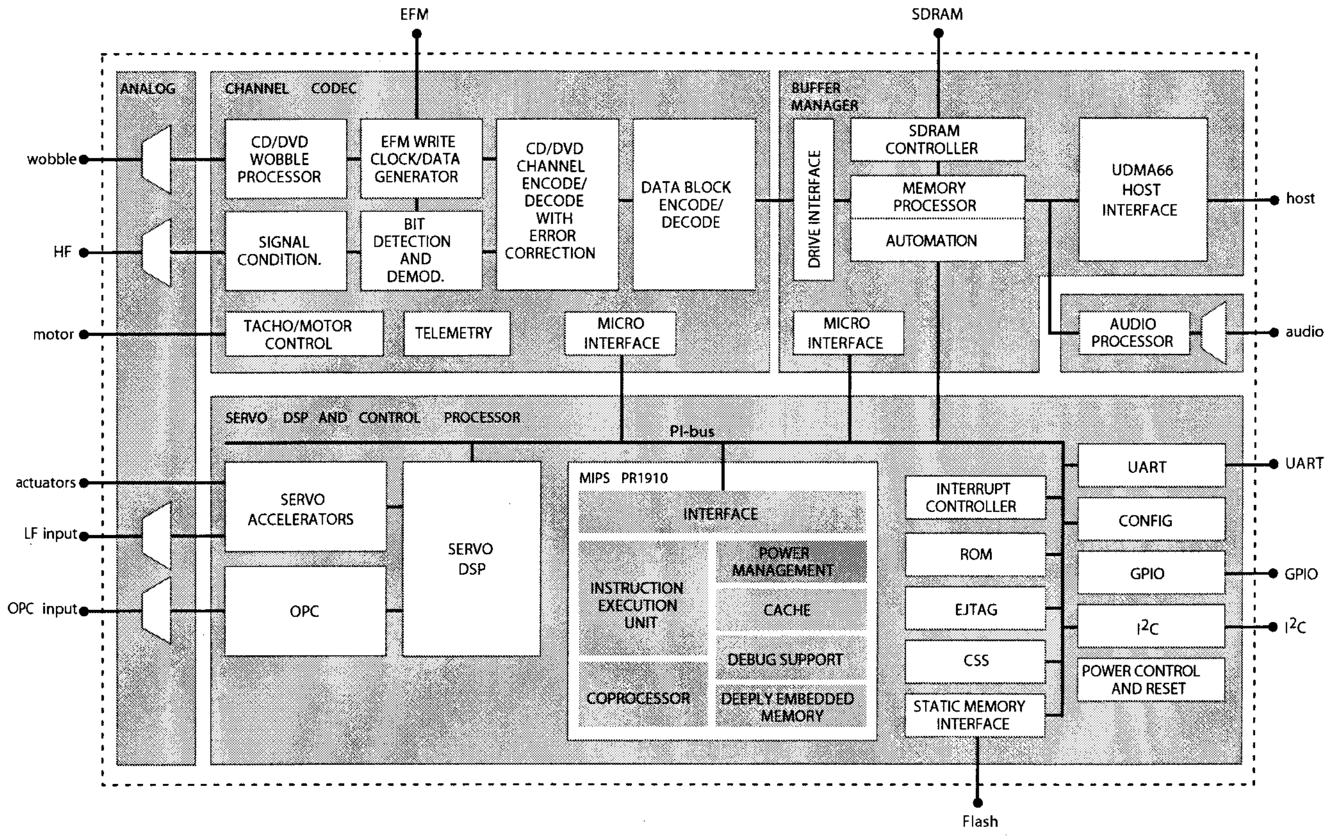

EFM
SDRAM
ANALOG
CHANNEL CODEC
BUFFER MANAGER
wobble
HF
motor
CD/DVD WOBBLE PROCESSOR
EFM WRITE CLOCK/DATA GENERATOR
CD/DVD CHANNEL ENCODE/ DECODE WITH ERROR CORRECTION
DATA BLOCK ENCODE/ DECODE
DRIVE INTERFACE
SDRAM CONTROLLER
MEMORY PROCESSOR
AUTOMATION
UDMA66 HOST INTERFACE
host
SIGNAL CONDITION.
BIT DETECTION AND DEMOD.
TACHO/MOTOR CONTROL
TELEMETRY
MICRO INTERFACE
MICRO INTERFACE
AUDIO PROCESSOR
audio
SERVO DSP AND CONTROL PROCESSOR
PI-bus
actuators
LF input
OPC input
SERVO ACCELERATORS
OPC
SERVO DSP
MIPS PR1910
INTERFACE
INSTRUCTION EXECUTION UNIT
POWER MANAGEMENT
CACHE
DEBUG SUPPORT
COPROCESSOR
DEEPLY EMBEDDED MEMORY
INTERRUPT CONTROLLER
ROM
EJTAG
CSS
STATIC MEMORY INTERFACE
UART
CONFIG
GPIO
I2C
POWER CONTROL AND RESET
UART
GPIO
I2C
Flash

Figure 9-41

IC7926 NCP303LSN, FEBE Board , Reset Circuit

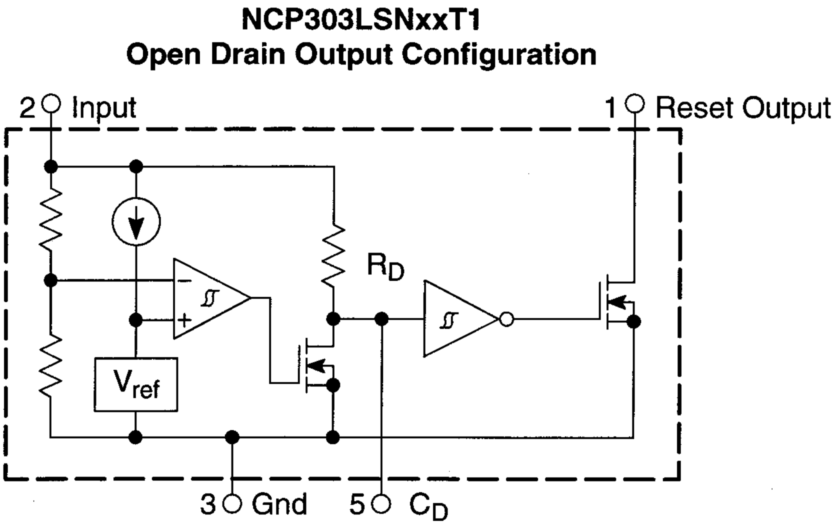
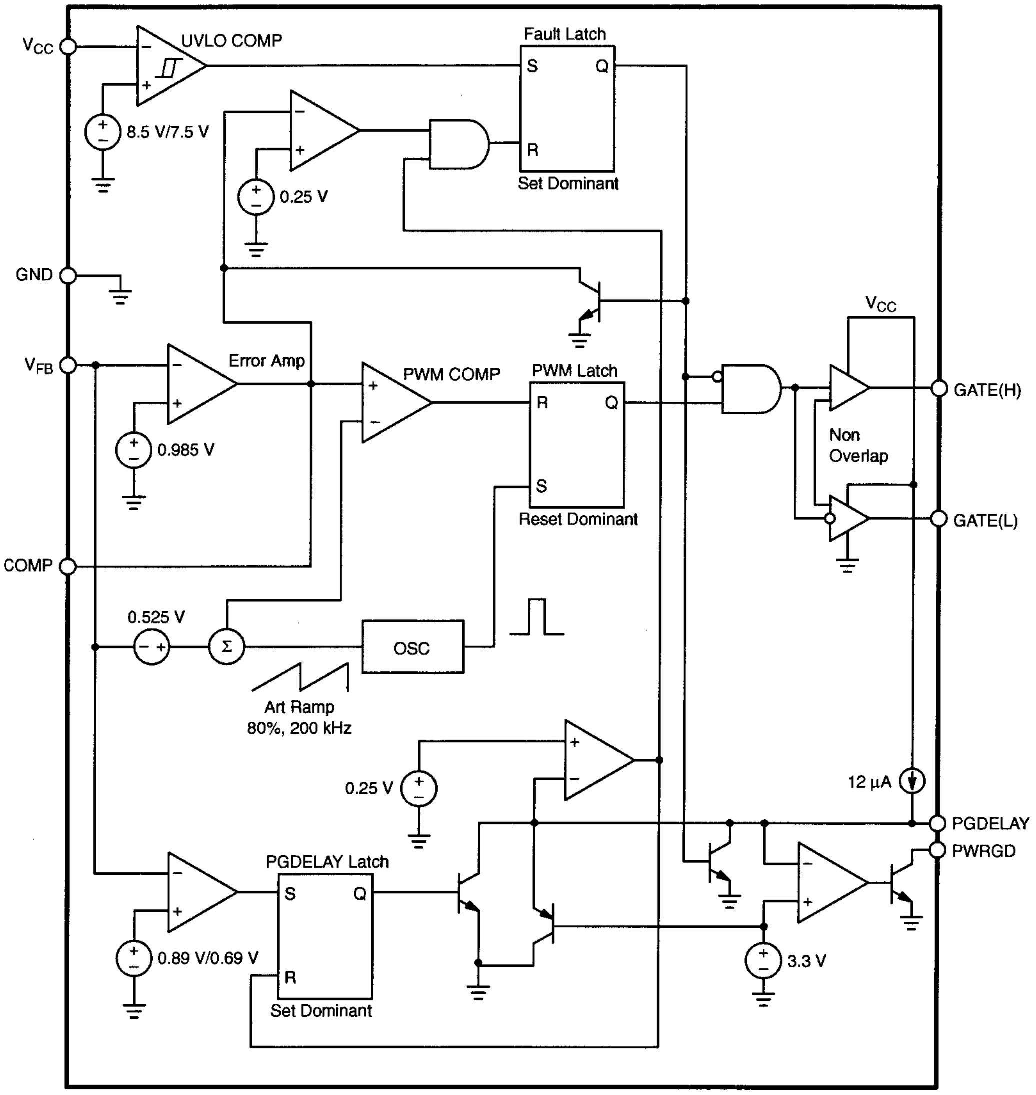

NCP303LSNxxT1
Open Drain Output Configuration
2 Input
1 Reset Output
RD
Vref
3 Gnd
5 CD

Figure 9-42

IC7929 NCP1570D, FEBE Board, DC/DC Converter Control



VCC
UVLO COMP
Fault Latch
S
Q
R
Set Dominant
8.5 V/7.5 V
0.25 V
GND
VCC
VFB
Error Amp
PWM COMP
PWM Latch
R
Q
S
Reset Dominant
0.985 V
GATE(H)
Non Overlap
GATE(L)
COMP
0.525 V
Σ
OSC
Art Ramp
80%, 200 kHz
0.25 V
12 µA
PGDELAY
PWRGD
PGDELAY Latch
S
Q
R
Set Dominant
0.89 V/0.69 V
3.3 V

Figure 9-43

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SO–8	PIN SYMBOL	FUNCTION
1	V_{CC}	Power supply input.
2	PWRGD	Open collector output goes low when V_{FB} is out of regulation. User must externally limit current into this pin to less than 20 mA.
3	PGDELAY	External capacitor programs PWRGD low–to–high transition delay.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft Start. Pulling pin < 0.45 locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High–side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low–side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V_{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

Figure 9-44

IC 7009 SAA7117AE/V2, LECO Board,Multistandard video decoder with adaptive comb filter and component video input

4 PINNING

SYMBOL	PIN		TYPE[1]	DESCRIPTION
	QFP160	BGA156		
DNC6	1	B2	I	do not connect, reserved for future extensions and for testing
AI41	2	B1	I	analog input 41 (either video or D1/SCART sensor) (7117A only)
AGND	3	C2	P	analog signal ground
V_{SSA4}	4	C1	P	ground for analog inputs AI4x
AI42	5	D2	I	analog input 42 (either video, D1/SCART sensor) (7117A only)
AI4D	6	D3	I	differential input for ADC channel 4 (pins AI41 to AI44)
AI43	7	D1	I	analog input 43 (either video or D1/SCART sensor) (7117A only)
V_{DDA4}	8	D4	P	analog supply voltage for analog inputs AI4x (3.3 V)
V_{DDA4A}	9	E2	P	analog supply voltage for analog inputs AI4x (3.3 V)
AI44	10	E1	I	analog input 44 (either video, D1/SCART sensor)
AI31	11	E3	I	analog input 31 (either video or D1/SCART sensor) (7117A only)
V_{SSA3}	12	E4	P	ground for analog inputs AI3x
AI32	13	F2	I	analog input 32 (either video, D1/SCART sensor) (7117A only)
AI3D	14	F1	I	differential input for ADC channel 3 (pins AI31 to AI34)
AI33	15	F3	I	analog input 33 (either video or D1/SCART sensor) (7117A only)
V_{DDA3}	16	F4	P	analog supply voltage for analog inputs AI3x (3.3 V)
V_{DDA3A}	17	G2	P	analog supply voltage for analog inputs AI3x (3.3 V)
AI34	18	G1	I	analog input 34 (either video or D1/SCART sensor) (7117A only)
AI21	19	G4	I	analog input 21(7117A only)
V_{SSA2}	20	H3	P	ground for analog inputs AI2x
AI22	21	G3	I	analog input 22;
AI2D	22	H1	I	differential input for ADC channel 2 (pins AI24 to AI21)
AI23	23	H2	I	analog input 23 (7117A only)
V_{DDA2}	24	H4	P	analog supply voltage for analog inputs AI2x (3.3 V)
V_{DDA2A}	25	J1	P	analog supply voltage for analog inputs AI2x (3.3 V)
AI24	26	J3	I	analog input 24
AI11	27	J2	I	analog input 11
V_{SSA1}	28	J4	P	ground for analog inputs AI1x

SYMBOL	PIN		TYPE(1)	DESCRIPTION
	QFP160	BGA156		
AI12	29	K1	I	analog input 12
AI1D	30	K3	I	differential input for ADC channel 1 (pins AI14 to AI11)
AI13	31	K2	I	analog input 13
V_{DDA1}	32	K4	P	analog supply voltage for analog inputs AI1x (3.3 V)
V_{DDA1A}	33	L1	P	analog supply voltage for analog inputs AI1x (3.3 V)
AI14	34	L3	I	analog input 14
AGNDA	35	L2	P	analog signal ground
DNC	36	M1	NC	do not connect, reserved for future extensions and for testing
V_{DDA0}	37	M3	P	analog supply voltage (3.3 V)
V_{SSA0}	38	M2	P	analog ground
AOUT	39	N1	O	analog output (7117A only)
VDDA_C18	40	N2	P	analog supply voltage (1.8 V)
VDDA_A18	41	P2	P	analog supply voltage (1.8 V)
DNC15	42	N3	I	do not connect, reserved for future extensions and for testing
GPIN	43	P3	I/pu	general purpose input (with internal pull-up)
CE	44	N4	I/pu	chip enable or reset input (with internal pull-up)
V_{DDD1}	45	M4	P	digital supply voltage 1 (peripheral cells, 3.3 V)
LLC	46	P4	O	line-locked system clock output (27 MHz nominal)
V_{SSD1}	47	L4	P	digital ground 1 (peripheral cells)
LLC2_54	48	N5	O	line-locked $^1/_2$ clock output (13.5 MHz nominal), or adc_clock 54 MHz, selectable via I^2C
$\overline{RES}$	49	P5	O	reset output (active LOW)
V_{DDD2}	50	M5	P	digital supply voltage 2 (core, 1.8 V)
V_{SSD2}	51	L5	P	digital ground 2
DNC23	52	N6	I	do not connect, reserved for future extensions and for testing
DNC24	53	P6	O	do not connect, reserved for future extensions and for testing
DNC25	54	M6	O	do not connect, reserved for future extensions and for testing
DNC26	55	L6	O	do not connect, reserved for future extensions and for testing
DNC27	56	N7	O	do not connect, reserved for future extensions and for testing
DNC28	57	P7	O	do not connect, reserved for future extensions and for testing
DNC29	58	L7	O	do not connect, reserved for future extensions and for testing
V_{DDD3}	59	M8	P	digital supply voltage 3 (peripheral cells, 3.3 V)
DNC30	60	M7	O	do not connect, reserved for future extensions and for testing
DNC31	61	P8	O	do not connect, reserved for future extensions and for testing
DNC32	62	N8	O	do not connect, reserved for future extensions and for testing
V_{SSD3}	63	L8	P	digital ground 3 (peripheral cells)
INT_A	64	P9	O/od	I^2C-bus interrupt flag (LOW if any enabled status bit has changed)
V_{DDD4}	65	M9	P	digital supply voltage 4 (core, 1.8 V)
SCL	66	N9	I	serial clock input (I^2C-bus)
V_{SSD4}	67	L9	P	digital ground 4 (core; connects to substrate)

SYMBOL	PIN		TYPE[1]	DESCRIPTION
	QFP160	BGA156		
SDA	68	P10	I/O/od	serial data input/output (I^2C-bus)
RTS0	69	M10	O	real-time status or sync information, controlled by subaddresses 11h and 12h
RTS1	70	N10	O	real-time status or sync information, controlled by subaddresses 11h and 12h
RTCO	71	L10	O/st/pd	real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see *"RTC Functional Description"*); notes 5 and 6
AMCLK	72	P11	O	audio master clock output
V_{DDD5}	73	M11	P	digital supply voltage 5 (peripheral cells, 3.3 V)
ASCLK	74	N11	O	audio serial clock output
ALRCLK	75	P12	O/st/pd	audio left/right clock output; notes 5 and 7
AMXCLK	76	M12	I	audio master external clock input
ITRDY	77	N12	I/pu	target ready input for image port data
DNC0	78	P13	NC	do not connect, reserved for future extensions and for testing
DNC16	79	N13	I/O	do not connect, reserved for future extensions and for testing
DNC17	80	N14	NC	do not connect, reserved for future extensions and for testing
DNC19	81	–	NC	do not connect, reserved for future extensions and for testing
DNC20	82	–	NC	do not connect, reserved for future extensions and for testing
FSW	83	M13	I/pd	Legacy fast switch function of SAA7118 (with internal pull-down)
ICLK	84	M14	I/O	clock output signal for image port, or optional asynchronous back-end clock input
IDQ	85	L13	O	output data qualifier for image port (optional: gated clock output)
ITRI	86	L12	I	image port output control signal, affects all input port pins inclusive ICLK, enable and active polarity is under software control
IGP0	87	L14	O	general purpose output signal 0 of image port
V_{SSD5}	88	L11	P	digital ground 5 (peripheral cells)
IGP1	89	K13	O	general purpose output signal 1 of image port
IGPV	90	K14	O	multi purpose vertical reference output signal of image port
IGPH	91	K12	O	multi purpose horizontal reference output signa of image port
IPD7	92	K11	O	MSB0 of image port data 1 output
IPD6	93	J13	O	MSB1 of image port data 1 output
IPD5	94	J14	O	MSB2 of image port data 1 output
V_{DDD6}	95	J12	P	digital supply voltage 6 (peripheral cells, 3.3 V)
V_{SSD6}	96	J11	P	digital ground 6 (core; connects to substrate)
IPD4	97	H13	O	MSB3 of image port data 1 output
IPD3	98	H14	O	MSB4 of image port data 1 output
IPD2	99	H11	O	MSB5 of image port data 1 output
IPD1	100	G12	O	MSB6 of image port data 1 output

SYMBOL	PIN		TYPE[1]	DESCRIPTION
	QFP160	BGA156		
V_{DDD7}	101	H12	P	digital supply voltage 7 (core, 1.8 V)
IPD0	102	G14	O	LSB of image port data 1 output
HPD7	103	G13	I/O	MSB0 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
V_{SSD7}	104	G11	P	digital ground 7 (peripheral cells)
HPD6	105	F14	I/O	MSB1 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
V_{DDD8}	106	F12	P	digital supply voltage 8 (core, 1.8 V)
HPD5	107	F13	I/O	MSB2 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
V_{SSD8}	108	F11	P	digital ground 8 (core)
HPD4	109	E14	I/O	MSB3 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD3	110	E12	I/O	MSB4 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD2	111	E13	I/O	MSB5 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD1	112	E11	I/O	MSB6 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD0	113	D14	I/O	LSB of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
V_{DDD9}	114	D12	P	digital supply voltage 9 (peripheral cells, 3.3 V)
DNC1	115	D13	NC	do not connect, reserved for future extensions and for testing
DNC2	116	C14	NC	do not connect, reserved for future extensions and for testing
DNC7	117	C12	NC	do not connect, reserved for future extensions and for testing
DNC8	118	C13	NC	do not connect, reserved for future extensions and for testing
DNC11	119	B14	NC	do not connect, reserved for future extensions and for testing
DNC12	120	B13	NC	do not connect, reserved for future extensions and for testing
DNC21	121	–	NC	do not connect, reserved for future extensions and for testing
DNC22	122	–	NC	do not connect, reserved for future extensions and for testing
DNC3	123	A13	NC	do not connect, reserved for future extensions and for testing
DNC4	124	B12	NC	do not connect, reserved for future extensions and for testing
DNC5	125	A12	I	do not connect, reserved for future extensions and for testing
XTRI	126	B11	I	X-port output control signal, affects all X-port pins (XPD7 to XPD0, XRH, XRV, XDQ and XCLK), enable and active polarity is under software control
XPD7	127	C11	I/O	MSB0 of expansion port data
XPD6	128	A11	I/O	MSB1 of expansion port data
V_{SSD9}	129	D11	P	digital ground 9 (peripheral cells)
XPD5	130	B10	I/O	MSB2 of expansion port data
XPD4	131	A10	I/O	MSB3 of expansion port data

SYMBOL	PIN		TYPE[1]	DESCRIPTION
	QFP160	BGA156		
V_{DDD10}	132	C10	P	digital supply voltage 10 (core, 1.8 V)
V_{SSD10}	133	D10	P	digital ground 10 (core)
XPD3	134	B9	I/O	MSB4 of expansion port data
XPD2	135	A9	I/O	MSB5 of expansion port data
V_{DDD11}	136	C9	P	digital supply voltage 11 (peripheral cells, 3.3 V)
V_{SSD11}	137	D9	P	digital ground 11 (peripheral cells)
XPD1	138	B8	I/O	MSB6 of expansion port data
XPD0	139	A8	I/O	LSB of expansion port data
XRV	140	D8	I/O	vertical reference I/O expansion port
XRH	141	C7	I/O	horizontal reference I/O expansion port
V_{DDD12}	142	C8	P	digital supply voltage 12 (core, 1.8 V)
XCLK	143	A7	I/O	clock I/O expansion port
XDQ	144	B7	I/O	data qualifier for expansion port or Source-Select (pixelwise switch between X-port input/decoder output)
V_{SSD12}	145	D7	P	digital ground 12 (core; connects to substrate)
XRDY	146	A6	O	task flag or ready signal from the region and field processing, I^2C-controlled
$\overline{TRST}$	147	C6	I/pu	test reset input (active LOW), for boundary scan test (with internal pull-up); notes 2, 3 and 4
TCK	148	B6	I/pu	test clock for boundary scan test; note 2
TMS	149	D6	I/pu	test mode select input for boundary scan test or scan test; note 2
TDO	150	A5	O	test data output for boundary scan test; note 2
V_{DDD13}	151	C5	P	digital supply voltage 13 (peripheral cells, 3.3 V)
TDI	152	B5	I/pu	test data input for boundary scan test; note 2
V_{SSD13}	153	D5	P	digital ground 13 (peripheral cells)
$V_{SS(xtal)}$	154	A4	P	ground for crystal oscillator
XTALI	155	B4	I	input terminal for 24.576 MHz (32.11 MHz) crystal oscillator or connection of external oscillator
XTALO	156	A3	O	24.576 MHz (32.11 MHz) crystal oscillator output; do not connect if clock input of XTALI is used
$V_{DD(xtal)}$	157	B3	P	supply voltage for crystal oscillator (1.8 V)
XTOUT	158	A2	O	crystal oscillator output signal; auxiliary signal
DNC9	159	C3	NC	do not connect, reserved for future extensions and for testing
DNC10	160	C4	NC	do not connect, reserved for future extensions and for testing

Notes

1. I = input, O = output, P = power, NC = not connected, st = strapping, pu = pull-up, pd = pull-down, od = open-drain.
2. In accordance with the *"IEEE1149.1"* standard the pads TDI, TMS, TCK and $\overline{TRST}$ are input pads with an internal pull-up transistor and TDO is a 3-state output pad.
3. For board design without boundary scan implementation connect the $\overline{TRST}$ pin to ground.

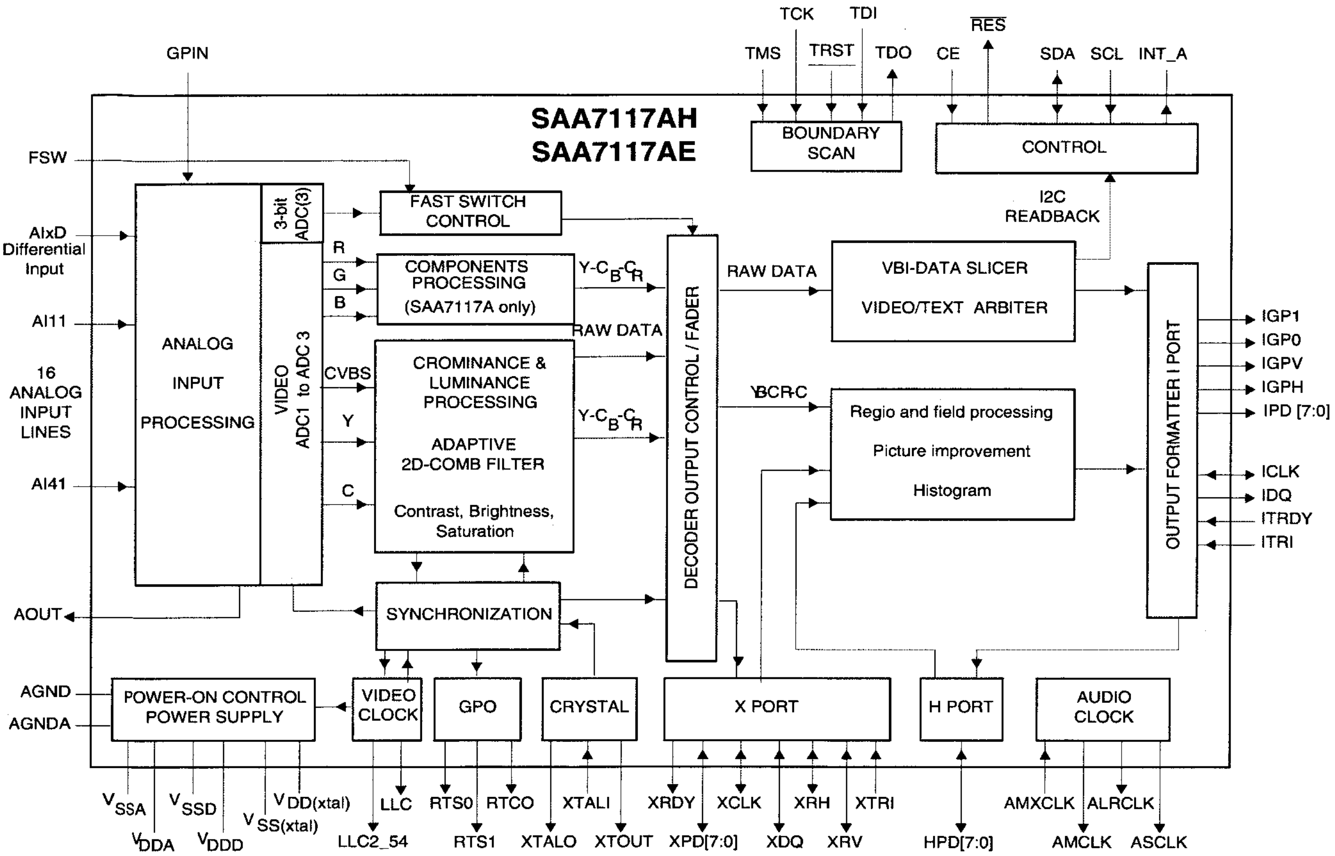

SAA7117AH
SAA7117AE
GPIN
TCK
TDI
TMS
TRST
TDO
CE
RES
SDA
SCL
INT_A
BOUNDARY SCAN
CONTROL
I2C READBACK
FSW
AIxD Differential Input
AI11
16 ANALOG INPUT LINES
AI41
AOUT
ANALOG INPUT PROCESSING
3-bit ADC(3)
VIDEO ADC1 to ADC 3
FAST SWITCH CONTROL
R
G
B
CVBS
Y
C
COMPONENTS PROCESSING (SAA7117A only)
Y-C_B-C_R
RAW DATA
CROMINANCE & LUMINANCE PROCESSING
ADAPTIVE 2D-COMB FILTER
Contrast, Brightness, Saturation
Y-C_B-C_R
DECODER OUTPUT CONTROL / FADER
RAW DATA
VBI-DATA SLICER
VIDEO/TEXT ARBITER
YBCRC
Regio and field processing
Picture improvement
Histogram
OUTPUT FORMATTER I PORT
IGP1
IGP0
IGPV
IGPH
IPD [7:0]
ICLK
IDQ
ITRDY
ITRI
SYNCHRONIZATION
AGND
AGNDA
POWER-ON CONTROL POWER SUPPLY
VIDEO CLOCK
GPO
CRYSTAL
X PORT
H PORT
AUDIO CLOCK
V_SSA
V_SSD
V_DD(xtal)
V_SS(xtal)
V_DDA
V_DDD
LLC
LLC2_54
RTS0
RTCO
RTS1
XTALI
XTALO
XTOUT
XRDY
XCLK
XPD[7:0]
XRH
XDQ
XTRI
XRV
HPD[7:0]
AMXCLK
ALRCLK
AMCLK
ASCLK

Fig.5 SAA7117(A)H/E block diagram.

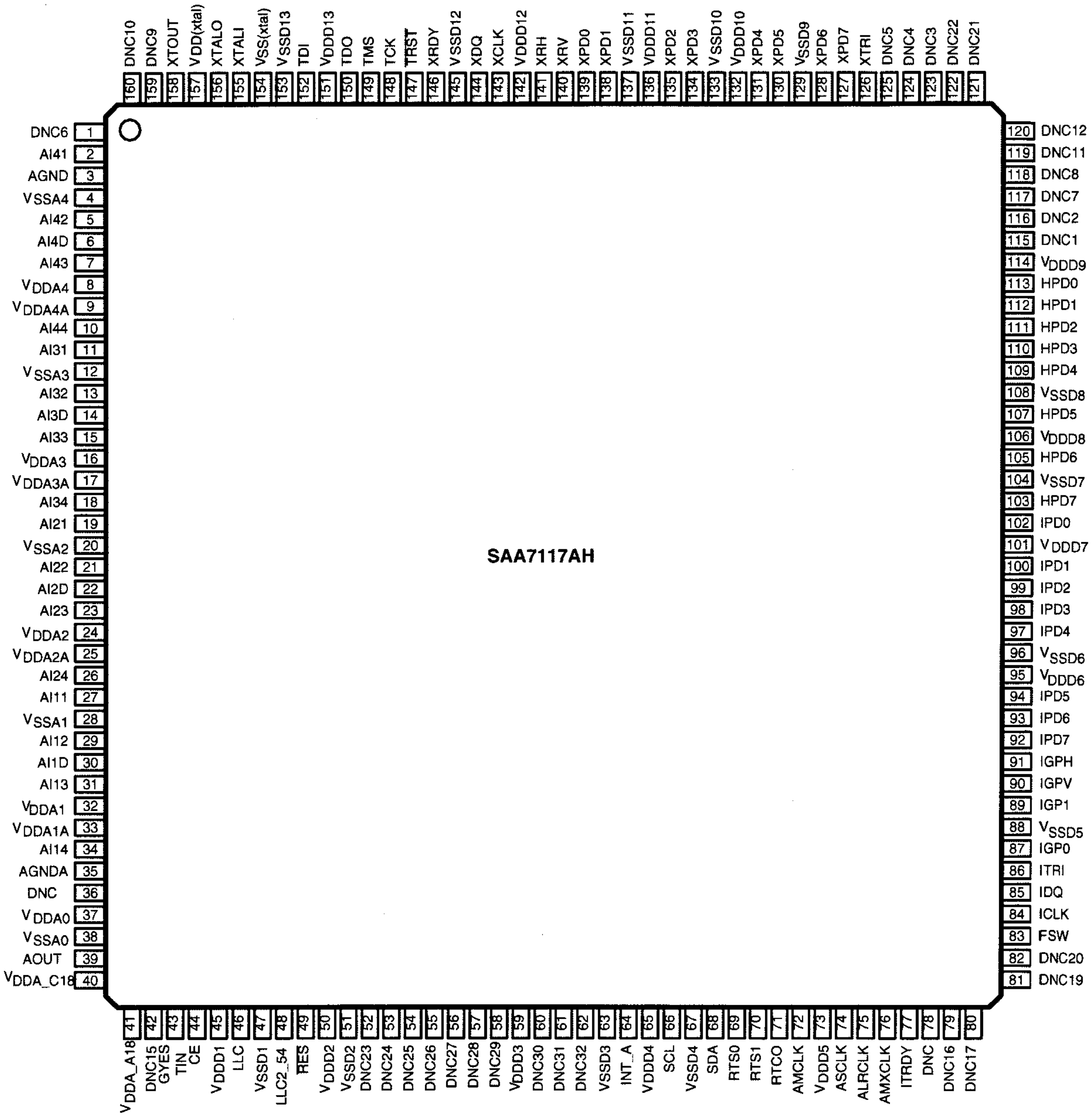

SAA7117AH
1 DNC6
2 AI41
3 AGND
4 VSSA4
5 AI42
6 AI4D
7 AI43
8 VDDA4
9 VDDA4A
10 AI44
11 AI31
12 VSSA3
13 AI32
14 AI3D
15 AI33
16 VDDA3
17 VDDA3A
18 AI34
19 AI21
20 VSSA2
21 AI22
22 AI2D
23 AI23
24 VDDA2
25 VDDA2A
26 AI24
27 AI11
28 VSSA1
29 AI12
30 AI1D
31 AI13
32 VDDA1
33 VDDA1A
34 AI14
35 AGNDA
36 DNC
37 VDDA0
38 VSSA0
39 AOUT
40 VDDA_C18
41 VDDA_A18
42 DNC15
GYES
43 TIN
44 CE
45 VDDD1
46 LLC
47 VSSD1
48 LLC2_54
49 RES
50 VDDD2
51 VSSD2
52 DNC23
53 DNC24
54 DNC25
55 DNC26
56 DNC27
57 DNC28
58 DNC29
59 VDDD3
60 DNC30
61 DNC31
62 DNC32
63 VSSD3
64 INT_A
65 VDDD4
66 SCL
67 VSSD4
68 SDA
69 RTS0
70 RTS1
71 RTCO
72 AMCLK
73 VDDD5
74 ASCLK
75 ALRCLK
76 AMXCLK
77 ITRDY
78 DNC
79 DNC16
80 DNC17
81 DNC19
82 DNC20
83 FSW
84 ICLK
85 IDQ
86 ITRI
87 IGP0
88 VSSD5
89 IGP1
90 IGPV
91 IGPH
92 IPD7
93 IPD6
94 IPD5
95 VDDD6
96 VSSD6
97 IPD4
98 IPD3
99 IPD2
100 IPD1
101 VDDD7
102 IPD0
103 HPD7
104 VSSD7
105 HPD6
106 VDDD8
107 HPD5
108 VSSD8
109 HPD4
110 HPD3
111 HPD2
112 HPD1
113 HPD0
114 VDDD9
115 DNC1
116 DNC2
117 DNC7
118 DNC8
119 DNC11
120 DNC12
121 DNC21
122 DNC22
123 DNC3
124 DNC4
125 DNC5
126 XTRI
127 XPD7
128 XPD6
129 VSSD9
130 XPD5
131 XPD4
132 VDDD10
133 VSSD10
134 XPD3
135 XPD2
136 VDDD11
137 VSSD11
138 XPD1
139 XPD0
140 XRV
141 XRH
142 VDDD12
143 XCLK
144 XDQ
145 VSSD12
146 XRDY
147 TRST
148 TCK
149 TMS
150 TDO
151 VDDD13
152 TDI
153 VSSD13
154 VSS(xtal)
155 XTALI
156 XTALO
157 VDD(xtal)
158 XTOUT
159 DNC9
160 DNC10

Fig.3 Pin configuration SAA7117AH (QFP160).

IIC 7301 NCP1571D, LECO Board, Low Volatge Buck Controller

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	V_{CC}	Power supply input.
2	PWRGD	Open collector output goes low when V_{FB} is out of regulation. User must externally limit current into this pin to less than 20 mA.
3	PGDELAY	External capacitor programs PWRGD low–to–high transition delay.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft Start. Pulling pin < 0.475 V locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High–side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low–side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V_{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

NCP1571

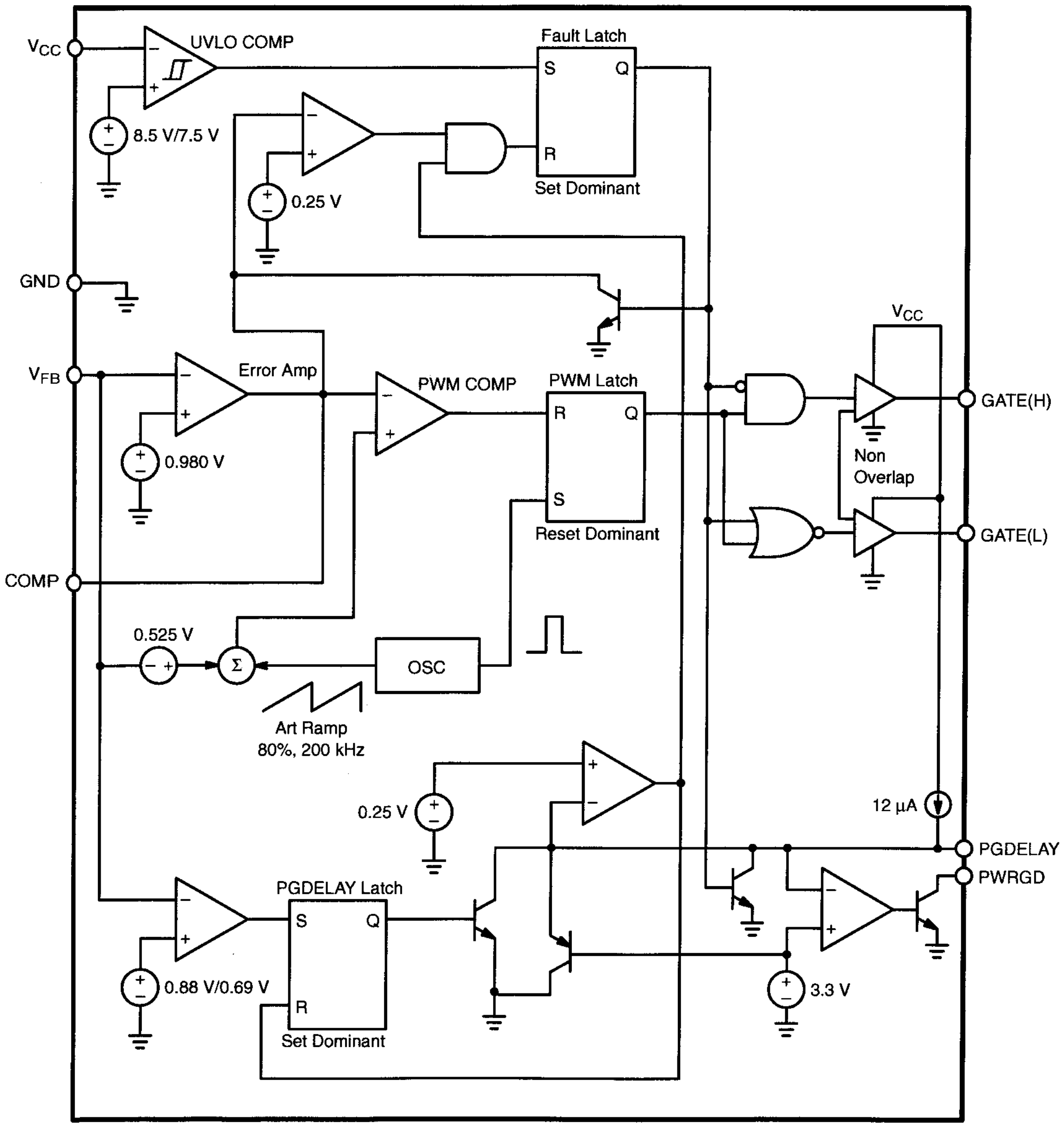
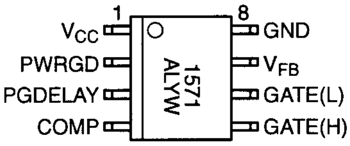

VCC
UVLO COMP
8.5 V/7.5 V
0.25 V
Fault Latch
S
Q
R
Set Dominant
GND
VFB
Error Amp
0.980 V
PWM COMP
PWM Latch
R
Q
S
Reset Dominant
VCC
Non Overlap
GATE(H)
GATE(L)
COMP
0.525 V
Σ
OSC
Art Ramp
80%, 200 kHz
0.25 V
12 µA
PGDELAY
PWRGD
PGDELAY Latch
S
Q
R
Set Dominant
0.88 V/0.69 V
3.3 V

Figure 2. Block Diagram

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

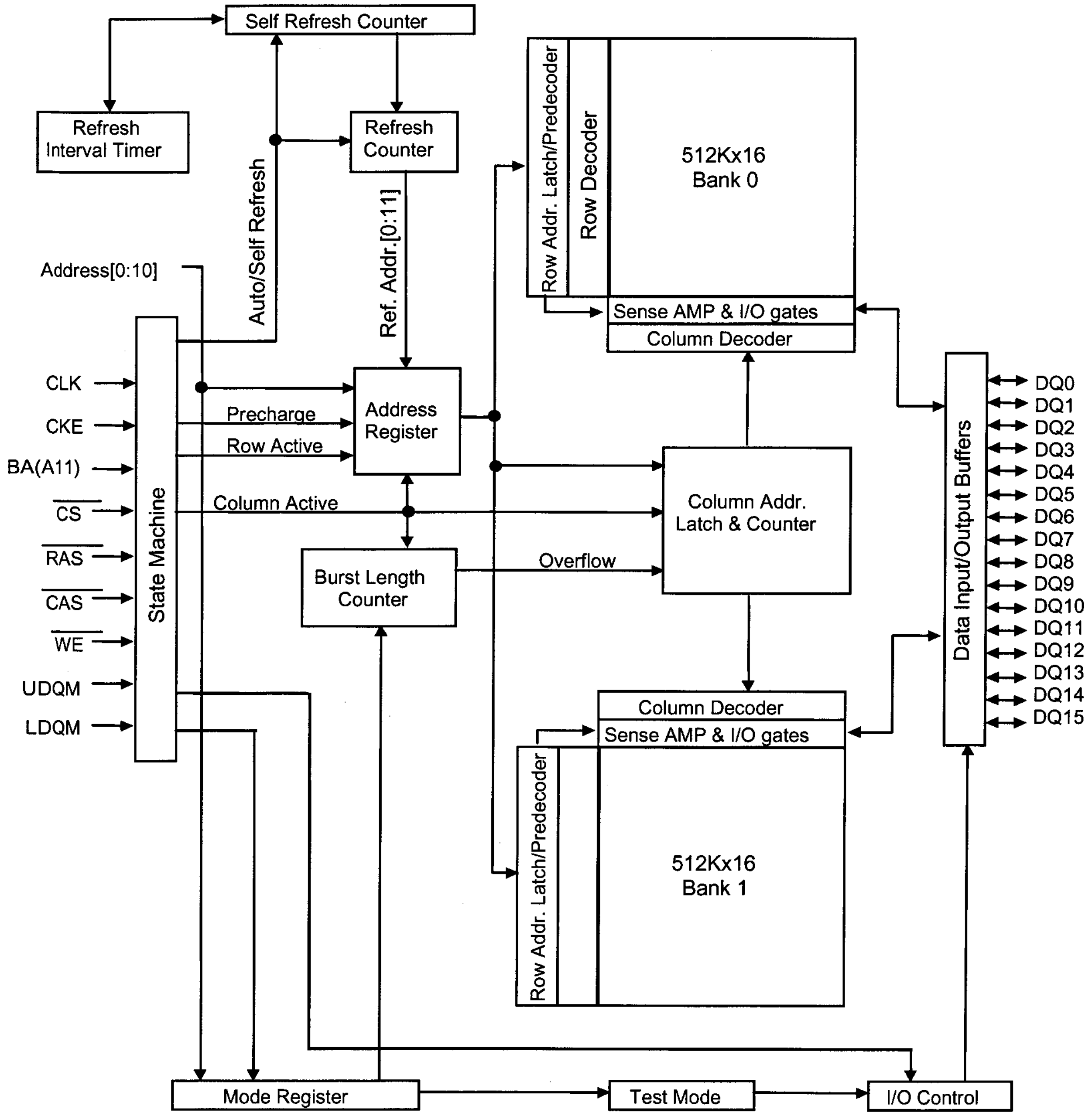
IC 7505 HY57V161610ET-7, LECO Board, 2 Banks x 512K x 16 Bit Synchronous DRAM

PIN DESCRIPTION

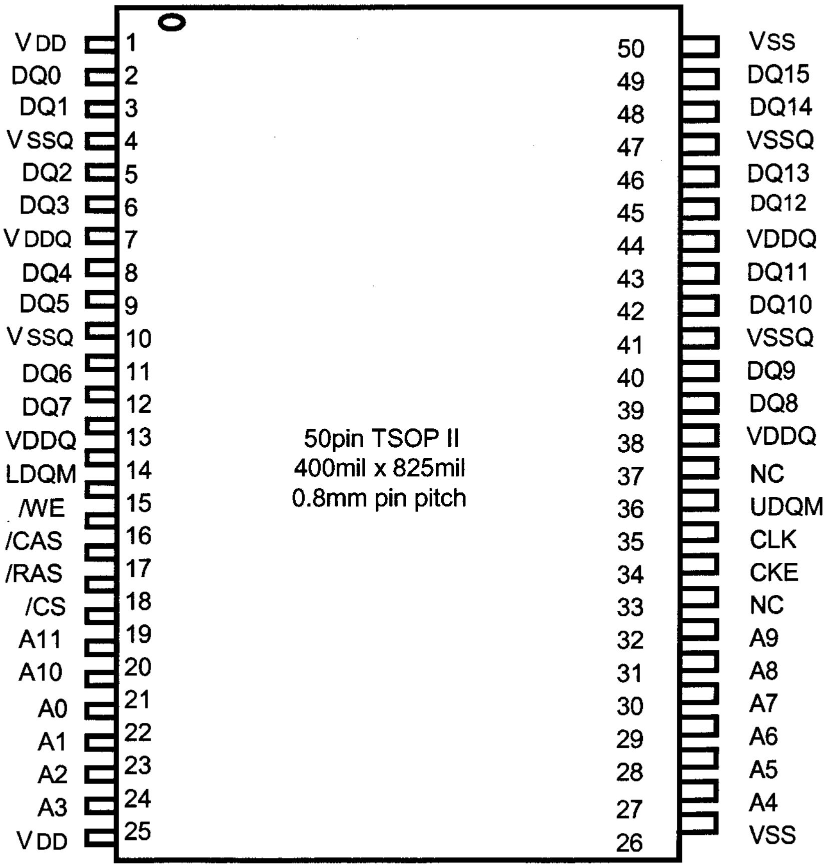
PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
$\overline{CS}$	Chip Select	Command input enable or mask except CLK, CKE and DQM
BA	Bank Address	Select either one of banks during both $\overline{RAS}$ and $\overline{CAS}$ activity.
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation. Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuit and input buffer
VDDQ/VSSQ	Data Output Power/Ground	Power supply for DQ
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mx16 Synchronous DRAM


Self Refresh Counter
Refresh Interval Timer
Refresh Counter
Auto/Self Refresh
Ref. Addr.[0:11]
Address[0:10]
CLK
CKE
BA(A11)
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
UDQM
LDQM
State Machine
Precharge
Row Active
Column Active
Address Register
Burst Length Counter
Overflow
Column Addr. Latch & Counter
Row Addr. Latch/Predecoder
Row Decoder
512Kx16 Bank 0
Sense AMP & I/O gates
Column Decoder
Column Decoder
Sense AMP & I/O gates
Row Addr. Latch/Predecoder
512Kx16 Bank 1
Data Input/Output Buffers
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
Mode Register
Test Mode
I/O Control

PIN CONFIGURATION


VDD 1
DQ0 2
DQ1 3
VSSQ 4
DQ2 5
DQ3 6
VDDQ 7
DQ4 8
DQ5 9
VSSQ 10
DQ6 11
DQ7 12
VDDQ 13
LDQM 14
/WE 15
/CAS 16
/RAS 17
/CS 18
A11 19
A10 20
A0 21
A1 22
A2 23
A3 24
VDD 25
50 VSS
49 DQ15
48 DQ14
47 VSSQ
46 DQ13
45 DQ12
44 VDDQ
43 DQ11
42 DQ10
41 VSSQ
40 DQ9
39 DQ8
38 VDDQ
37 NC
36 UDQM
35 CLK
34 CKE
33 NC
32 A9
31 A8
30 A7
29 A6
28 A5
27 A4
26 VSS
50pin TSOP II
400mil x 825mil
0.8mm pin pitch

IC 7501 PNX7860E, LECO Board, High speed processor for DVD+R/RW & CD-R/RW

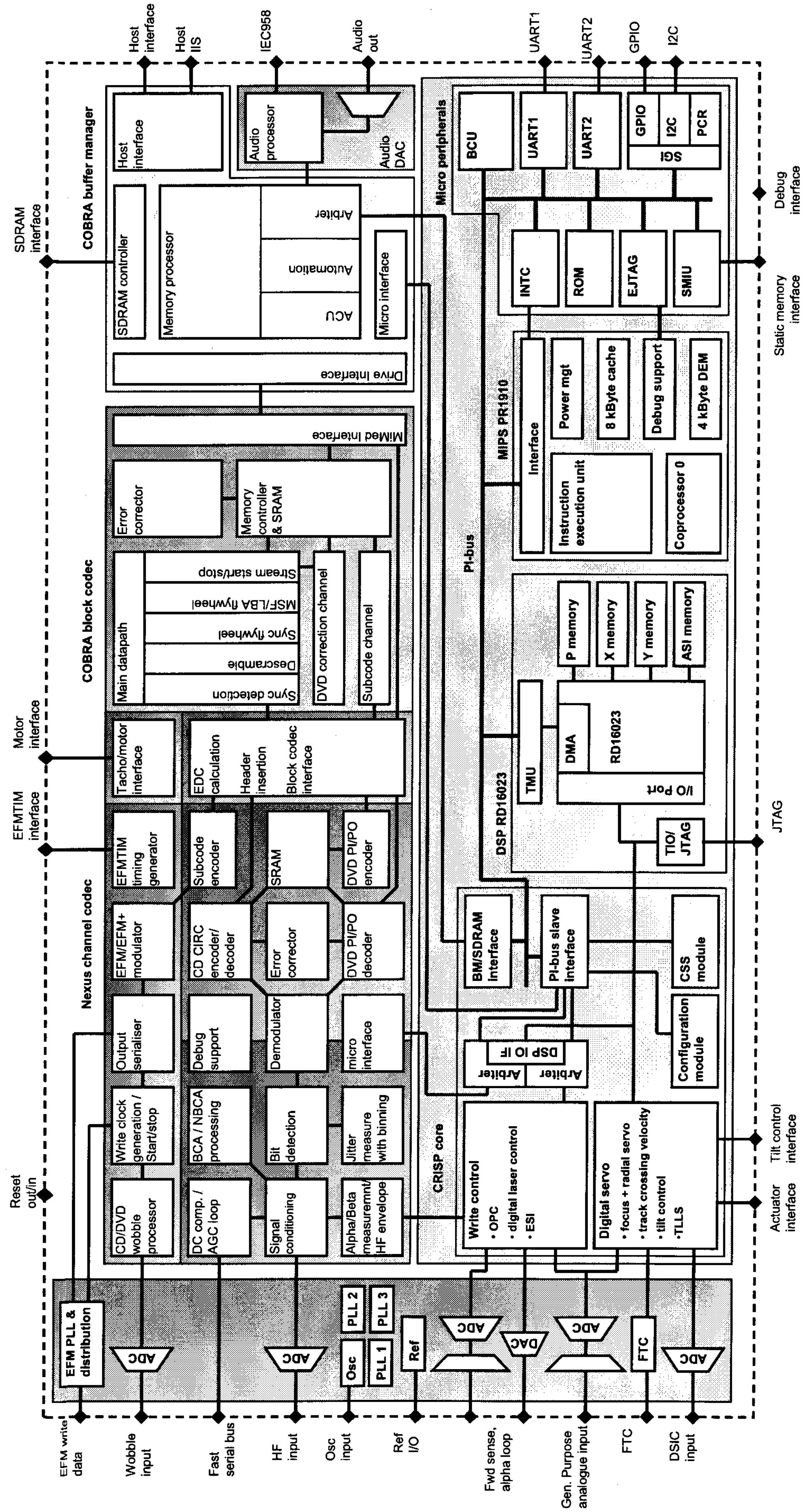

Host interface
Host IIS
IEC958
Audio out
UART1
UART2
GPIO
I2C
SDRAM interface
Motor interface
EFMTIM interface
Reset out/in
Debug interface
Static memory interface
JTAG
Tilt control interface
Actuator interface
EFM write data
Wobble input
Fast serial bus
HF input
Osc input
Ref I/O
Fwd sense, alpha loop
Gen. Purpose analogue input
FTC
DSIC input
COBRA buffer manager
Host interface
Audio processor
Audio DAC
SDRAM controller
Memory processor
Arbiter
Automation
ACU
Micro interface
Drive interface
COBRA block codec
MiMed interface
Error corrector
Memory controller & SRAM
Main datapath
Stream start/stop
MSF/LBA flywheel
Sync flywheel
Descramble
Sync detection
DVD correction channel
Subcode channel
Tacho/motor interface
EDC calculation
Header insertion
Block codec interface
Nexus channel codec
EFMTIM timing generator
Subcode encoder
SRAM
DVD PI/PO encoder
EFM/EFM+ modulator
CD CIRC encoder/decoder
Error corrector
DVD PI/PO decoder
Output serialiser
Debug support
Demodulator
micro interface
Write clock generation / Start/stop
BCA / NBCA processing
Bit detection
Jitter measure with binning
CD/DVD wobble processor
DC comp. / AGC loop
Signal conditioning
Alpha/Beta measuremnt/ HF envelope
Micro peripherals
BCU
UART1
UART2
GPIO
I2C
PCR
SGI
INTC
ROM
EJTAG
SMIU
MIPS PR1910
Interface
Power mgt
8 kByte cache
Debug support
4 kByte DEM
Instruction execution unit
Coprocessor 0
PI-bus
DSP RD16023
P memory
X memory
Y memory
ASI memory
TMU
DMA
RD16023
I/O Port
TIO/ JTAG
BM/SDRAM interface
PI-bus slave interface
CSS module
Configuration module
DSP IO IF
Arbiter
Arbiter
CRISP core
Write control
• OPC
• digital laser control
• ESI
Digital servo
• focus + radial servo
• track crossing velocity
• tilt control
•TLLS
EFM PLL & distribution
ADC
ADC
PLL 2
PLL 3
Osc
PLL 1
Ref
ADC
DAC
ADC
FTC
ADC

Table 3: Pinning list

Symbol	Pin	Type	Main function	Alternative function
RFP	U1	AI	differential RF input positive	
RFN	U2	AI	differential RF input negative	
RFREF	T1	AO	common mode reference of RF input	
WIN	T2	AI	wobble input signal	
WREF	P3	AIO	wobble ADC decoupling point	
EFMCLKP	E2	DO	differential EFM clock output positive	
EFMCLKN	E1	DO	differential EFM clock output negative	
EFMDATP	F1	DO	differential EFM data output positive	
EFMDATN	F2	DO	differential EFM data output negative	
CAL_SH1	Y3	DO	Signal used for drive calibration	
CAL_SH2	Y4	DO	Signal used for drive calibration	
TIMRS	AA1	DO	EFMTIM RF sampling signal	
TIMTH1	Y2	DO	EFMTIM input sampling signal 1	
TIMTH2	Y1	DO	EFMTIM input sampling signal 2	
TIMREF	AA2	DO	EFMTIM slicer reference level	
TIMRWN	AB1	DO	EFMTIM read/write signal for preprocessor	
LDRWN	AB2	DO	Codec read/write signal for laser driver (LASERON)	
WSB	AA3	DO	Bank signal for Write strategy	
VTHR	H1	AI	Threshold voltage from Elantec laser driver	
VDEL	H2	AI	Delta voltage from Elantec laser driver	
AMEAS	J2	AI	Alpha measurement from Cheetah	
IAPCR	G1	AO	Threshold power control to Elantec laser driver	
IAPCW	G2	AO	Delta reference current to Elantec laser driver	
VOPUREF	H3	AIO	Reference voltage to OPU shared with VREFIN	
VREF_LCA	J3	AIO	Laconic reference voltage input	
VREFH	H4	AIO	Decoupling point for Laconic function	
VREFL	J4	AIO	Decoupling point for Laconic function	
LASP	J1	AO	laser power signal to pre-processor	
DAC0_STEPA0	V3	AODO	general purpose DAC output	LADIC step output
GPIO50_ESEN	Y9	B	PI-GPIO 5.0 / DSP GPIO 0	serial enable to Elantec laser driver
GPIO51_ESCLK	Y7	B	PI-GPIO 5.1 / DSP GPIO 1	serial clock to Elantec laser driver
GPIO52_ESDIO	W7	B	PI-GPIO 5.2 / DSP GPIO 2	serial data to/from Elantec laser driver

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Table 3: Pinning list

Symbol	Pin	Type	Main function	Alternative function
GPIO53	W9	B	PI-GPIO 5.3 / DSP GPIO 3	
AUX1_A1	M3	AI	aux ADC input 1 / max value of EFM signal (external beta)	
AUX2_A2	M2	AI	aux ADC input 2 / min value of EFM signal (external beta)	
AUX3_CALF	M1	AI	aux ADC input 3 / average value of EFM signal (if DSIC not used)	
AUX4_VOLUME	L3	AI	aux ADC input 4 / headphone volume setting	
AUX5_SINPHI	L2	AI	aux ADC input 5 / sine input from PCS Hall amplifiers	
AUX6_COSPHI	L1	AI	aux ADC input 6 / cosine input from PCS Hall amplifiers	
AUX7_TEMP	K2	AI	aux ADC input 7 / actuator temperature	
AUX8_ACTEMF	K1	AI	aux ADC input 8 / EMF for actuator damping	
GPAIREF	L4	AO	top of the ADC ladder (to be connected to analogue VDDA)	
D1_TILTN	N2	AI	normalised tilt signal	
D2_TLN	N1	AI	norm. track-loss signal	
D3_REN	P2	AI	norm. radial error signal	
D4_FEN	P1	AI	norm. focus error signal	
S1_MIRN	R2	AI	norm. mirror signal	
S2_XDN	R1	AI	XDN input	
LFREF	M4	AIO	I/O voltage ref. for servo ADC	
IREF	P4	AI	analogue current reference	
FTC	T3	AI	fast track count input	
EC	B1	DO	EMF control (torque control pin on motor driver)	
FG	B2	DIH	Frequency generator (tacho pulse from motor driver)	
RA	A2	DO	radial output (tri-state during reset)	
SL	A1	DO	sledge output (tri-state during reset)	
FO	A4	DO	focus output (tri-state during reset)	
SERVOREF	C4	DO	Programmable PDM output used as reference	
GPIO30_REFSIN	C6	B	PI-GPIO 3.0	PCS sinphi DC offset cancellation
GPIO31_REFCOS	C7	B	PI-GPIO 3.1	PCS cosphi DC offset cancellation
GPIO32_TOS	A3	B	PI-GPIO 3.2	tilt sine output
GPIO33_TOC	B3	B	PI-GPIO 3.3	tilt cosine output
GPIO34_TOSTOCEN	C5	BPU	PI-GPIO 3.4	tilt sine/cosine driver enable
MIUD0	A22	B	Memory interface data 0	

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Table 3: Pinning list

Symbol	Pin	Type	Main function	Alternative function
MIUD1	A21	B	Memory interface data 1	
MIUD2	A20	B	Memory interface data 2	
MIUD3	A19	B	Memory interface data 3	
MIUD4	A18	B	Memory interface data 4	
MIUD5	A17	B	Memory interface data 5	
MIUD6	A16	B	Memory interface data 6	
MIUD7	A15	B	Memory interface data 7	
MIUD8	B21	B	Memory interface data 8	
MIUD9	B20	B	Memory interface data 9	
MIUD10	B19	B	Memory interface data 10	
MIUD11	B18	B	Memory interface data 11	
MIUD12	B17	B	Memory interface data 12	
MIUD13	B16	B	Memory interface data 13	
MIUD14	B15	B	Memory interface data 14	
MIUD15	B14	B	Memory interface data 15	
GPIO35_MIUUBN	C18	B	PI-GPIO 3.5	upper byte enable
GPIO36_MIULBN	C17	B	PI-GPIO 3.6	lower byte enable
GPIO37_MIUA0	C11	B	PI-GPIO 3.7	Memory interface address 0
MIUA1	C22	DO	Memory interface address 1	
MIUA2	B4	DO	Memory interface address 2	
MIUA3	A5	DO	Memory interface address 3	
MIUA4	B5	DO	Memory interface address 4	
MIUA5	A6	DO	Memory interface address 5	
MIUA6	B6	DO	Memory interface address 6	
MIUA7	A7	DO	Memory interface address 7	
MIUA8	B7	DO	Memory interface address 8	
MIUA9	A10	DO	Memory interface address 9	
MIUA10	B10	DO	Memory interface address 10	
MIUA11	A11	DO	Memory interface address 11	
MIUA12	B11	DO	Memory interface address 12	
MIUA13	A12	DO	Memory interface address 13	
MIUA14	B12	DO	Memory interface address 14	
MIUA15	A13	DO	Memory interface address 15	
MIUA16	B13	DO	Memory interface address 16	
MIUA17	A14	DO	Memory interface address 17	
MIUA18	A8	DO	Memory interface address 18	
MIUA19	B8	DO	Memory interface address 19	
MIUCS3	C21	DO	Chip select 3 (ext. ROM)	
MIUWEN	A9	DO	Write enable	
MIUOEN	B22	DO	Output enable	

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Table 3: **Pinning list**

Symbol	Pin	Type	Main function	Alternative function
GPIO10_MIUA20	B9	B	PI-GPIO 1.0 / PI interrupt 0	Memory interface address 20 (default after reset)
GPIO11_MIUA21	C14	B	PI-GPIO 1.1 / PI interrupt 1	Memory interface address 21
GPIO12_IEC958	D22	B	PI-GPIO 1.2 / PI interrupt 2	IEC958 output
GPIO13_SHOCKIN	C9	B	PI-GPIO 1.3 / PI interrupt 3	Shock sensor input
GPIO14_SILD2	C8	B	PI-GPIO 1.4 / PI interrupt 4	SILD for second preprocessor
GPIO15_MIURDY	C15	B	PI-GPIO 1.5 / PI interrupt 5	Memory interface ready
GPIO16_MIUCS0	C16	B	PI-GPIO 1.6 / PI interrupt 6	Chip select 0
GPIO17_MIUCS1	C13	B	PI-GPIO 1.7 / PI interrupt 7	Chip select 1
GPIO20_MIUCS2	C12	B	PI-GPIO 2.0	Chip select 2
GPIO21_TXD1	F21	B	PI-GPIO 2.1	TXD1
GPIO22_RXD1	E21	B	PI-GPIO 2.2	RXD1
GPIO23_TXD2	E22	B	PI-GPIO 2.3	TXD2
GPIO24_RXD2	D21	B	PI-GPIO 2.4	RXD2
GPIO25_SIDA	AA4	B	PI-GPIO 2.5	SIDA for preprocessor
GPIO26_SICL	AB3	B	PI-GPIO 2.6	SICL for preprocessor
GPIO27_SILD	AB4	B	PI-GPIO 2.7	SILD for preprocessor
SCL	W5	IIC	I2C serial clock	
SDA	Y5	IIC	I2C serial data	
DD0	N21	B	Host interface data bus 0	Generic DMA data bus 0
DD1	P21	B	Host interface data bus 1	Generic DMA data bus 1
DD2	R21	B	Host interface data bus 2	Generic DMA data bus 2
DD3	T21	B	Host interface data bus 3	Generic DMA data bus 3
DD4	U21	B	Host interface data bus 4	Generic DMA data bus 4
DD5	V21	B	Host interface data bus 5	Generic DMA data bus 5
DD6	W21	B	Host interface data bus 6	Generic DMA data bus 6
DD7	Y21	B	Host interface data bus 7	Generic DMA data bus 7
DD8	Y22	B	Host interface data bus 8	Generic DMA data bus 8
DD9	W22	B	Host interface data bus 9	Generic DMA data bus 9
DD10	V22	B	Host interface data bus 10	Generic DMA data bus 10
DD11	U22	B	Host interface data bus 11	Generic DMA data bus 11
DD12	T22	B	Host interface data bus 12	Generic DMA data bus 12
DD13	R22	B	Host interface data bus 13	Generic DMA data bus 13
DD14	P22	B	Host interface data bus 14	Generic DMA data bus 14
DD15	N22	B	Host interface data bus 15	Generic DMA data bus 15
DMARQ_GACK	M22	DO	Host interface DMA request	Generic DMA acknowledge
DMACK_GREQ	K22	DIH	Host interface DMA acknowledge	Generic DMA request
DIOW	M21	DI	Host interface write strobe	
DIOR	L22	DI	Host interface read strobe	
IORDY	L21	DO	Host interface ready	
INTRQ	K21	DO	Host interface interrupt request	

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Table 3: **Pinning list**

Symbol	Pin	Type	Main function	Alternative function
DA0_GFB	H22	BH	Host interface address 0	Generic DMA first byte signal
DA1_GWR	J22	BH	Host interface address 1	Generic DMA write strobe
DA2_GRD	H21	BH	Host interface address 2	Generic DMA read strobe
PDIAG	J21	B	Host interface passed test	
CS0	G22	DIH	Host interface chip select 0	
CS1	G21	DIH	Host interface chip select 1	
DASP	F22	BOD	Host interface active slave present	
HRESET	Y20	DIH	Host reset	
GPIO54_BCLK	R20	B	PI-GPIO 5.4 / DSP GPIO 4	Host I2S bit clock output
GPIO55_WCLK	T20	B	PI-GPIO 5.5 / DSP GPIO 5	Host I2S word clock output
GPIO56_DATA	U20	B	PI-GPIO 5.6 / DSP GPIO 6	Host I2S data input/output
GPIO57_SYNC	V20	B	PI-GPIO 5.7 / DSP GPIO 7	Host I2S sync input/output
XDA0	AA6	DO	SDRAM address	
XDA1	AB6	DO	SDRAM address	
XDA2	AA5	DO	SDRAM address	
XDA3	AB5	DO	SDRAM address	
XDA4	AB22	DO	SDRAM address	
XDA5	AA21	DO	SDRAM address	
XDA6	AB21	DO	SDRAM address	
XDA7	AA20	DO	SDRAM address	
XDA8	AB20	DO	SDRAM address	
XDA9	AA19	DO	SDRAM address	
XDA10	AB7	DO	SDRAM address	
XDA11	AB19	DO	SDRAM address	
XDA12	Y17	DO	SDRAM address/bank select	
XDA13	AB8	DO	SDRAM address/bank select	
XDA14	AA7	DO	SDRAM address/bank select	
XDD0	AA10	B	SDRAM data bus	
XDD1	AB11	B	SDRAM data bus	
XDD2	AA11	B	SDRAM data bus	
XDD3	AB12	B	SDRAM data bus	
XDD4	AA12	B	SDRAM data bus	
XDD5	AB13	B	SDRAM data bus	
XDD6	AA13	B	SDRAM data bus	
XDD7	AB14	B	SDRAM data bus	
XDD8	AA14	B	SDRAM data bus	
XDD9	AB15	B	SDRAM data bus	
XDD10	AA15	B	SDRAM data bus	

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Table 3: Pinning list

Symbol	Pin	Type	Main function	Alternative function
XDD11	AB16	B	SDRAM data bus	
XDD12	AA16	B	SDRAM data bus	
XDD13	AB17	B	SDRAM data bus	
XDD14	AA17	B	SDRAM data bus	
XDD15	AB18	B	SDRAM data bus	
XWR	AB10	B	SDRAM write strobe	
XRAS	AB9	B	SDRAM RAS strobe	
XCAS	AA9	B	SDRAM CAS	
XCS	AA8	B	SDRAM chip select	
XCLK	AA18	DO	SDRAM clock	
XDQM	Y18	DO	SDRAM data mask high.low (UDQM/LDQM)	
XCKE	AA22	DO	SDRAM clock enable	
DAC_HP_R	C1	AO	DAC headphone output right	
DAC_LO_R	C2	AO	DAC line output right	
DAC_VREF	C3	AI	DAC voltage reference	
DAC_LO_L	D1	AO	DAC line output left	
DAC_HP_L	D2	AO	DAC headphone output left	
DAC_VPOS	D4	VDDA	DAC supply positive	
DAC_VNEG	D3	VSSA	DAC supply negative	
OSC_IN	V1	AI	crystal oscillator input	
OSC_OUT	V2	AO	crystal oscillator output	
POR_OUTN	W2	BOD	power-on reset output, active low, open drain	
POR_NEG	W3	DIHPU	active low power-on-reset	
PCODE	W11	DIHPD	Test pin, do not connect in application	
TDI	W17	DIPU	JTAG test data input	
TDO	W18	DO	JTAG test data output	
TMS	Y15	DIPU	JTAG test mode select	
TCK	W15	DIHPD	JTAG test clock	
TRST	W13	DIPU	JTAG test reset, external pull-down resistor required, see IEEE 1149.1.	
ADBG0	F20	B	Application debug signal 0 (tri-state default)	
ADBG1	G20	B	Application debug signal 1 (tri-state default)	
ADBG2	H20	B	Application debug signal 2 (tri-state default)	
ADBG3	J20	B	Application debug signal 3 (tri-state default)	
ADBG4	E20	B	Application debug signal 4 (tri-state default)	

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Table 3: Pinning list

Symbol	Pin	Type	Main function	Alternative function
ADBG5	N20	B	Application debug signal 5 (tri-state default)	
ADBG6	K20	B	Application debug signal 6 (tri-state default)	
ADBG7	L20	B	Application debug signal 7 (tri-state default)	
ADBG8	M20	BPD	Application debug signal 8 (tri-state default)	PORCONF0
ADBG9	W20	BPD	Application debug signal 9 (tri-state default)	PORCONF1
ADBG10	D20	BPD	Application debug signal 10 (tri-state default)	PORCONF2
ADBG11	P20	BPD	Application debug signal 11 (tri-state default)	PORCONF3
ADBG12	C20	BPD	Application debug signal 12 (tri-state default)	PORCONF4
ADBG13	C19	BPD	Application debug signal 13 (tri-state default)	PORCONF5
VSSA1	G3	VSSA	analogue ground	
VDDA1	G4	VDDA	analogue supply (3.3V)	
VSSA2	K3	VSSA	analogue ground	
VDDA2	K4	VDDA	analogue supply (3.3V)	
VSSA3	N3	VSSA	analogue ground	
VDDA3	N4	VDDA	analogue supply (3.3V)	
VSSA4	R3	VSSA	analogue ground	
VDDA4	R4	VDDA	analogue supply (3.3V)	
VSSA5	U3	VSSA	analogue ground	
VDDA5	U4	VDDA	analogue supply (3.3V)	
VDD3P1	V4	VDDD	pad digital supply (3.3V)	
VSS3P1	W4	VSSD	digital ground	
VDD3P2	W6	VDDD	pad digital supply (3.3V)	
VSS3P2	Y6	VSSD	digital ground	
VDD3P3	W8	VDDD	pad digital supply (3.3V)	
VSS3P3	Y8	VSSD	digital ground	
VDD3P4	W12	VDDD	pad digital supply (3.3V)	
VSS3P4	Y12	VSSD	digital ground	
VDD3P5	W14	VDDD	pad digital supply (3.3V)	
VSS3P5	Y14	VSSD	digital ground	
VDD3P6	W19	VDDD	pad digital supply (3.3V)	
VSS3P6	Y19	VSSD	digital ground	
VDD3P7	V19	VDDD	pad digital supply (3.3V)	
VSS3P7	U19	VSSD	digital ground	
VDD3P8	P19	VDDD	pad digital supply (3.3V)	

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Table 3: Pinning list

Symbol	Pin	Type	Main function	Alternative function
VSS3P8	N19	VSSD	digital ground	
VDD3P9	M19	VDDD	pad digital supply (3.3V)	
VSS3P9	L19	VSSD	digital ground	
VDD3P10	K19	VDDD	pad digital supply (3.3V)	
VSS3P10	J19	VSSD	digital ground	
VDD3P11	H19	VDDD	pad digital supply (3.3V)	
VSS3P11	G19	VSSD	digital ground	
VDD3P12	D19	VDDD	pad digital supply (3.3V)	
VSS3P12	D18	VSSD	digital ground	
VDD3P13	D15	VDDD	pad digital supply (3.3V)	
VSS3P13	D14	VSSD	digital ground	
VDD3P14	D13	VDDD	pad digital supply (3.3V)	
VSS3P14	D12	VSSD	digital ground	
VDD3P15	D9	VDDD	pad digital supply (3.3V)	
VSS3P15	D8	VSSD	digital ground	
VDD3P16	D7	VDDD	pad digital supply (3.3V)	
VSS3P16	D6	VSSD	digital ground	
VDD3P17	F4	VDDD	pad digital supply (3.3V)	
VSS3P17	F3	VSSD	digital ground	
VDD18C1	W10	VDDD	core digital supply (1.8V)	
VSS18C1	Y10	VSSD	digital ground	
VDD18C2	W16	VDDD	core digital supply (1.8V)	
VSS18C2	Y16	VSSD	digital ground	
VDD18C3	T19	VDDD	core digital supply (1.8V)	
VSS18C3	R19	VSSD	digital ground	
VDD18C4	F19	VDDD	core digital supply (1.8V)	
VSS18C4	E19	VSSD	digital ground	
VDD18C5	D17	VDDD	core digital supply (1.8V)	
VSS18C5	D16	VSSD	digital ground	
VDD18C6	D11	VDDD	core digital supply (1.8V)	
VSS18C6	D10	VSSD	digital ground	
VDD18P1	E4	VDDD	pad digital supply (1.8V)	
VSS18C7	E3	VSSD	digital ground	

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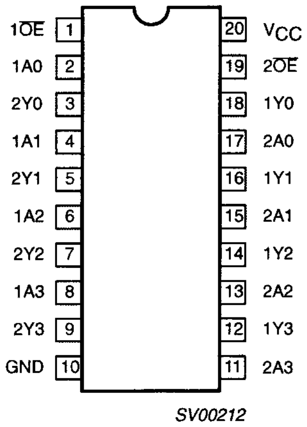
IC 7802 74LVC244APW, LECO Board, Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Bus inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	$2\overline{OE}$	Output enable input (active-LOW)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION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2Y0 3
1A1 4
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2Y2 7
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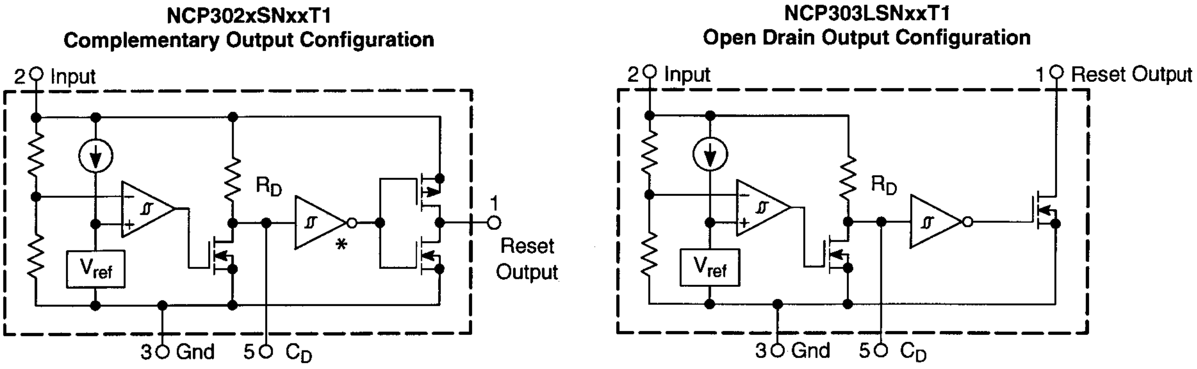
2Y3 9
GND 10
20 VCC
19 2OE
18 1Y0
17 2A0
16 1Y1
15 2A1
14 1Y2
13 2A2
12 1Y3
11 2A3
SV00212

IC 7925 NCP303LSN29, LECO Board, Voltage Detector Series with Programmable Delay

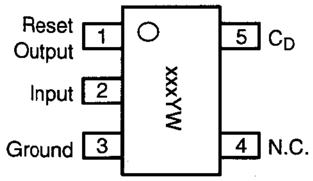

NCP302xSNxxT1
Complementary Output Configuration
2 Input
RD
Vref
1
Reset Output
*
3 Gnd
5 CD
NCP303LSNxxT1
Open Drain Output Configuration
2 Input
1 Reset Output
RD
Vref
3 Gnd
5 CD

* Inverter for active low devices.
Buffer for active high devices.

This device contains 28 active transistors.

Figure 1. Representative Block Diagrams

PIN CONNECTIONS AND MARKING DIAGRAM



xxx = 302 or 303
Y = Year
W = Work Week

(Top View)

9.5 List of Abbreviations

MOBO (Analog) Board

+5VSTBY	Permanent Supply 5V
8SC2	Pin8 Scart2 (only for Europe)
A_DATA	Data from Analog- to Digital-Board (UART-Communication)
A_RDY	Analog-board ready (status information to digital-board)
A18 - A19	Parallel Address Bus (CC - Flash-ROM and S-RAM)
A8 - A17	Parallel Address Bus (CC - Flash-ROM and S-RAM)
AD0 - AD7	Parallel Address Bus (CC - Flash-ROM and S-RAM)
AFC	Automatic Frequency Control
AFEL	Audio Frontend Left
AFER	Audio Frontend Right
AGC / WSRI	Automatic Gain Control (for Europe), Wide Screen Rear In (for NTSC)
AINFL	Audio In Front Left
AINFR	Audio In Front Right
AKILL	Audio Kill Signal
ALADC	Audio Left to ADC
ALDAC	Audio Left from DAC
ALE	Address Latch Enable
AM0	Adress-mode 0
AM1	Adress-mode 1
ARADC	Audio Right to ADC
ARDAC	Audio Right from DAC
ASCC1	Audio Scart 1 Mute (System Clock Output for Real time Clock-Adjustment)
AVCC	Power Supply for A/D-converter
AVSS	GND-Pin for A/D-converter
CFIN	Chroma Front In
CS0_	Chip Select 0 (CC - S-RAM)
CS2_	Chip Select 2 (CC - Flash-ROM)
CVBSFIN	Video Front In
D_DATA	Data from Digital- to Analog-Board (UART-Communication)
D_RDY	Digital-board ready (status information from digital-board)
DAC_MUTE	Mute Signal for DAC
DAOUT	Digital Audio Out
DVAL	Audio from Digital Video In Left
DVAR	Audio from Digital Video In Right
DVCC1	Power Supply Pin
DVCC2	Power Supply Pin
DVCC3	Power Supply Pin
DVSS1	GND Pin
DVSS2	GND Pin
DVSS3	GND Pin
FAN_OFF	Fan for Basic engine
FBIN	Fast Blanking input
FOME	FOllow ME Status line (matching signals yes/no; only for Europe)
G1...10	DISPLAY GRID
INT	Interrupt OUT for the CC
INT	Interrupt – line from Display Print
ION	Inverse ON-Line
IPFAIL	Inverse Power Fail Detection
IPOR	Inverse Power On Reset
IRESET	Inverse Reset Input
K1	Key-Input-Line
K2	Key-Input-Line
KILL	Signal from IR-Receiver
P50 IN	P50 INput-line (only for Europe)
P50 OUT	P50 OUTput-line (only for Europe)
POR_DC	Power On Reset for Display Control Print (Ext_DL)
PSS	Output Enable ReaD (CC - Flash-ROM and S-RAM)
PWM_FIL	Control line for Filament Voltage Generation
PWONSW	Amplifier Switch Audio A/D Converter
RD_	Pal/Secam-Select
RECLED	Control Signal for REC-LED
RESET_DIG	Reset Line to Digital Board
RP_	Inverse Reset line to Flash-ROM
RSA1/2	Record Selector 1/2
RY/BY_	Ready/Busy – input line (from Flash-ROM)
SIF1	Sound intermediate frequency
SB1	Secam Band 1 (PCB-Test entrance)
SCL	IC-Bus
SCLSW	Switched I^{2}C-Bus
SDA	IC-Bus
SDASW	Switched I^{2}C-Bus
SFS_TS	SAW Filter Select Trap Select
STBY	Standby-Line (Flash_Toshiba)
SYNC	Video Sync input
TEMP_SENSE	Temperature Sense Line
VER	HW-version input
VFV	Video from Frontend
VKK	VFT Driver Power Supply
VREFH	Pin for Reference-voltage input to A/D-converter
VREFL	Pin for Reference-voltage input to A/D-converter
VS1/2	View Selector 1/2
WR_	Write Enable (CC - Flash-ROM and S-RAM)
WSFI	Wide Screen Signalling Front In
WU	Wake Up
X1	Oscillator Pin
X12	Oscillator Pin
XIN	Oscillator Pin
XOUT	Oscillator Pin
XT1	Low Frequency Oscillator Pin
XT2	Low Frequency Oscillator Pin
YFIN	Luminance Front In

FEBE Board (Backend part)

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DENC	Digital (Video) Encoder (Video DAC)
DV	Digital Video (Camcorder)
EF	Emitter Follower
OSD	On-Screen Display
VIP	Video Input Processor (Video ADC)
2Fh	Progressive scan video
2V5	+2V5 Power supply for Link+Codec IC7431
3V3	+3V3 Power supply
3V3_A	+3V3 Analog power supply for PHY IC7400
3V3_D	+3V3 Digital power supply for PHY IC7400

3V3_DLY	+3V3 Power supply for IC7500
3V3_LINK	+3V3 Power supply for Link+Codec IC7431
3V3_F	+3V3 Power supply for optional Flash memory IC7432
3V3_RAM	+3V3 Power supply for SDRAM IC7430
3V3_uP	+3V3 Power supply for Microcontroller IC7802
3V3_32kHz	+3V3 Power supply for audio format adaptation circuitry IC7507 and IC7508
3V3_AC	+3V3 Power supply for audio system clock generator IC7605 and IC7606
+5V	+5V Power supply
5V_PLL	+5V Power supply for VCO of audio PLL IC7604
A (1:17)	Flash address lines of uPD72893
A_MUTE	Audio Mute
ABCK	Audio Bit Clock
AD (1:10)	Address bus lines for Host I/F of Link+Codec IC7431
AEMP1	PCM1 emphasis ON/OFF for PCM1 output
AFS1	Audio sampling frequency indication signal
ALRCLK	Audio Word Select
AMCLK44	11.2896MHz (=256 * 44.1 kHz) audio master clock signal for 44.1 kHz audio
AMCLK48	12.288MHz (=256 * 48 kHz) audio master clock signal for 32 kHz and 48 kHz audio
APWM	PWM signal for audio PLL
ASIC	Application Specific Integrated Circuit
BUFENn_AUD	Buffer Enable Audio
BUFENn_VID	Buffer Enable Video
CLK27M_CON	27MHz Clock to Digital Board
CS	Parallel interface chip select input of Link+Codec IC7431
CTL (0:1)	Link interface control lines
CTSN	Clear to Send
D (0:15)	Flash data lines of Link+Codec IC7431
DCDi	Directional Correlational Deinterlacing. Circuitry that reduces jaggies on diagonal edges when deinterlacing video-sourced material.
DV_STATUS	Interrupt pin for reading DV-status
HS_CLK	Video clock input of Link+Codec IC7431
INT	Interrupt request output of Link+Codec IC7431 (input to Micro-Controller)
IOR	Parallel interface IO read control input of Link+Codec IC7431
ISPN	In System Programming signal (used for programming IC7802)
LKON	Link-on signal outputLPSLink power status inputLREQLink request input
MA (0:10)	SDRAM address lines of Link+Codec IC7431
MCAS	SDRAM column address strobe signal
MCLK	SDRAM clock signal
MD (0:15)	SDRAM data lines of Link+Codec IC7431
MRAS	SDRAM row-address strobe signal
MWE	SDRAM write enable signal
PCM1	Audio Serial Data Output of Link+Codec IC7431
PCM1_NEW	'MSB justified' to I2S converted audio serial data; audio serial data input of audio DAC UDA1334A
PD (0:15)	Data bus lines for Host I/F of Link+Codec IC7431
PHY_D (0:7)	Data bus connection between PHY and LINK device
RESETn	DVIO board reset
RESET_FM	Reset signal driven by Flashmaster programming device
RESTB	Reset input of Link+Codec IC7431
RTSN	Request to Send
RWZ	Parallel interface read/write control input of Link+Codec IC7431
RXD	Receive Data
SCLK	Link control output clock
TXD	Transmit Data
VPP	+10V switchable programming voltage of microcontroller
YUV (0:7)	Digital Video

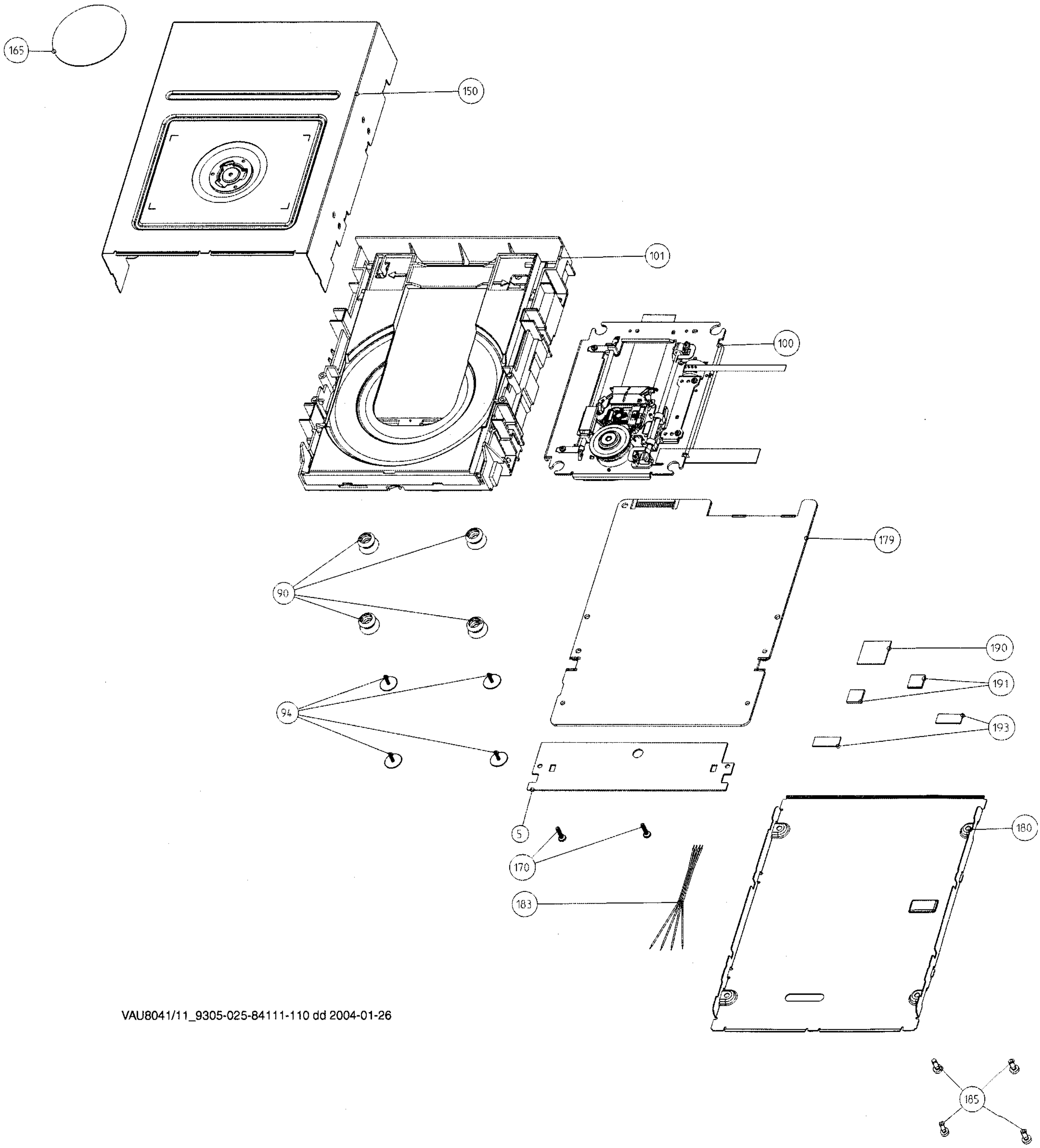
FEBE Board (Frontend part)

ADC	Analogue to Digital Converter
ADIP	ADdress In Pre-groove
AGC	Automatic Gain Control
CD	Compact Disc
CLV	Constant Linear Velocity
DROPPI	Dvd Rewritable Opu Pre-Processor IC
AM	Amplitude Modulation
BE	Basic Engine
ComPair	Computer aided rePair
CD-DA	CD Digital Audio
CS	Chip Select
DAC	Digital to Analogue Converter
DAIO	Digital Audio Input Output
DENC	Digital Encoder
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DRAM	Dynamic RAM
DSD	Direct Stream Digital
DSP	Digital Signal Processing
DVD	Digital Versatile Disc
EEPROM	Electrical Erasable Programmable ROM
EFM	Eight to Fourteen bit Modulation
FDS	Full Diagnostic Software
HF	High Frequency
I^2C	Integrated Ic bus (signals at 5V level)
I2S	Integrated Ic Sound bus (signals at 3.3V level)
IC	Integrated Circuit
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
LADIC	LAser Driver IC
LLD	Loss Less Decoder
LPCM	Linear Pulse Code Modulation
LRCLK	Left/Right CLocK
MACE	Mini All Cd Engine
MPEG	Motion Pictures Experts Group
NC	Not Connected
NVM	Non Volatile Memory: IC containing DVD related data e.g. alignments
OPC	Optimum Power Calibration
OPU	Optical Pickup Unit
PCB	Printed Circuit Board (see PWB)
PCS	Position Control Sledge
PLL	Phase Locked Loop
PCM	Pulse Code Modulation
PCM_CLK	Audio system clock for DAC
PCM_OUTx	Audio serial output data
PSU	Power Supply Unit
PWB	Printed Wiring Board (see PCB)
RAM	Random Access Memory
RGB	Red, Green and Blue colour space
ROM	Read Only Memory
RF	Radio Frequency
S2B	Serial to Basic engine, communication bus between host- and servo processor
SCL	Serial Clock I^2C

SCLK	Audio serial bit clock
SDA	Serial Data I^2C
SDRAM	Synchronous DRAM
SMC	Surface Mounted Components
S/PDIF	Sony Philips Digital InterFace
SPIDRE	Signal Processing Ic for Dvd REwritable
SRAM	Static Random Access Memory
STBY	STandBY
SVCD	Super Video CD
SW	SoftWare
THD	Total Harmonic Distortion
TTL	Transistor Transistor Logic (5V logic)
uP	Microprocessor
VCD	Video CD
Y/C	Luminance (Y) and Chrominance (C) signal
YUV	Component video

10. Spare Parts List

10.1 Exploded View of FEBE Module (VAU8041)


165
150
101
100
179
90
94
190
191
193
5
170
183
180
185

VAU8041/11_9305-025-84111-110 dd 2004-01-26

Figure 10-1

10.2 Exploded View of Lecolite Module

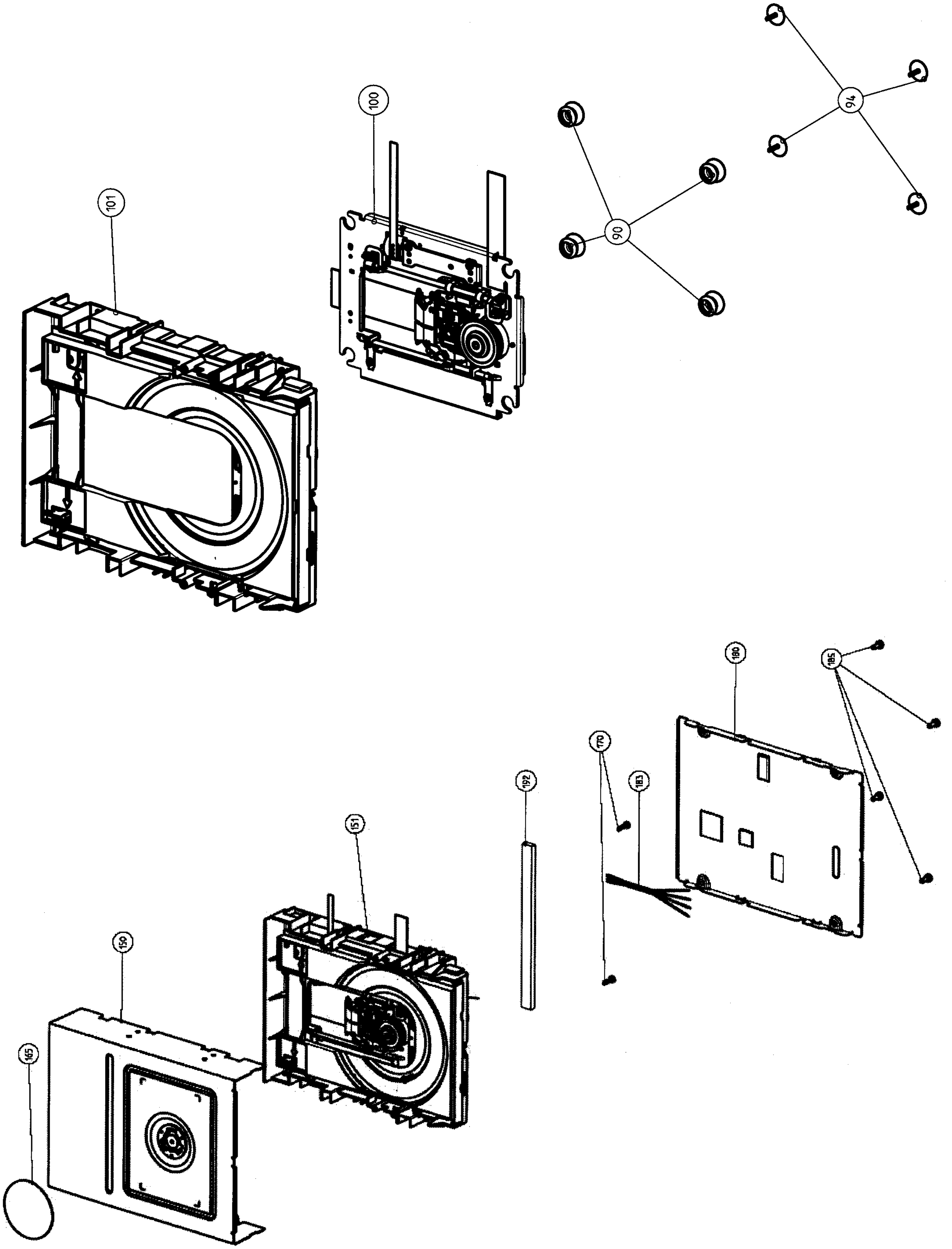
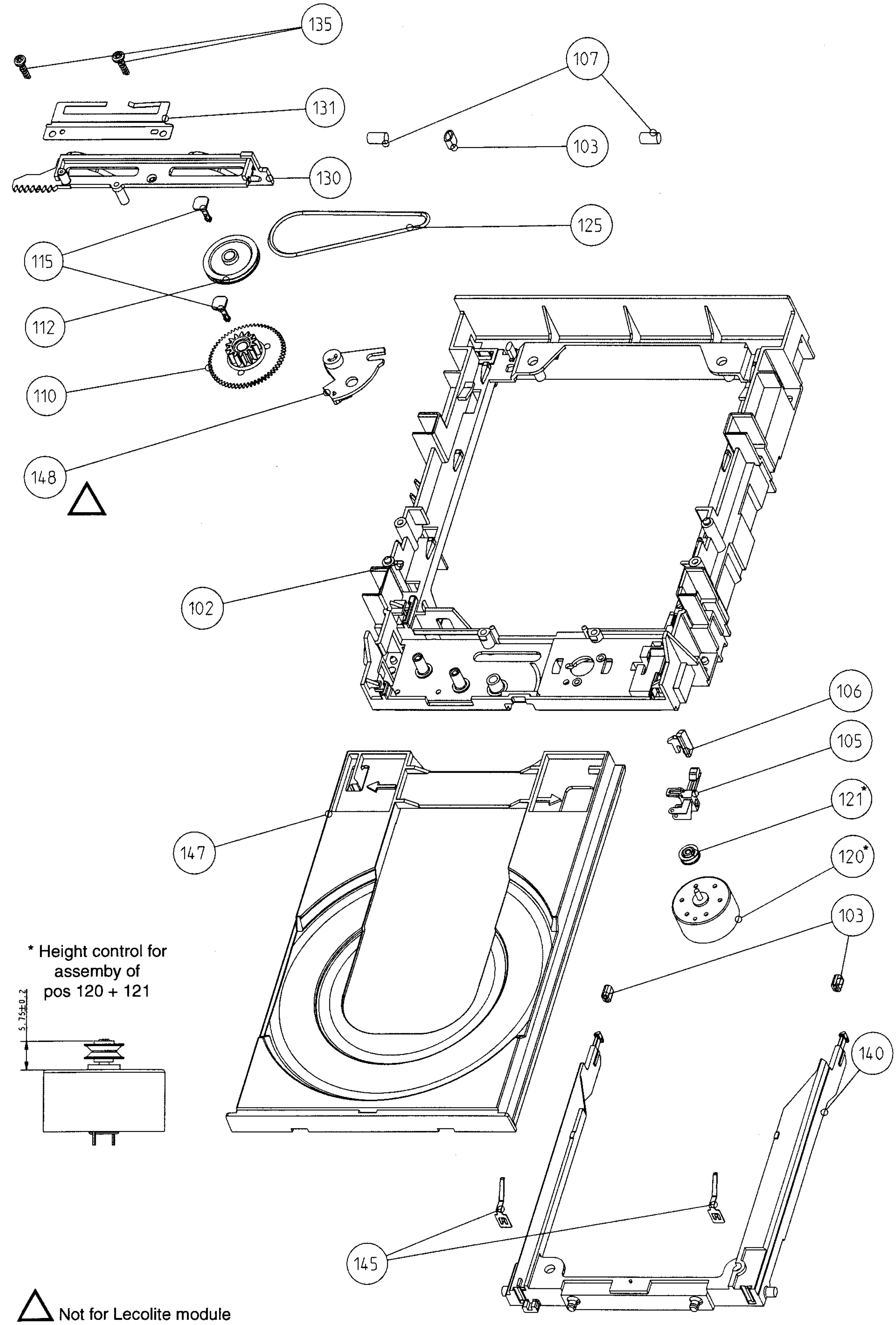

94
100
90
101
180
185
170
183
192
151
150
165

Figure 10-2

10.3 Exploded View of the Loader Mechanism

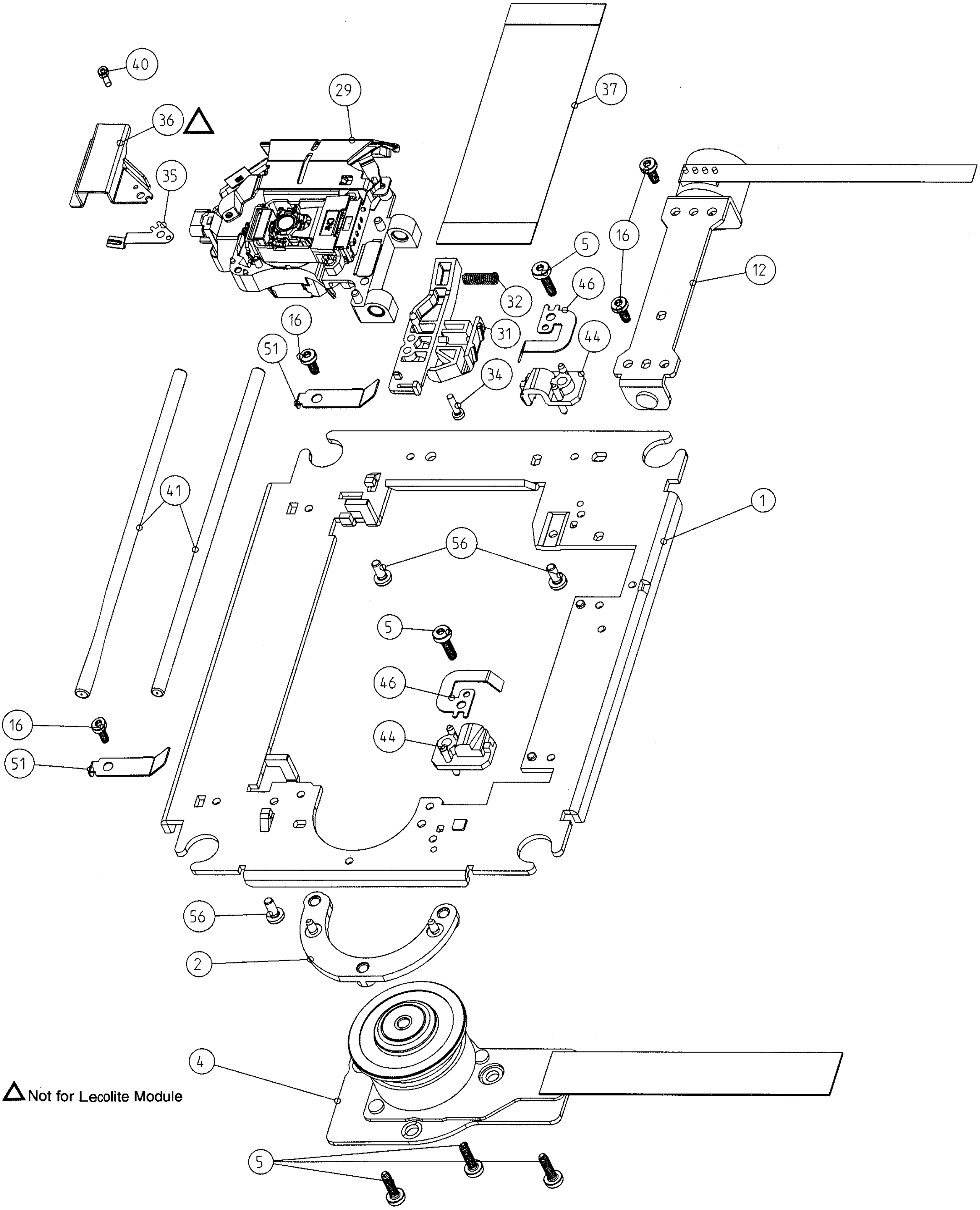

135
107
131
103
130
125
115
112
110
148
102
106
105
121*
120*
103
147
* Height control for assemby of pos 120 + 121
5.75±0.2
140
145

△ Not for Lecolite module

AV3.5 Loader Assy_3139-197-60291-110 dd 2004-02-13 (POS)

Figure 10-3

10.4 Exploded View of the DVDR Drive Mechanism

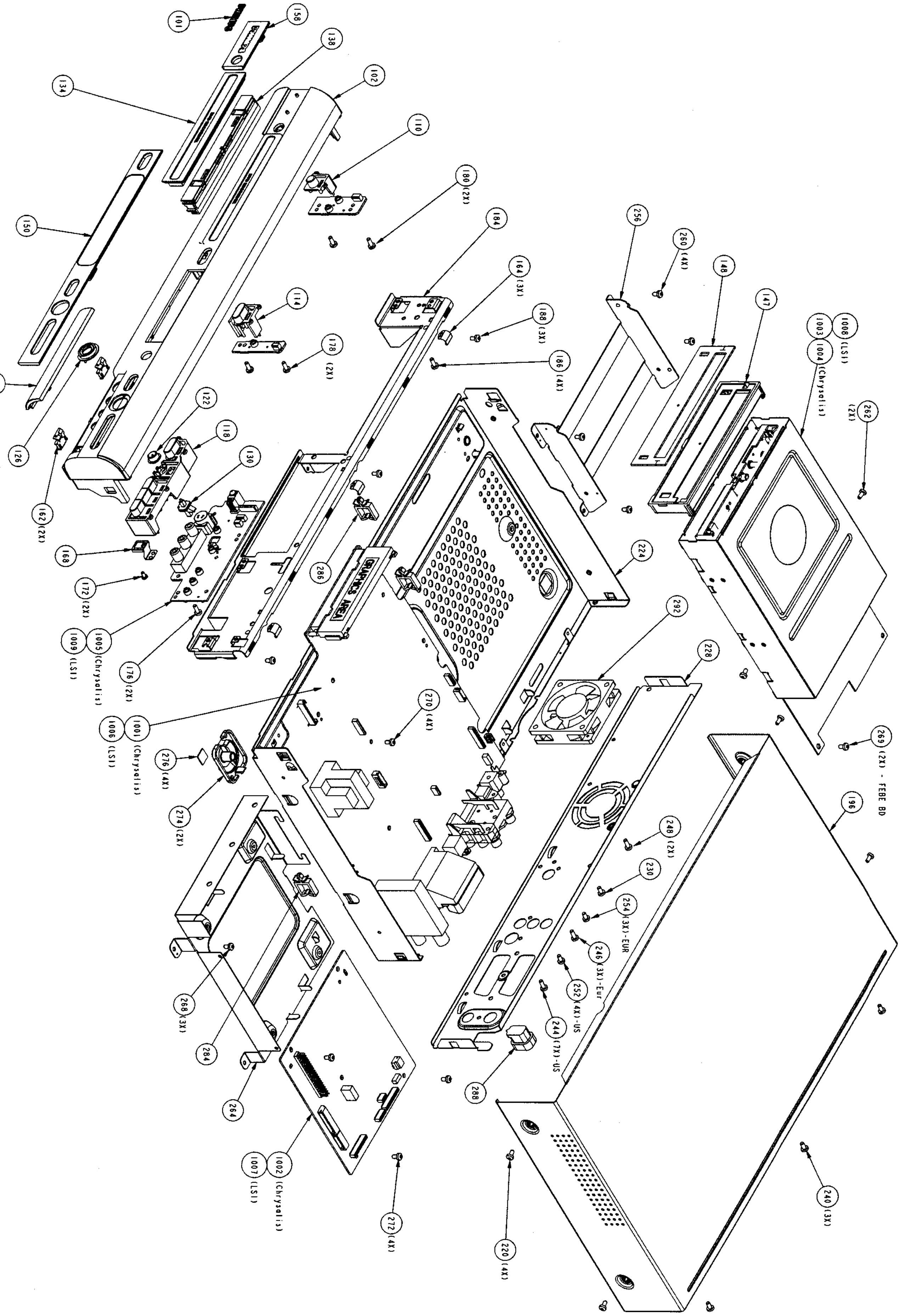

40
29
37
36
35
16
5
16
12
46
32
31
44
16
51
34
41
1
56
5
46
44
16
51
56
2
4
5

△ Not for Lecolite Module

AV3.5 Mechanism_3139-197-50301-110 dd 2004-02-13 (POS)

Figure 10-4

10.5 Exploded View of the Set


101
158
138
134
102
110
180 (2X)
150
184
256
260 (4X)
148
164 (3X)
188 (3X)
147
1008 (LS1)
1003
1004 (Chrysalis)
114
178 (2X)
186 (4X)
262 (2X)
160
122
118
126
130
162 (2X)
224
168
286
292
172 (2X)
1005 (Chrysalis)
1009 (LS1)
176 (2X)
228
270 (4X)
1001 (Chrysalis)
1006 (LS1)
269 (2X) - FEBE BD
276 (4X)
274 (2X)
196
248 (2X)
230
254 (3X)-EUR
246 (3X)-Eur
252 (4X)-US
244 (7X)-US
268 (3X)
284
288
264
1002 (Chrysalis)
1007 (LS1)
272 (4X)
220 (4X)
240 (3X)

DVDR615_00_8622-610-11632-110 dd wk417

Figure 10-5

MISCELLANEOUS - SET EXPLODED VIEW

Various

101	3139 247 51831	BADGE PHILIPS ASSY SILVER
102	3139 244 04741	CABINET FRONT DVDR610/00/02/19/33
102	3139 244 04731	CABINET FRONT DVDR610/05
102	3139 244 04671	CABINET FRONT DVDR615/00/02/19/33
102	3139 244 04751	CABINET FRONT DVDR615/05
102	3139 244 05621	CABINET FRONT DVDR616/00/02
102	3139 244 05611	CABINET FRONT DVDR616/05
110	3139 244 04561	BUTTON STANDBY
114	3139 244 04531	BUTTON EJECT
118	3139 244 04521	BUTTON SET
122	3139 244 04491	BUTTON CAP REC
126	3139 244 04511	RING REC
130	3139 244 04501	LIGHT GUIDE REC
134	3139 244 04551	COVER TRAY
138	3103 604 00811	HOLDER COVER TRAY
147	3103 604 01141	COVER DUST
148	3103 603 20122	FOAM RUBBER SEALING
150	3139 244 04541	WINDOW DVDR610/615
150	3139 244 04711	WINDOW DVDR616
158	3139 244 04481	WINDOW LEFT DVDR610/615
158	3139 244 04701	WINDOW LEFT DVDR616
160	3139 244 04721	DOOR FLAP DVDR610
160	3139 244 04471	DOOR FLAP DVDR615/616
162	3103 604 00441	HINGE DOOR FRONT AV
164	3103 601 20231	SPRING GROUND
168	3103 601 20212	SPRING I-LINK DVDR615/616
196	3139 241 21871	COVER TOP
274	3103 604 00622	FOOT
276	3103 603 20041	CUSHION FOOT
288	4822 532 60948	BUSH, MAINS CORD
292	2822 031 01441	FAN 12VDC 0.7W 3000RPM B
333	3139 248 72121	REMOTE CONTROL
336	2422 070 98231	MAINS CORD IEC 2A5 1M8 / 00/02/19/33
336	2422 070 98236	MAINS CORD UK 5A 1M8 / 05
342	2422 076 00532	CBLE SCART 1M5 SCART 21P BK B
345	4822 320 50377	CONNECT. CABLE PAL
1001	3139 248 82891	PCBAS MOBO BOARD 04 E1
1004	9305 025 84111	VAU8041/21 (PHOS) Y DVDR610
1004	9305 025 84121	VAU8041/21 (PHOS) Y DVDR615/616
8003	3139 111 04001	FFC FOIL 15P/180/15P BD 1MMP
8007	3139 111 03991	FFC FOIL 22P/280/22P BD 1MMP
8008	3139 110 34891	FFC FOIL 22P/120/22P AD 1MMP
8010	3139 111 03981	FFC FOIL 10P/280/10P BD 1MMP
8011	2422 076 00578	CBLE IEEE1394 F/480/SHR B DVDR615/616

MISCELLANEOUS VAU8041 MODULE EXPLODED VIEW

Various

5	3139 194 01581	SEALING STRIP
12	3104 148 01950	SLEDGE MOTOR
90	3104 144 10730	SUSPENSION
94	3139 190 40231	T6 PAN HEAD M2X8.5 TT-P SEMS FW
100	3139 197 50301	AV3.5 MECHANISM ASSY (DVD-M)
101	3139 197 60291	AV3.5 LOADER ASSY
105	3139 198 80010	SEALING STRIP
120	3139 198 00620	TRAY MOTOR
121	3104 144 04980	MOTOR PULLEY, TRAY
125	3104 144 10121	TRAY MOTOR BELT
147	3104 144 04272	TRAY
150	3139 197 60301	TOP PLATE ASSY
179	3104 128 09271	FEBE PCBA 4MB/32MB NO DV-IN DVDR610
179	3104 128 09281	FEBE PCBA 4MB/32MB W/ DV-IN DVDR615/616
190	3139 194 01541	HEAT SINK PAD (CENTAURUS)
191	3139 194 01551	HEAT SINK PAD (CHEETAH)
193	3139 194 01561	HEAT SINK PAD (DRIVER)

MISCELLANEOUS LECO MODULE EXPLODED VIEW

Various

0012	3139 198 01201	SLEDGE MOTOR SPS-15RF-075KP
0090	3104 144 10730	SUSPENSION
0094	3139 190 40231	T6 PAN HEAD M2X8.5 TT-P SEMS FW
0100	3139 197 50341	D4.0 MECHANISM ASSY
0101	3139 197 60331	D4.0 LOADER ASSY
0105	3139 198 80010	SWITCH
0120	3139 198 01211	TRAY-MOTOR TRICORE DM24215
0121	3104 144 04980	"MOTOR PULLEY, TRAY"
0125	3104 144 10121	TRAY MOTOR BELT
0147	3104 144 04272	TRAY
0150	3139 247 60451	ASSEMBLY TOP PLATE D4.0

MOBO (ANALOG) BOARD

Various

1100	2722 171 00042	VFD DISPLAY BJ928GN
1101	4822 242 82114	CERAM RESONATOR 8MHZ
1102	4822 242 70938	RES XTL 32KHZ768 12P5 DT-38 B
1120	4822 276 13732	SWITCH TACT PUSH
1122	4822 276 13732	SWITCH TACT PUSH
1202	4822 276 13732	SWITCH TACT PUSH
1203	4822 276 13732	SWITCH TACT PUSH
1205	4822 276 13732	SWITCH TACT PUSH
1209	4822 276 13732	SWITCH TACT PUSH
1210	4822 276 13732	SWITCH TACT PUSH
1300▲	4822 071 51002	FUSE RAD LT 1A 250V IEC A
1301▲	9965 000 07788	FUSE RAD T2A IEC UL250V
1302▲	4822 252 11215	SURGE PROTECT DSP-301N-A21F A
1303▲	4822 265 11253	SOC FUSE V 1P F PTF/65 B
1304▲	2422 086 10786	FUSE RAD LT 4A 250V IEC A
1305▲	2422 086 10899	FUSE 5X20 ET 1A25 250V IEC B
1306▲	4822 071 55001	FUSE RAD LT 500MA 250V IEC A
1308▲	4822 071 51002	FUSE RAD LT 1A 250V IEC A
1310▲	2422 086 10769	FUSE RAD LT 125MA 250V IEC A
1600	2422 543 01427	RES XTL 18M432 12P HC49/US A
1700	2422 542 90147	TUN IF V+U PLL IEC BGIDKL B
1900	4822 265 11154	CON V 22P F 1.00 FFC 0.3 B
1915	4822 267 11031	CON V 10P F 1.00 FFC 0.3 B
1920	2422 026 05301	SOC CINCH V 3P FJPJ1127 B
1921	2422 026 05307	CON MDIN H 4P F YKF51 B
1922	2422 025 17797	CON V 15P F 1.00 FFC 0.3 B
1931▲	4822 265 20723	CON BM V 2P M 7.92 VH B
1940	2422 033 00334	CON BM EURO H 42P F BK GRND-L
1942	2422 025 17797	CON V 15P F 1.00 FFC 0.3 B
1945	2422 026 05308	SOC CINCH H 3P F YEWHRD Y
1947	4822 265 11154	CON V 22P F 1.00 FFC 0.3 B
1948	4822 267 10994	SOC MDIN H 4P F TCS7927 B
1955	4822 267 31729	SOC CINCH H 1P F BK B

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2102	4822 124 11968	SUPCAP SE 5V5 S 220MF P80M20 A
2301	2020 554 90173	CERSAF KX 250V S 2,2NF PM20 B
2302	2020 021 91506	ELCAP ZL 16V S 1000UF PM20 B
2306	4822 122 31175	1NF 10% 500V
2308	4822 122 31175	1NF 10% 500V
2309	2020 021 91506	ELCAP ZL 16V S 1000UF PM20 B
2311▲	4822 121 10512	275V 220NF 20%
2313	4822 121 70386	47NF 10% 250V
2315▲	2022 020 00742	ELCAP LS 400V S 68UF PM20 B
2316	2020 021 91506	ELCAP ZL 16V S 1000UF PM20 B
2318▲	4822 126 14525	47PF 5% 1KV
2321	2020 021 91506	ELCAP ZL 16V S 1000UF PM20 B
2324	4822 121 41857	10NF 5% 250V
2326	4822 126 10206	2,2NF 10% 500V
2327	4822 121 51598	2,2NF 5% 400V

-ww-

3211	4822 117 12063	NTC DC 5W 10K 5%
3300▲	4822 053 21335	3M3 5% 0,5W
3301▲	4822 053 21335	3M3 5% 0,5W
3318▲	4822 053 21684	680K 5% 0,5W
3330	2322 193 14477	RST MFLM PR01 A 0,47R PM5 A
3331	2322 193 14687	RST MFLM PR01 A 0,68R PM5

-~-

5100	2422 549 43062	IND FXD EMI 100MHZ 600R R
5101	4822 157 50964	100MUH
5300▲	2422 531 02546	TFM SMT SLOT SRW28EC9-E01V0* B
5301	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5302▲	2422 549 44509	FIL MAINS 25MH 0A4 HF2022R Y
5303	4822 157 11737	22UH 10% 9X9,5
5304	4822 157 11737	22UH 10% 9X9,5
5305	4822 157 70826	2,4UH
5306	4822 157 11737	22UH 10% 9X9,5
5307	4822 157 70826	2,4UH
5401	4822 157 11706	10UH 5% 2,4X3,4
5402	4822 157 11706	10UH 5% 2,4X3,4
5551	2422 536 00019	TRANSFORMER 6RG (SAGA) B
5600	4822 157 11706	10UH 5% 2,4X3,4
5601	4822 157 11706	10UH 5% 2,4X3,4
5700	4822 157 11737	22UH 10% 9X9,5
5701	2422 549 43062	IND FXD EMI 100MHZ 600R R
5702	2422 549 43062	IND FXD EMI 100MHZ 600R R
5703	2422 549 43062	IND FXD EMI 100MHZ 600R R
5704	4822 157 11706	10UH 5% 2,4X3,4
5801	4822 157 11706	10UH 5% 2,4X3,4
5802	2422 549 43062	IND FXD EMI 100MHZ 600R R
5803	2422 549 43062	IND FXD EMI 100MHZ 600R R

-▷|-

6002	4822 130 11397	BAS316
6003	4822 130 11397	BAS316
6004	4822 130 11397	BAS316
6006	4822 130 11397	BAS316
6007	4822 130 11397	BAS316
6100	4822 130 80622	BAT54
6101	4822 130 80622	BAT54
6102	4822 130 11416	PDZ6.8B
6103	4822 130 11397	BAS316
6104	4822 130 11397	BAS316
6105	4822 130 11397	BAS316
6108	4822 130 11397	BAS316
6114	4822 130 11397	BAS316
6188	4822 130 80622	BAT54
6200	9340 548 61115	PDZ12B
6201	9340 548 61115	PDZ12B
6202	9340 548 61115	PDZ12B
6203	9340 548 61115	PDZ12B
6204	9340 548 61115	PDZ12B
6211	9322 190 44676	LED VS LTL-1MHHR
6300	9322 161 76682	SB340L-7024
6301	9322 161 76682	SB340L-7024

6302	4822 130 31083	BYW55
6303	4822 130 31083	BYW55
6304	9322 184 68682	STPS5L40-C2
6305	4822 130 31083	BYW55
6306	9322 184 68682	STPS5L40-C2
6307	4822 130 31083	BYW55
6308	9322 126 71673	BYT42M A
6309	9322 161 78682	SB360L-7024
6310	4822 130 31878	1N4003G
6311	4822 130 10871	SBYV27-200
6312	4822 130 11397	BAS316
6313	4822 130 11416	PDZ6.8B
6314	3198 020 55680	BZX384-C5V6
6315	4822 130 41601	BYV95A
6316	4822 130 34142	BZX79-B33
6317	4822 130 80622	BAT54
6318	4822 130 41601	BYV95A
6319	4822 130 30842	BAV21
6320	9340 548 69115	PDZ27B
6321	4822 130 34382	BZX79-B8V2
6322	4822 130 11397	BAS316
6401	4822 130 11416	PDZ6.8B
6402	4822 130 11416	PDZ6.8B
6403	4822 130 11416	PDZ6.8B
6404	4822 130 11416	PDZ6.8B
6405	9340 548 61115	PDZ12B
6406	9340 548 61115	PDZ12B
6407	9340 548 61115	PDZ12B
6408	9340 548 61115	PDZ12B
6409	4822 130 11416	PDZ6.8B
6410	9340 548 61115	PDZ12B
6411	9340 548 61115	PDZ12B
6412	9340 548 61115	PDZ12B
6413	9340 548 61115	PDZ12B
6414	9340 548 61115	PDZ12B
6415	9340 548 61115	PDZ12B
6416	4822 130 11416	PDZ6.8B
6417	4822 130 11416	PDZ6.8B
6418	9340 548 61115	PDZ12B
6419	9340 548 61115	PDZ12B
6420	9340 548 61115	PDZ12B
6421	9340 548 61115	PDZ12B
6422	9340 548 61115	PDZ12B
6423	9340 548 61115	PDZ12B
6424	4822 130 11397	BAS316
6600	4822 130 11397	BAS316
6803	9340 548 61115	PDZ12B
6804	9340 548 61115	PDZ12B
6805	4822 130 11522	UDZ15B
6806	9340 548 61115	PDZ12B
6807	4822 130 11522	UDZ15B

7000	3198 010 42320	BC857BW
7001	4822 130 60854	DTA124EU-W
7002	4822 130 60854	DTA124EU-W
7004	9322 148 78668	AD1852JRS
7005	4822 209 62312	MC33078D
7006	4822 130 60854	DTA124EU-W
7008	9352 670 99118	UDA1361TS/N1
7009	4822 130 61553	DTC124EU
7045	3198 010 42310	BC847BW
7100	9322 196 98685	NCP301LSN47
7101	4822 130 61553	DTC124EU
7102	4822 130 40981	BC337-25
7103	3198 010 42310	BC847BW
7104	4822 130 41246	BC327-25
7105	3198 010 42310	BC847BW
7106	4822 130 41246	BC327-25
7107	3139 240 50861	TMP87CM74AFG-5JP4 w/ mark “ASP017-50861" (Lead-free)
7107	3139 240 50921	TMP87CM74AF-5JP4 w/ mark “ASP017-50921" (non Lead-free)
7108	3198 010 42310	BC847BW
7110	3198 010 42310	BC847BW
7111	4822 130 61553	DTC124EU
7112	3198 010 42310	BC847BW
7113	3198 010 42320	BC857BW
7114	9965 000 04199	BSN20
7115	9965 000 04199	BSN20
7116	3198 010 42320	BC857BW
7118	3198 010 42310	BC847BW
7123	3198 010 42310	BC847BW
7124	3198 010 42310	BC847BW
7200	9322 185 95667	IR RECEIVER TSOP4836
7300	9322 183 38668	STS9NF30L
7301	4822 209 14933	TL431IZ
7302	4822 130 11336	STP16NE06FP
7303	4822 209 14933	TL431IZ
7304	9322 183 38668	STS9NF30L
7305	4822 209 14933	TL431IZ
7306	9322 163 75685	SI2306DS
7307	4822 130 11417	STP3NB60FP
7308	4822 130 61553	DTC124EU
7309	9322 180 12685	SI2312DS
7310	4822 130 41782	BF422
7311	9352 673 56112	TEA1507P/N1
7312	3198 010 42320	BC857BW
7313	3198 010 42310	BC847BW
7314	3198 010 42310	BC847BW
7316	9965 000 09548	PHOTOCOUPLER TCET1108G
7318	4822 130 40959	BC547B
7319	4822 209 14933	TL431IZ
7321	9322 163 75685	SI2306DS
7322	9322 163 75685	SI2306DS
7323	3198 010 42310	BC847BW
7324	4822 130 61553	DTC124EU
7325	9322 163 75685	SI2306DS
7401	3198 010 42310	BC847BW
7402	3198 010 42320	BC857BW
7404	3198 010 42320	BC857BW
7405	3198 010 42310	BC847BW
7407	3198 010 42310	BC847BW
7408	9340 219 30115	BC817-25W
7409	3198 010 42310	BC847BW
7410	9322 173 41668	ST6618
7411	9322 024 55662	NJM2234M
7412	3198 010 42320	BC857BW
7413	3198 010 42310	BC847BW
7414	3198 010 42310	BC847BW
7415	9340 219 30115	BC817-25W
7416	9322 174 75668	NJM2235M
7500	4822 209 62312	MC33078D
7501	5322 209 11102	HEF4052BT
7503	4822 209 62312	MC33078D
7504	5322 209 11102	HEF4052BT
7505	9340 219 30115	BC817-25W
7507	9340 219 30115	BC817-25W
7551	5322 209 11517	PC74HCU04T
7600	9322 186 87668	MSP3415G-QG-B8V3 (MIAS)
7601	4822 130 61553	DTC124EU
7602	9340 219 30115	BC817-25W
7603	9340 219 30115	BC817-25W
7802	9340 219 30115	BC817-25W
7803	9322 174 76668	NJM2267M
7804	9340 219 30115	BC817-25W
7951	4822 209 60177	LM339D
7953	3198 010 42310	BC847BW
7954	3198 010 42310	BC847BW

FEBE BOARD

Various

1000	2422 025 17955	CON V 6P M 1.00 SR R
1001	2422 543 01368	RES XTL 24M576 12P CX8045 R
1002	2422 543 01422	RES XTL 24M576 18P CX8045 R
1100	2422 025 17821	CON H 45P F 0.50 FPC 0.3 R
1302	2422 543 01025	RES XTL 16M93 20P CX-16F R
1400	2422 025 05548	CON H 4P F 1.00 FFC 0.3
1401	2422 025 18382	CON H 11P F 1.00 FPC 0.3
1601	2122 662 00152	PTC 1812 16V 0R18 PM
1602	2122 662 00136	PTC 1812 6V 0R21 PM
1901	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1902	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1903	8204 056 66001	CON V 7P M 2.00 PH R
1904▲	2422 086 11087	FUSE F 1A 125V UL R
1905	8204 056 66011	CON V 12P M 2.00 PH R
1906▲	2422 086 11087	FUSE F 1A 125V UL R
1907	2422 025 16729	CON BM V 10P F 1.00 FFC 0.3 R
1908▲	2422 086 11087	FUSE F 1A 125V UL R

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2013	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2014	4822 124 12095	100UF 20% 16V
2062	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2071	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2073	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2081	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2083	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2098	4822 124 80151	47UF 16V
2107	5322 124 41945	22UF20% 35V
2416	4822 124 12095	100UF 20% 16V
2431	4822 124 23002	10UF 16V
2446	5322 124 41945	22UF20% 35V
2448	2020 552 95812	CER2 1206 X7R 16V 1U PM10 R
2515	4822 124 23002	10UF 16V
2533	4822 124 23002	10UF 16V
2538	4822 124 23002	10UF 16V
2580	5322 124 41945	22UF20% 35V
2612	5322 124 41945	22UF20% 35V
2653	5322 124 41945	22UF20% 35V
2654	5322 124 41945	22UF20% 35V
2666	4822 124 23002	10UF 16V
2667	4822 124 23002	10UF 16V
2668	4822 124 23002	10UF 16V
2669	4822 124 23002	10UF 16V
2812	4822 124 23002	10UF 16V
2818	4822 124 23002	10UF 16V
2828	4822 124 23002	10UF 16V
2838	2020 021 91857	ELCAP FK 6V3 100U PM20 R
2981	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2989	2020 021 91729	ELCAP RKV 35V 4U7 PM20 R
2999	2020 021 91857	ELCAP FK 6V3 100U PM20 R

-WW-

3000	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3001	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3003	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3004	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3005	4822 117 13523	220R 5% RESN 0.63W
3006	4822 117 13523	220R 5% RESN 0.63W
3007	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3008	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3009	4822 117 13523	220R 5% RESN 0.63W
3010	4822 117 13523	220R 5% RESN 0.63W
3025	4822 117 12662	10R X4 5%
3029	4822 117 12662	10R X4 5%
3084	3198 031 11010	RST NETW 1206 4X10OR PM5 COL R
3085	3198 031 11010	RST NETW 1206 4X10OR PM5 COL R
3541	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3542	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3543	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3562	4822 117 13526	150R 5% RESN 0.63W
3583	4822 117 13526	150R 5% RESN 0.63W
3584	4822 117 13526	150R 5% RESN 0.63W
3585	4822 117 13526	150R 5% RESN 0.63W
3587	4822 117 13526	150R 5% RESN 0.63W
3588	4822 117 13526	150R 5% RESN 0.63W
3589	4822 117 13526	150R 5% RESN 0.63W
3615	2350 035 10829	RST NETW ARV24 4X 82R PM5 R
3631	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3635	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3639	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3643	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3800	2350 035 10229	RST NETW ARV24 4X22R PM5 R
3801	2350 035 10229	RST NETW ARV24 4X22R PM5 R
3802	2350 035 10229	RST NETW ARV24 4X22R PM5 R
3803	2350 035 10229	RST NETW ARV24 4X22R PM5 R
3804	4822 117 13573	NETW 4 X 47R 5% MNR14
3805	4822 117 13573	NETW 4 X 47R 5% MNR14
3806	4822 117 13573	NETW 4 X 47R 5% MNR14
3807	4822 117 13573	NETW 4 X 47R 5% MNR14

3808	4822 117 13573	NETW 4 X 47R 5% MNR14
3809	4822 117 13573	NETW 4 X 47R 5% MNR14
3810	4822 117 13573	NETW 4 X 47R 5% MNR14
3811	4822 117 13573	NETW 4 X 47R 5% MNR14
3812	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3813	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3814	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3815	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3846	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3873	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3874	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3875	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3876	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3877	3198 031 14720	RST NETW 1206 4X4K7 PM5 COL R
3897	3198 031 11030	RST NETW 1206 4X 10K PM5 COL R
3903	3198 031 11030	RST NETW 1206 4X 10K PM5 COL R
3904	3198 031 11030	RST NETW 1206 4X 10K PM5 COL R

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5000	4822 157 11499	BLM11P600SPT
5001	4822 157 11499	BLM11P600SPT
5002	4822 157 11499	BLM11P600SPT
5003	4822 157 11499	BLM11P600SPT
5012	4822 157 11499	BLM11P600SPT
5013	4822 157 11499	BLM11P600SPT
5016	4822 157 11499	BLM11P600SPT
5018	4822 157 11499	BLM11P600SPT
5019	4822 157 11499	BLM11P600SPT
5022	4822 157 11499	BLM11P600SPT
5101	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5102	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5103	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5104	3198 018 51090	FXDIND 0603 10U PM10 COL R
5202	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5300	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5301	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5400	2422 536 00501	IND FXD D62LCB 10U PM20 R
5405	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5501	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5502	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5504	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5603	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5607	2422 549 45322	IND FXD 0603 EMI 100MHZ 150R R
5614	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5615	2422 549 45322	IND FXD 0603 EMI 100MHZ 150R R
5616	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5800	4822 157 11499	BLM11P600SPT
5802	4822 157 11499	BLM11P600SPT
5803	4822 157 11499	BLM11P600SPT
5804	4822 157 11717	BLM31P500SPT
5805	4822 157 11499	BLM11P600SPT
5806	4822 157 11717	BLM31P500SPT
5807	4822 157 11717	BLM31P500SPT
5808	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5900	4822 157 11499	BLM11P600SPT
5901	4822 157 11499	BLM11P600SPT
5902	4822 157 11499	BLM11P600SPT
5903	4822 157 11499	BLM11P600SPT
5904	4822 157 11499	BLM11P600SPT
5905	2422 536 00598	IND FXD 1210 1U5 PM20 R
5906	2422 549 45634	IND FXD 0603 EMI 100MHZ 60R R
5909	2422 549 45634	IND FXD 0603 EMI 100MHZ 60R R
5914	2422 549 45634	IND FXD 0603 EMI 100MHZ 60R R
5915	2422 536 00598	IND FXD 1210 1U5 PM20 R
5916	2422 549 45634	IND FXD 0603 EMI 100MHZ 60R R
5917	2422 549 45634	IND FXD 0603 EMI 100MHZ 60R R
5918	4822 157 11499	BLM11P600SPT
5919	2422 536 00598	IND FXD 1210 1U5 PM20 R
5920	2422 536 00598	IND FXD 1210 1U5 PM20 R
5921	4822 157 11499	BLM11P600SPT
5922	4822 157 70649	4,7UH (NL322522T-4R7J)
5923	2422 536 00598	IND FXD 1210 1U5 PM20 R
5924	2422 536 00598	IND FXD 1210 1U5 PM20 R
5925	3198 018 90050	FXDIND 0603 100MHZ 1K COL R
5926	4822 157 70649	4,7UH (NL322522T-4R7J)
5927	4822 157 11499	BLM11P600SPT
5928	4822 157 11499	BLM11P600SPT
5929	4822 157 11717	BLM31P500SPT
5930	4822 157 11499	BLM11P600SPT
5931	2422 535 94995	IND FXD 10145 10U PM20 R
5932	4822 157 11717	BLM31P500SPT
5933	4822 157 11717	BLM31P500SPT
5934	4822 157 11717	BLM31P500SPT
5935	4822 157 11499	BLM11P600SPT
5936	4822 157 11717	BLM31P500SPT

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6001	4822 130 11528	1PS76SB10
6100	4822 130 11397	BAS316
6400	9340 571 37115	PMEG1020EA (PHSE)
6401	9340 571 37115	PMEG1020EA (PHSE)
6402	9340 571 37115	PMEG1020EA (PHSE)
6403	9340 571 37115	PMEG1020EA (PHSE)
6500	4822 130 81637	PMLL4148L
6501	5322 130 31928	BAS16
6502	5322 130 31928	BAS16
6503	5322 130 31928	BAS16
6604	4822 130 11522	UDZ15B
6605	9322 159 72685	MM3Z6V2 (ONSE) R
6900	4822 130 11528	1PS76SB10

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7000	9352 683 02157	PDI1394P25BD (PHSE) Y
7001	9352 682 52557	PDI1394L40 (PHSE) Y
7005	9352 683 81115	74LVC1G32GW (PHSE) R
7006	5322 130 60159	BC846B
7007	9352 673 95518	SAA7118E/V1 (PHSE) R
7008	9322 116 74668	LD1117D33
7101	5322 130 60159	BC846B
7102	5322 130 60159	BC846B
7103	5322 130 60159	BC846B
7104	9340 547 21215	BSH205 (PHSE) R
7201	9352 713 79157	TZA1047HL (PHSE) Y
7300	9352 713 77157	TZA1042HL (PHSE) Y
7401	5322 209 82941	LM358D
7402	9352 735 89518	SA56202TW (PHSE)
7403	5322 209 82941	LM358D
7405	5322 209 82941	LM358D
7409	9322 164 64668	BA5995FM (RHM0) R
7500	9352 737 02557	PNX7850E_Z_M2A (PHSE)
7503	3104 123 97361	FLASH ASSY VAD8041 SW
7504	9322 166 67668	MT48LC4M16A2TG-7E(MRN0)R
7506	9322 184 07685	PST3642N (MITM)
7603	4822 209 17398	LD1117DT33
7607	9322 144 97668	LD1117DT (ST00) R
7608	8204 056 08131	LD1117DT18 (ST00) R
7800	9352 745 77557	PNX7100EH/C3 (PHSE) Y
7804	2722 171 08804	OSC XTL 4MHZ 20P FXO-31 R
7805	9352 115 40118	74LVC245APW (PHSE) R
7900	3104 123 97403	FLASH ASSY 4MB FEBE BACK-END
7902	9322 182 03668	MT48LC8M16A2TG-75(MRN0)R
7903	9322 182 03668	MT48LC8M16A2TG-75(MRN0)R
7904	9322 130 41668	M24C64-WMN6 (ST00) R
7905	9322 130 41668	M24C64-WMN6 (ST00) R
7910	5322 130 60159	BC846B
7913	9352 684 56115	74LVC1G04GW
7914	5322 130 60159	BC846B
7915	9352 684 56115	74LVC1G04GW
7916	5322 130 60159	BC846B
7917	5322 130 60159	BC846B
7918	4822 130 61553	DTC124EU
7920	5322 130 60159	BC846B
7921	5322 130 60159	BC846B
7922	9352 456 80115	74HCT1G125GW
7923	9352 500 20118	74LVC08AD (PHSE) R
7924	9352 317 20118	74LVC125APW (PHSE) R
7926	9322 191 99685	NCP303LSN29 (ONSE) R
7927	9322 188 69668	STS5DNF20V (ST00) R
7928	9322 188 69668	STS5DNF20V (ST00) R
7929	9322 188 68668	NCP1570D (ONSE) R
7950	9340 425 20115	BC847BS (PHSE) R

LECO Board

Various

1002	2422 543 01422	RES XTL SM 24M576 18P CX8045 R
1100	2422 025 17821	CON H 45P F 0.50 SM FPC 0.3 R
1300	2422 086 11087	FUSE SM F 1A 125V UL R
1301	2422 086 11087	FUSE SM F 1A 125V UL R
1302	2422 025 17441	CON BM V 12P M 2.00 PH SMD R
1303	2422 086 11087	FUSE SM F 1A 125V UL R
1304	2422 086 11087	FUSE SM F 1A 125V UL R
1305	2122 662 00152	PTC SM 1812 16V 0R18 PM
1306	2122 662 00136	PTC SM 1812 6V 0R21 PM
1400	2422 025 05548	CON H 4P F 1.00 SM FFC 0.3
1401	2422 025 18382	CON H 11P F 1.00 SM FPC 0.3
1500	2422 543 01453	RES XTL SM 16M934 20P CX8045 R
1700	2422 025 17909	CON BM H 50P F 0.5 54132
1902	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1903	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1911	2422 025 17104	CON BM V 7P M 2.00 PH SMD R
1912	2422 025 16729	CON BM V 10P F 1.00 FFC 0.3 R

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2067	2020 021 91729	ELCAP SM RKV 35V 4U7 PM20 R
2082	2020 021 91729	ELCAP SM RKV 35V 4U7 PM20 R
2087	2020 021 91729	ELCAP SM RKV 35V 4U7 PM20 R
2094	2020 021 91729	ELCAP SM RKV 35V 4U7 PM20 R
2107	5322 124 41945	22UF20% 35V
2300	2022 031 00347	ELCAP SM OCV 6V3 100U PM20 R
2304	2022 031 00347	ELCAP SM OCV 6V3 100U PM20 R
2320	4822 124 23002	10UF 16V
2325	5322 124 41945	22UF20% 35V
2327	5322 124 41945	22UF20% 35V
2416	4822 124 12095	100UF 20% 16V
2431	4822 124 23002	10UF 16V
2446	4822 124 12095	100UF 20% 16V
2515	4822 124 23002	10UF 16V
2531	5322 124 41945	22UF20% 35V
2580	4822 124 80151	47UF 16V
2800	4822 124 23002	10UF 16V
2802	4822 124 23002	10UF 16V
2807	4822 124 23002	10UF 16V
2810	4822 124 23002	10UF 16V
2815	4822 124 23002	10UF 16V
2932	2020 021 91729	ELCAP SM RKV 35V 4U7 PM20 R
2938	2020 021 91729	ELCAP SM RKV 35V 4U7 PM20

-WW-

3083	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3084	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3541	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3542	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3543	3198 031 13390	RST NETW 1206 4X 33R PM5 COL

3545	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3583	4822 117 13526	150R 5% RESN 0.63W
3584	4822 117 13526	150R 5% RESN 0.63W
3585	4822 117 13526	150R 5% RESN 0.63W
3587	4822 117 13526	150R 5% RESN 0.63W
3588	4822 117 13526	150R 5% RESN 0.63W
3589	4822 117 13526	150R 5% RESN 0.63W
3590	4822 117 13526	150R 5% RESN 0.63W
3615	2350 035 10829	RST NETW SM ARV24 4X 82R PM5 R
3631	2120 108 94458	RST NETW SM RAC16 4X 56R PM5 R
3635	2120 108 94458	RST NETW SM RAC16 4X 56R PM5 R
3639	2120 108 94458	RST NETW SM RAC16 4X 56R PM5 R
3643	2120 108 94458	RST NETW SM RAC16 4X 56R PM5 R
3802	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3803	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3804	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3805	3198 031 13390	RST NETW 1206 4X 33R PM5 COL
3811	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3812	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3813	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3814	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3815	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3816	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3817	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R
3821	2350 035 10229	RST NETW SM ARV24 4X22R PM5 R

5010	4822 157 11499	BLM11P600SPT
5011	4822 157 11499	BLM11P600SPT
5012	4822 157 11499	BLM11P600SPT
5013	4822 157 11499	BLM11P600SPT
5014	4822 157 11499	BLM11P600SPT
5015	4822 157 11499	BLM11P600SPT
5018	4822 157 11499	BLM11P600SPT
5101	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5102	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5103	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5104	3198 018 51090	FXDIND SM 0603 10U PM10 COL R
5202	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5300	4822 157 11717	BLM31P500SPT
5301	4822 157 11717	BLM31P500SPT
5302	2422 535 94995	IND FXD SM 10145 10U PM20 R
5303	2422 549 45322	IND FXD 0603 EMI 100MHZ 150R R
5305	2422 549 45322	IND FXD 0603 EMI 100MHZ 150R R
5400	2422 536 00501	IND FXD SM D62LCB 10U PM20 R
5405	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5501	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5502	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5504	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5505	2422 549 44991	IND FXD 0603 EMI 100MHZ 600R
5800	4822 157 11717	BLM31P500SPT
5801	4822 157 11717	BLM31P500SPT
5802	4822 157 11717	BLM31P500SPT
5803	4822 157 11717	BLM31P500SPT
5900	4822 157 11499	BLM11P600SPT
5908	4822 157 11499	BLM11P600SPT
5909	4822 157 70649	"4,7UH (NL322522T-4R7J)"
5910	4822 157 70649	"4,7UH (NL322522T-4R7J)"
5911	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5912	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5913	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5914	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5915	2422 536 00598	IND FXD SM 1210 1U5 PM20 R
5916	2422 536 00598	IND FXD SM 1210 1U5 PM20 R
5917	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5918	4822 157 11499	BLM11P600SPT
5919	2422 536 00598	IND FXD SM 1210 1U5 PM20 R
5920	2422 536 00598	IND FXD SM 1210 1U5 PM20 R
5924	2422 536 00598	IND FXD SM 1210 1U5 PM20 R
5925	2422 536 00598	IND FXD SM 1210 1U5 PM20 R
5926	4822 157 11499	BLM11P600SPT
5927	3198 018 31280	FXDIND SM 0805 1U2 PM10 COL R
5928	3198 018 31280	FXDIND SM 0805 1U2 PM10 COL R
5929	3198 018 31280	FXDIND SM 0805 1U2 PM10 COL R
5930	3198 018 54770	FXDIND SM 0603 0U47 PM10 COL R
5931	3198 018 54770	FXDIND SM 0603 0U47 PM10 COL R
5932	3198 018 54770	FXDIND SM 0603 0U47 PM10 COL R
5933	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5934	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5935	2422 549 45218	IND FXD 0603 EMI 100MHZ 150R R
5940	4822 157 11499	BLM11P600SPT

6001	4822 130 11528	1PS76SB10
6100	4822 130 11397	BAS316
6300	4822 130 11522	UDZ15B
6301	9322 159 72685	DIO REG SM MM3Z6V2 (ONSE) R

7007	9352 683 81115	IC SM 74LVC1G32GW (PHSE) R
7008	5322 130 60159	BC846B
7009	9352 762 35557	IC SM SAA7117AE/ V2(PHSE) Y
7010	9322 217 28668	IC SM LD1117DT18 (ST00) R
7101	5322 130 60159	BC846B
7102	5322 130 60159	BC846B
7103	5322 130 60159	BC846B
7104	9340 547 21215	FET POW SM BSH205 (PHSE) R
7201	9352 749 67157	IC SM TZA1047HL/M2 (PHSE) Y
7300	9322 188 69668	FET POW SM STS5DNF20V (ST00) R
7301	9322 207 93668	IC SM NCP1571D (ONSE) R
7302	9322 217 28668	IC SM LD1117DT18 (ST00) R
7303	9322 163 75685	FET SIG SM SI2306DS (VISH)
7401	5322 209 82941	LM358D
7402	9352 735 89518	IC SM SA56202TW (PHSE)
7403	5322 209 82941	LM358D
7405	5322 209 82941	LM358D
7409	9322 164 64668	IC SM BA5995FM (RHM0) R
7501	9352 755 53557	IC SM PNX7860E (PHSE) Y
7503	3139 240 50981	FLASH EMBEDDED SW (D4.0)
7505	9322 210 30668	IC SM HY57V161610ET-7(HYNX) R
7800	9352 757 62557	IC SM PNX7252EL/C1 (PHSE) Y
7801	5322 130 60159	BC846B
7802	9352 104 20118	IC SM 74LVC244APW(PHSE) R
7900	9322 130 41668	IC SM M24C64-WMN6 (ST00) R
7901	3139 240 50991	FLASH EMBEDDED SW (U4.01L)
7902	3139 240 51011	EEPROM BOOT SW (U4.0)
7903	9322 213 80668	IC SM MT48LC16M16A2P-6A (MRN0)R
7910	9352 684 56115	74LVC1G04GW
7911	5322 130 60159	BC846B
7912	5322 130 60159	BC846B
7913	9352 684 56115	74LVC1G04GW
7914	4822 130 61553	DTC124EU
7916	5322 130 60159	BC846B
7917	5322 130 60159	BC846B
7918	5322 130 60159	BC846B
7919	5322 130 60159	BC846B
7920	9352 456 80115	74HCT1G125GW
7925	9322 191 99685	IC SM NCP303LSN29 (ONSE) R
7926	2722 171 08804	OSC XTL SM 4MHZ 20P FXO-31 R
7927	9352 500 20118	IC SM 74LVC08AD (PHSE) R
7928	5322 130 60159	BC846B
7930	5322 130 60159	BC846B

11. Revision List

Version 1.0: Initial release
Version 1.1: Addition of Lecolite (LECO) module for DVDR610/00/02/05 usage